A 100-120 GHz Quadruple-LO Pumped Harmonic Diode Mixer Using Standard GaAs Based 0.15-µm PHEMT Process

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***Abstract*—A 100-120 GHz 4x sub-harmonically pumped diode mixer using standard 0.15-µm PHEMT process on 4-mil GaAs substrate is presented. Fourth order mixing was performed using an anti-parallel diode pair. Filters and harmonic stubs are implemented using grounded coplanar waveguide structure. The average conversion loss is 27 dB from 100 to 120 GHz, in a compact chip size of 1.0 x 1.0 mm^2.**

***Index Terms*—coplanar waveguide (CPW), millimeter-wave, Schottky diodes, sub-harmonically pumped mixers**

I. Introduction

Several sub-harmonically pumped (SHP) monolithic diode mixers operating over 100 GHz have been presented over the past few years [1]-[3],[5]-[6]. Most of them are of 2nd order LO mixing designs, achieving better than 20 dB conversion losses, with one example achieving better than 15 dB from 78 to 114 GHz [3]. A 4th order LO mixer design achieved a very low conversion loss of 11.4 dB at 94 GHz [6]. With the exception of [3], which utilizes a commercial 0.15-µm GaAs PHEMT process, SHP diode mixers over 100 GHz either use specialized Schottky diode process [6] or InP HEMT technology [1]-[2] which is usually not accessible to public. Furthermore, applications at such high frequency are very limited, mostly in radio astronomy and military. Therefore, SHP mixer above 100 GHz is still a relatively untouched topic in MMIC designs.

In this paper, we present a 100-120 GHz sub-harmonically pumped diode mixer using standard 0.15-µm PHEMT process on 4-mil GaAs substrate. Grounded coplanar waveguide structure was used as the transmission line medium. The average conversion loss is 27 dB from 100 to 120 GHz with a chip size of 1.0 x 1.0 mm^2.

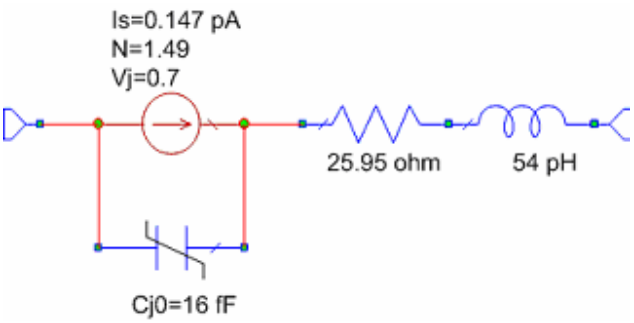

Fig. 1. The equivalent circuit of the 2-finger 15-µm gate-width diode

II. Circuit Design and Fabrication

A. Process Description

This subharmonic mixer was designed using WIN Semiconductors 0.15-µm pHEMT MMIC process on 4-mil GaAs substrate. This is a two-metal airbridge process, with device f_T of 85 GHz and maximum transconductance of 495 mS/mm; passives such as thin film resistors, spiral inductors and MIM capacitors are also provided.

Since the foundry does not provide standard Schottky diodes in the design library, various diode sizes were designed and measured ranging from 200-µm to 15-µm gate widths, realized by connecting the source and drain of a transistor. The smallest diode was used to minimize the parasitics: a two-finger diode with total gate width of 15-µm, which has a cutoff frequency of 380 GHz. The equivalent circuit of the diode and its parameters are shown in Fig. 1. The fitted dc-IV curve of the model to the measured one is plotted in Fig. 2, and Fig. 3 shows the fitted S-parameters of the model to the measured S-parameters at various biases from 1 to 50 GHz. From Fig. 2 and Fig.3, it can

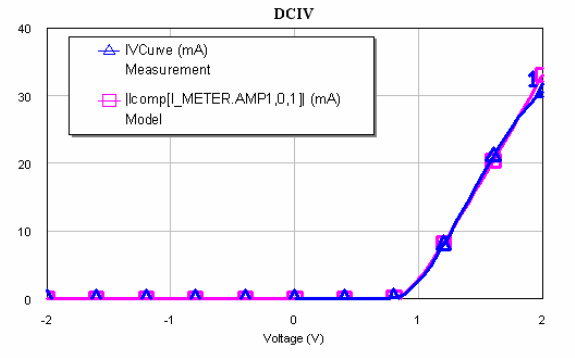

Fig. 2. Comparison of IV curve between measurement and model

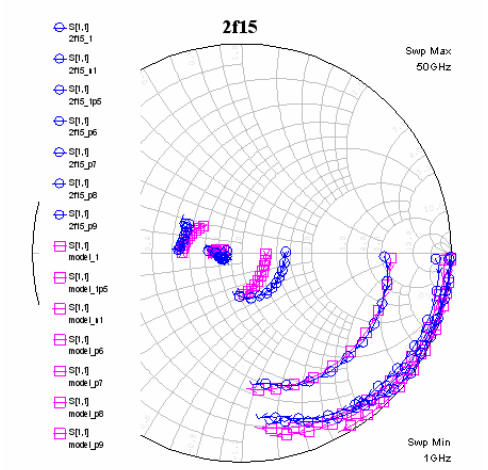

Fig. 3. Comparison of S-parameters between measurement and model. The bias points shown are: -1 V, 0.6V, 0.7V, 0.8V, 0.9V, 1V, and 1.5V

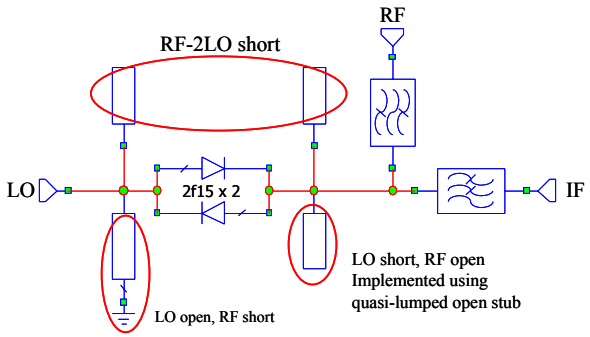

Fig. 4. The schematic of the 100-120 GHz 4x sub-harmonic mixer.

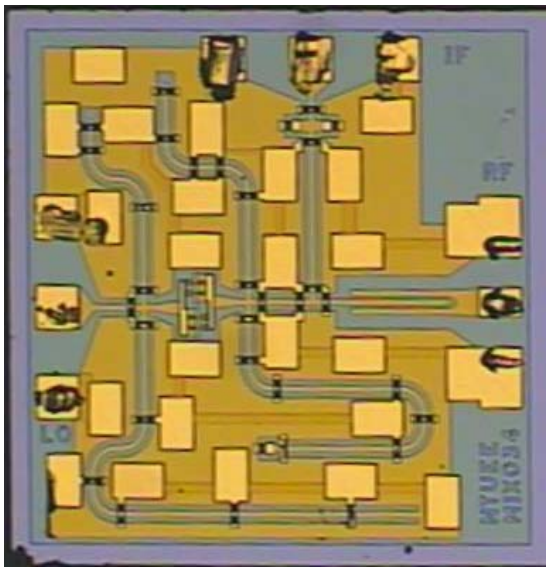

Fig. 5. The layout of the 4x sub-harmonic mixer. The chip size is 1.0 x 1.0 mm^2.

be observed that the model is fitted reasonably well up to 50 GHz.

B. Circuit Design

The schematic of this circuit is based on the circuit schematic

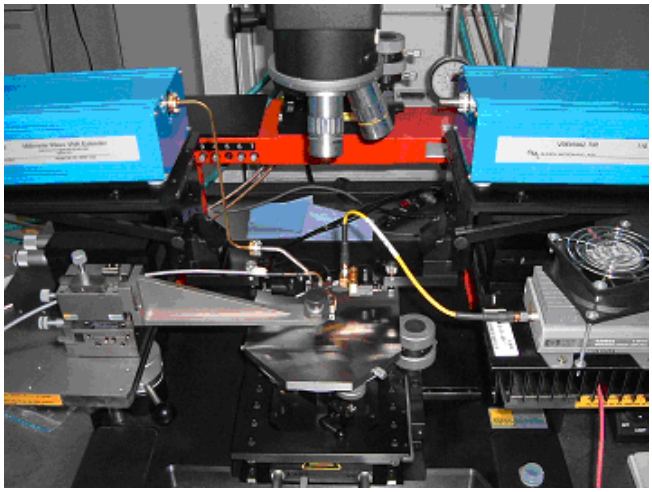

Fig. 6. The measurement setp of the 4x sub-harmonic mixer.

of [6], shown in Fig. 4. In our implementation, we utilized grounded coplanar waveguide (GCPW) as our transmission line structure. Via-holes were judiciously placed to prevent unwanted parallel plate modes in substrate. An anti-parallel diode pair is used to create the mixing signal. Two open stubs connected to both ends of the anti-parallel diode pair are used to suppress the 2nd order LO mixing signal (f_{RF}-$2f_{LO}$), a quarter wavelength short stub at the LO port acts as an open for LO signal and short for RF signal, and a quasi-lumped open stub at the RF-IF end acting as LO short and RF open. The chip photo is shown in Fig. 5, with a chip size of 1.0 x 1.0 mm^2.

III. Measurement Results

The circuit is measured via on-wafer probing. The measurement setup is shown in Fig. 6. The RF signal is provided by an Agilent 8510C Network Analyzer with OML V06VNA2 D-band Millimeter Wave VNA Extender, which are the two blue boxes shown in Fig. 6 (only the left one is used). The power is calibrated using Elva-1's D-band CW power meter (not shown in Fig. 6). LO source is from an HP 83650B signal generator with an HP83050A amplifier to provide the required power level (only the HP83050A is shown on the right). IF signal is measured using an Agilent spectrum analyzer, which is also used to measure the isolation signal (not shown in Fig. 6). All of the measurements are calibrated to the probe tips.

The measured conversion loss vs. LO power is plotted in Fig. 7. The LO frequency is set at 27.25 GHz. Best conversion loss is achieved at 15 dBm LO power for various RF frequency. Fig. 8 shows the conversion loss over RF frequency with LO set at 27.25 GHz and 15 dBm. The simulated conversion loss is plotted as a broken line. Two sets of measured data from two chips are plotted, showing good consistency, and have the same shape as simulation, albeit a slightly higher conversion loss. The measured conversion loss is better than 30 dB from 100 to 120 GHz with best performance at 115 GHz of 25.5 dB.

There are several reasons to the difference in conversion loss between simulation and measurement. The first reason is the

extraction of the models is based on S-parameter measurements up to 50 GHz. The parameters may be a bit different at the operating frequency of this circuit. The second reason is the extensive use of full wave simulation for junctions and turns, which may cause quirks and numerical errors during harmonic-balance simulation. Both of these reasons may be supported by simulation: an increase of 5 ohms series resistance and 5 fF junction capacitance will degrade the conversion loss to about -23 dB at 108 GHz, with only a slight change in model IV curves and S-parameters; from simulation, there is a kink at 117 GHz, which is not intuitively correct, and warnings due to use of EM results are also observed during simulation. The above observations are not definitive conclusions, further measurements and circuit verifications are needed to improve the accuracy of the simulations.

IV. Conclusion

A 4th order LO mixing sub-harmonically pumped diode mixer operating at 100 to 120 GHz is presented. This circuit was fabricated using a commercially available 0.15-μm GaAs pHEMT process. The conversion loss is 25.5 dB to 30 dB, with a very small chip size of 1.0 x 1.0 mm^2.

Acknowledgment

This work was supported in part by the National Science Council of Taiwan, R.O.C. (project numbers NSC 93-2213-E-002-033, NSC 93-2219-E-002-024, and NSC 93-2752-E-002-002-PAE). The chip fabrication was coordinated by the Chip Implementation Center (CIC), Taiwan. The authors would like to thank Mei-Chao Yeh, Jia-Hsiang Fu, and Pei-Si Wu for the diode measurements and model characterizations.

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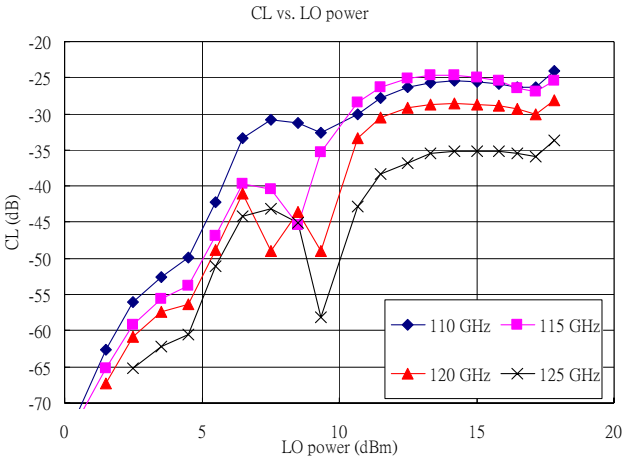

Fig. 7. Conversion loss vs. LO power at 110, 115, 120, and 125 GHz RF frequencies.

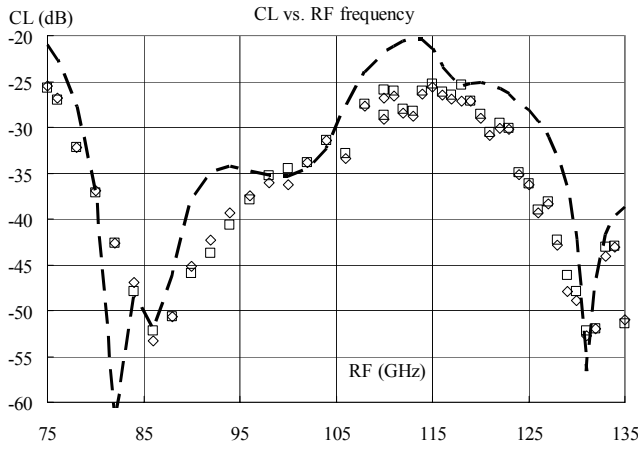

Fig. 8. Conversion loss vs. RF frequency. LO is set at 27.25 GHz and 15 dBm. The measurements for two chip dies are plotted.