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Coupled single-electron transistors as a differential voltage amplifier

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Abstract. We have investigated a possible application of single-electron transistor (SET) devices for use as a differential voltage amplifier. The device consists of a box-SET and probe-SET coupled with each other through a tunnel junction, with the gate electrodes of the two SETs acting as differential signal inputs. The voltage across the probe-SET at a fixed bias current provides information about the charge states of both the probe-SET and the box-SET, which was confirmed by simulations based on the orthodox theory of single-electron tunnelling. When operated as a differential amplifier, the output probe-SET voltage signal was measured as a function of the two gate input signals. While the output signal was found to be proportional to the difference in the two input signals, it remained unchanged for input signals of the same amplitude (referred to as the common mode signal), and the common-mode rejection ratio was found to be 27.5 dB.

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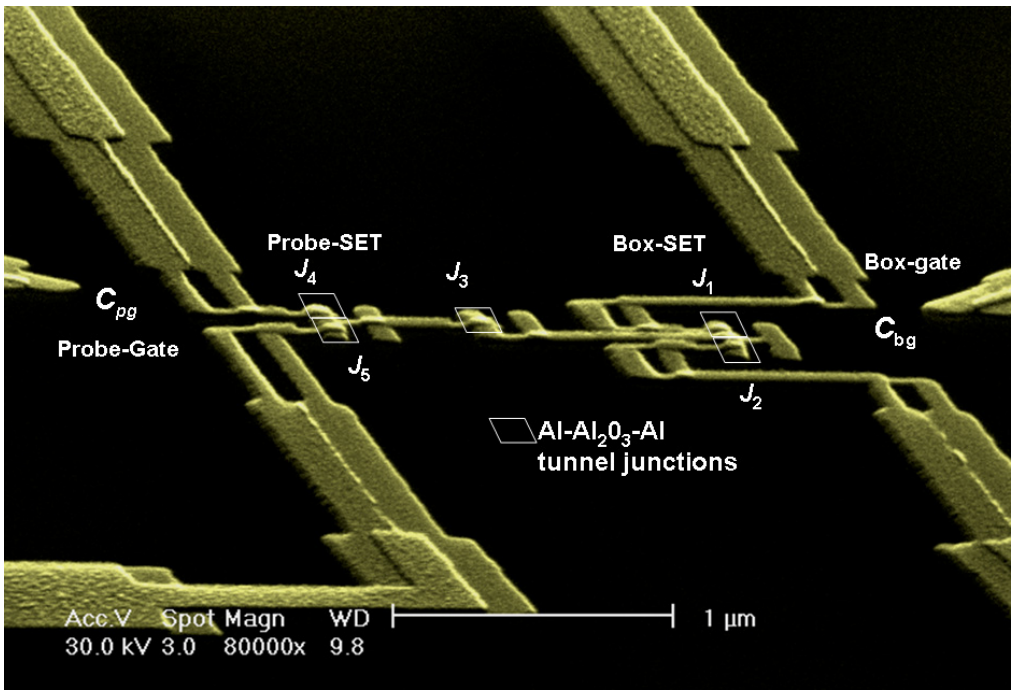
The single-electron transistor (SET) holds great promise for its potential in the next generation of electronic devices because of its great advantages in low power consumption and high packing density. SETs with various kind of materials have been realized [1]–[4], and they have been shown to possess extremely high charge sensitivity, outperforming state-of-the-art field-effect-transistors by three orders of magnitude [5]–[7]. In particular, the SET's capability to amplify small charge signals on a fast timescale has made it an useful detector for a variety of applications [8]–[10], and should prove useful in ultra-low-noise analogue-circuit applications. However, research into SET analogue-circuitry has been rather limited. One of the reasons is that when used as an electrometer, SET suffers from the inevitable random charge noises present in the surroundings, which largely limits its sensing capability. On the other hand, the operational amplifier is a widely used building block in analogue circuits. The most important feature of this device is the differential signal amplification, which allows for rejection of the common mode noise and hence significantly increases the signal-to-noise ratio. Here, we propose and demonstrate an SET-based differential voltage amplifier which utilizes the advantages of the high charge sensitivity of the SET and the differential amplifier's ability in resistance to the external noises. Our circuit consists of a pair of coupled SETs (CSET). Similar circuitry was reported previously [11]–[13], but these studies focused on detection of charge states of the SET islands. In this study, the charge states of the junction-coupled metallic islands have been mapped out and operation of this SET differential voltage amplifier was demonstrated. Furthermore, application of the CSET as a readout device for qubits is discussed.

Figure 1(a) shows a scanning electron microscope (SEM) image of a measured CSET device. The SETs are made of aluminum and were fabricated on a thermally oxidized silicon substrate by standard e-beam lithography and shadow evaporation techniques [14]. The SET on the left, referred to as a probe-SET, serves as an electrometer, whose island is coupled to the island of the adjacent SET, referred to as a box-SET. The central islands of the two SETs are coupled via a tunnel junction j_3 with capacitance C_m, located at the overlap between the two central islands. The area of all junctions (including the coupling junction and SET junctions) is about $80 \times 80\,\mathrm{nm}^2$. Assuming a specific capacitance [15] of 45 fF $\mu\mathrm{m}^{-2}$, the junction capacitance was estimated to be 300 aF, corresponding to a charging energy (E_C) of about 130 μeV (or 1.5 K). Two signal gate electrodes are placed about 500 nm away from the two SET islands and are used to tune the potential of adjacent islands. In addition, two compensate gate electrodes (not shown in the SEM image) are placed about 2.5 μm away from the SET islands, and are used to cancel out unwanted charge induced by the crosstalk.

Transport measurements were conducted in a dilution refrigerator at a temperature of about 80 mK, which corresponds to an energy scale much lower than the charging energy of the two SETs. Figure 2 shows current–voltage (I_p–V_p) characteristics of the probe-SET. The low-temperature I_p–V_p characteristics displayed prominent Coulomb-blockade structures. At temperatures well below the superconducting transition temperature ($\sim$1.2 K) of the aluminum electrodes, the devices showed a sharp supercurrent structure in the low bias voltage region, as shown in the inset (a) of figure 2. The single-electron tunnelling should manifest itself in an oscillatory modulation of the source-drain current I_p as a function of the applied voltage V_{pg} on the probe-gate. The inset (b) of figure 2 shows this modulation at the Josephson-quasiparticle peak [16] of the probe-SET. Based on the current–gate voltage modulations, the device parameters including gate capacitance of both the SETs were estimated. To map out the charge states the probe-SET was symmetrically current-biased and the box-SET was short-circuited and grounded, as illustrated in figure 1(b). To cancel out the effect of crosstalk due to unwanted capacitive

(a)



(b)

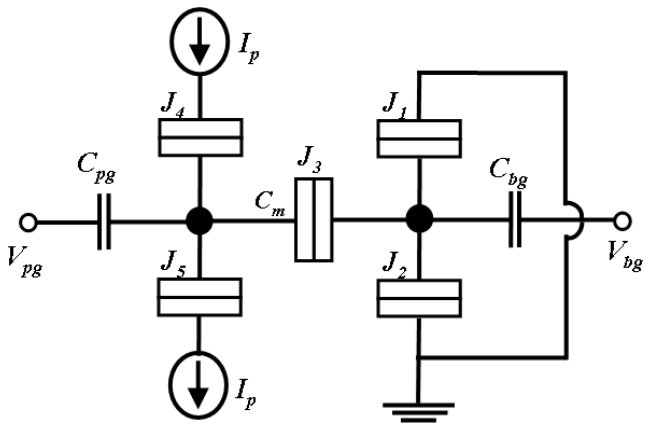


Figure 1. (a) SEM image of a measured sample. The junction areas are marked by white parallelograms and the two control gates are located outside the image. (b) Schematic diagram of the coupled-SET circuit with bias circuit. The electrons in the two islands are allowed to exchange through the tunnel junction J_3 with capacitance C_{m}.

coupling between the probe-SET gate to the box-SET island ($C_{\mathrm{pg\_b}}$) and the box-SET gate to the probe-SET island ($C_{\mathrm{bg\_p}}$), compensation voltages (V_{bcg} and V_{pcg}) were applied to the two compensation gates:

$$V_{\mathrm{bcg}} = V_{\mathrm{pg}}(C_{\mathrm{pg\_b}}/C_{\mathrm{bcg}}) \qquad V_{\mathrm{pcg}} = V_{\mathrm{bg}}(C_{\mathrm{bg\_p}}/C_{\mathrm{pcg}}),$$

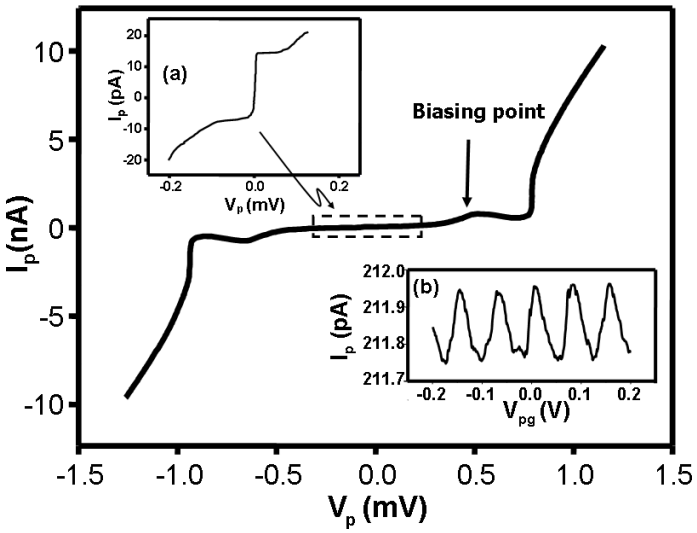


Figure 2. I_p–V_p characteristics of the probe-SET measured at 80 mK. The inset (a) shows a blow-up region where a sharp supercurrent structure is clearly seen. The inset (b) shows oscillatory I_p–V_{pg} modulation at $V_p = 0.52$ mV, as indicated by the arrow in the main plot.

where C_{bcg} (C_{pcg}) is the capacitance between the box (probe) compensation gate and the respective SET islands. With this compensation, the charge states of the two islands were mapped out by the source-drain voltage (V_p) of the probe-SET at a fixed bias current. Figure 3(a) shows an intensity plot of V_p taken at $I_p = 0.43$ nA as a function of the gate voltage on probe-SET (V_{pg}) and the gate voltage on box-SET (V_{bg}). The dark regions have low V_P values (minimum Coulomb blockade) with island charge number varying between two successive integers and the brighter regions correspond to the higher V_P values (maximum Coulomb blockade) where the average numbers of island charges are fixed. The key feature of figure 3(a) is the systematic and repeated presence of breaks in the Coulomb-blockade peak due to addition or removal of one electron from the box-SET.

For a comparison, figure 3(b) shows the intensity plot of V_P made by simulation with the same device parameters and under the same operating conditions. The corresponding charge states on the two islands (b, p), where b and p are the number of excess electrons on the box- and probe-islands respectively, are also indicated. For illustrative purposes, the regions (0, 0), (1, 0), (0, 1) and (1, 1) are labelled as a, b, c, d respectively, and the borders separating a, b, c and d are labelled as ab, ac, bc, cd and bd respectively. Borders ab and cd are dark ridges where Coulomb blockade is at the minimum on the probe island. On border bc both states (0, 1) and (1, 0) are degenerate, and due to electrostatic charge repulsion between the probe- and box-islands the probe-SET current is suppressed, resulting in a slightly higher voltage drop V_p compared to that on borders ab and cd. Borders ac and bd were not probed in the present measurement configuration. In order to understand figure 3(b) in detail, the device is modelled using a classical capacitance circuit. The total electrostatic energy is given by [17]

$$E_{\text{static}} = \frac{1}{2}\Delta Q^T \begin{pmatrix} C_{\Sigma b} & -C_m \\ -C_m & C_{\Sigma p} \end{pmatrix}^{-1} \Delta Q, \tag{1}$$

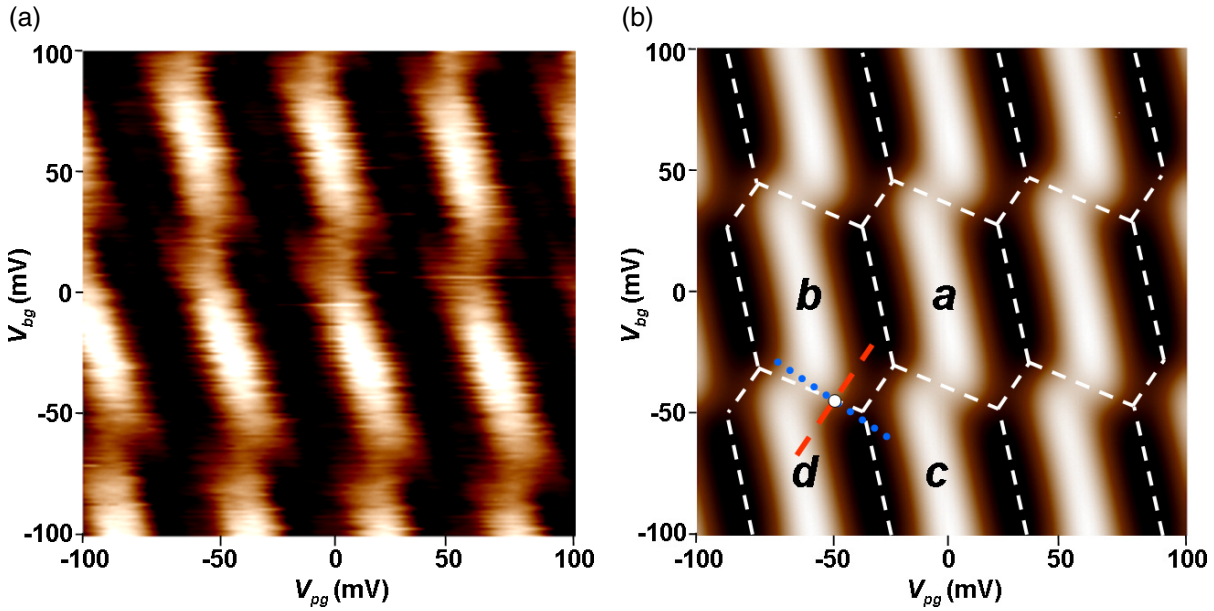


Figure 3. (a) Intensity plot of V_P as a function of gate voltages V_{bg} and V_{pg} measured at $I_p = 0.43$ nA. Bright regions indicate high V_p values. (b) The same plot as in (a) but made by simulation. The dashed line and dotted line indicate the applied gate voltages for common-mode and differential-mode input signals, respectively.

with

$$\Delta Q = \begin{pmatrix} eN_b - C_{bg}V_{bg} \\ eN_p - C_{pg}V_{pg} \end{pmatrix}.$$

Here $C_{\Sigma b}$ and $C_{\Sigma p}$ are the total capacitances seen by the box- and probe-islands, respectively. The formula implies that the total electrostatic energy stored on the two SETs is a result of the difference between the quantized charge in the islands and the continuous charge induced by the external gate voltages. From this expression it is clear that the energetically stable charge state (b, p) of this model depends critically upon the two gate voltages and the magnitude of the coupling capacitances. Based on this model, a numerical calculation (for the computer program algorithm, see [18]) was made using the orthodox theory [19] of single-electron tunnelling and showed good agreement with the measurement results displayed in figure 3(a). This suggests that the charge states of the two coupled islands could be mapped using one of the two SETs as a probe. Furthermore, there exists a section of the contour curves which fulfils the condition $V_{pg} = V_{bg}$, and this section is parallel to border bc. This feature allows the device to be operated as a two-input amplifier with an output proportional to the difference in the input signals, yet insensitive to the common-mode signals.

The differential voltage amplifier is a basic analogue circuit used in all linear integrated circuits. Taking advantage of the common-mode noise rejection, the differential amplifiers possess the important features of high open-loop gain with a large signal-to-noise ratio. Here, we operated the coupled-SET circuit as a differential amplifier, and the results are shown in figure 4. When the same gate voltages were applied along the section of the contour curve

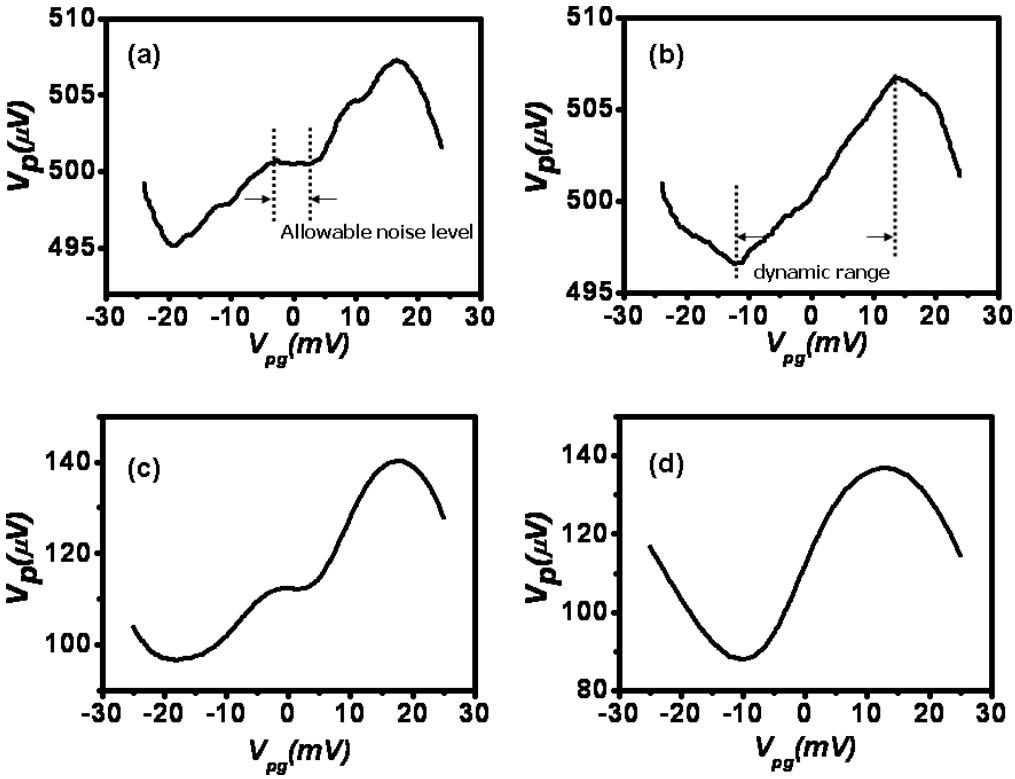


Figure 4. (a) For common-mode signals: V_p as a function of V_{pg} traced along the dashed line in figure 3(b). (b) For differential-mode signals: V_p as a function of V_{pg} traced along the dotted line in figure 3(b). (c), (d) The same plot as in (a) and (b) but made by simulations.

(i.e. common-mode signal $V_{pg} = V_{bg}$, along the red-dashed line in figure 4(a), the output voltage V_p remained unchanged. In contrast, when opposing gate signals were applied ($V_{pg} = -V_{bg}$, along the blue-dotted line in figure 4(a), V_p increased linearly with the gate voltages. Figures 4(c) and (d) show respectively the simulation results for common-mode signals and differential-mode signals at the same source-drain current and in the same gate voltage range, which also shows good agreement with the measurement results. The common-mode rejection ratio is defined as:

$$\mathrm{CMMR(dB)} = 20 \times \log\left(\frac{A_d}{A_{cm}}\right), \tag{2}$$

where A_d is the differential-mode gain and A_{cm} is the common-mode gain. In this device, the common-mode rejection ratio was calculated to be 27.5 dB. Although this may not be better than that of commercial operational amplifiers, with the unrivalled charge sensitivity of the SETs, this device should exhibit its niche in applications such as detection of charge-qubits. In a readout scheme incorporating a CSET device, the probing-gate and box-gate electrodes can be arranged such that the random offset charges are probed by both gates and the qubit signal is probed by the probing-gate alone. Such an arrangement means the readout problem arising from random offset charges should, to a certain extent, be solved and an improved signal-to-noise ratio is expected. To take full advantage of the common-mode noise rejection, one can configure a differential

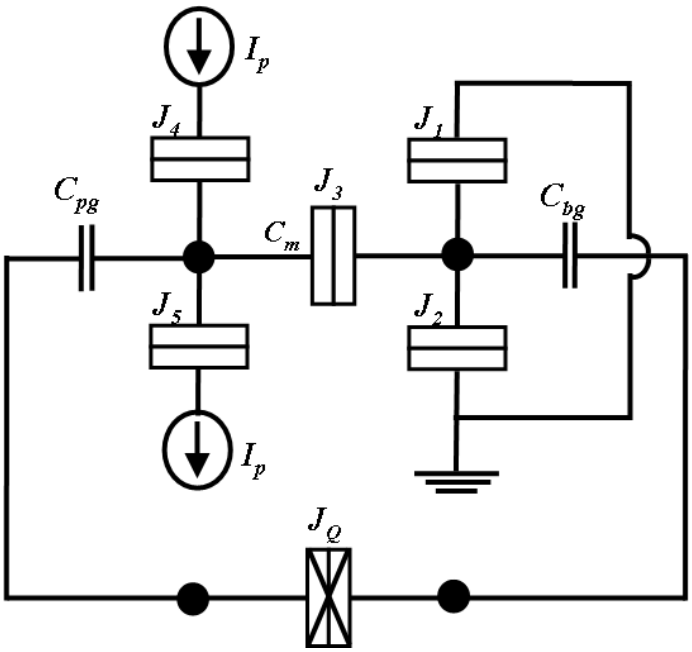


Figure 5. The proposed CSET readout circuit for a differential qubit with the two superconducting boxes coupled by a Josephson junction J_Q.

qubit in the form of a gradiometer proposed by Shnirman *et al* [20] with the readout circuit proposed by Bladh *et al* [21]. As shown in figure 5, the qubit consists of two superconducting boxes weakly coupled via a Josephson junction J_Q, and the set of basis states is parametrized by the Cooper-pair number difference between the two boxes whose charge states are detected by the probing-gate and box-gate electrodes. Tunnelling of a Cooper pair from one box to the other would cause the same amount of changes in V_{pg} and V_{bg} but with opposing sign, which is similar to the differential-mode operation shown in figures 3(b) and 4(b). Further, if J_1 and J_2 are current-biased from the same source as for J_4 and J_5, then the readout circuit is completely symmetric and the qubit should experience less noise from the readout SETs as far as the common-mode source noise is concerned. This circuit is also compatible with the radio-frequency SET (RF-SET) scheme [22], which can be used for high sensitive, fast readout of the qubit charge states.

The similarity between the CSET device and the coupled qubit device demonstrated by Pashkin *et al* [23] is apparent. The only difference is that the coupling capacitance in their devices is replaced by a tunnel junction J_3 in our CSET. Consequently, the Hamiltonian of the CSET in the superconducting state is modified as (cf equation (1) of [23])

$$H = \begin{bmatrix} E_{00} & -\frac{1}{2}E_{J1} & -\frac{1}{2}E_{J4} & 0 \\ -\frac{1}{2}E_{J1} & E_{10} & -\frac{1}{2}E_{J3} & -\frac{1}{2}E_{J4} \\ -\frac{1}{2}E_{J4} & -\frac{1}{2}E_{J3} & E_{01} & -\frac{1}{2}E_{J1} \\ 0 & -\frac{1}{2}E_{J4} & -\frac{1}{2}E_{J1} & E_{11} \end{bmatrix}, \tag{3}$$

where E_{J3} is the Josephson coupling energy of J_3. The energy diagram along border *bc* shown in figure 6 (cf figure 2 in [23]) suggests a decreasing energy difference between (1, 0) and (0, 1) states at the degenerate point with increasing coupling strength.

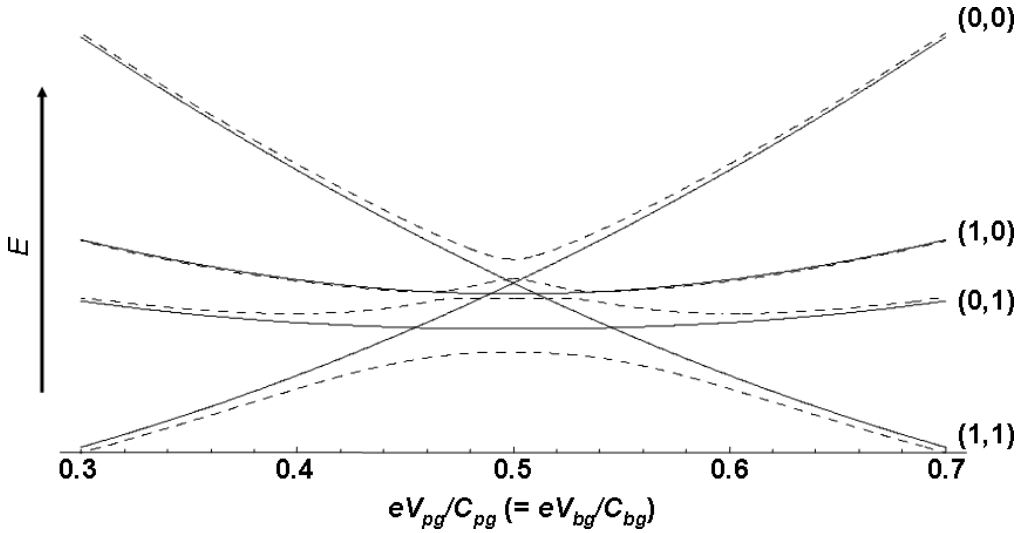


Figure 6. Energy diagram of the CSET in the superconducting state along border *bc* (see figure 3(b). The diagram shows the ground state electrostatic energies (solid curves) and the eigenenergies of the Hamiltonian in equation (3) (dashed curves) for states (b, p) noted beside each curve. Device parameters from [23] are used for a comparison, and an E_{J3} of 40 μeV is assumed.

In conclusion, we have proposed and demonstrated a SET differential amplifier with good common-mode noise rejection characteristics. The charge states of the two SET islands were mapped out and confirmed by simulations. The device was operated as a differential amplifier with the two gates acting as positive and negative signal inputs, and a common-mode rejection ratio of about 27.5 dB was obtained. Such a device should have a niche in applications where detection of small charge signal in a noisy environment is required. In particular, the CSET device is well suited for the readout of differential qubits.

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