行政院國家科學委員會專題研究計畫 期中進度報告

可應用於軟性電子的 TFT 電路設計技術之開發--子計畫五：適用於軟性顯示器 TFT 陣列的缺陷容忍技術之開發 (1/3)

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適用於軟性顯示器TFT陣列的缺陷容忍技術之開發

一、中文摘要

使用軟性基板並且將TFT array的周邊電路整合到基板上已成為平面顯示器的發展趨勢。在可見的未來，高度整合的軟性顯示器TFT array在改善良率、提升系統可靠度、降低生產測試成本等方面都將遇到重大的挑戰。

對平面顯示器而言，TFT array的生產測試在整個生產過程中扮演一個極為重要的角色。確保只有合格的TFT array模組進入後段的組裝程序可以避免其他模組的浪費，降低生產成本。此外，詳盡的TFT array測試資料也可以幫助製程的監控，作為良率提升的依據，對於新建立的製程與生產線格外重要。而隨著pixel的面積變小與數目增加，生產毫無瑕疵的TFT array將變得更為困難，修復技術與缺陷容忍技術將是維持可接受良率的重要關鍵。

本計畫預計執行三年，目的為開發適用於軟性顯示器TFT陣列的缺陷容忍技術。第一年的主要目標為發展TFT array的可測試性設計技術，首先將探討TFT array的錯誤模型，接著將發展TFT array的可測試性設計電路架構（包括電量量測電路與測試匯流排）。第二年的計畫目標為評估所提出的可測試性設計技術並發展TFT array的連線缺陷修復技術。在第三年，將評估第二年所提的修復技術並將可測試性與修復用電路進行整合。此外，也將探討可容忍缺陷的pixel架構。

平面顯示器已成為台灣繼晶圓廠、IC設計之後，最重要的產業之一。面對亞洲各國的強烈競爭，台灣必須在生產測試、良率與可靠性方面保持技術優勢才能維持領先的地位。本計畫所研發的TFT aray可測試性設計、修復、與缺陷容忍技術將可有效提升國內平面顯示器工業的技術層次與競爭力，對未來台灣成為全球平面顯示器的重要供應及研發重鎮會有深遠影響。

關鍵字 – 軟性顯示器、TFT array、可測試性設計技術、修復技術、缺陷容忍技術

二、英文摘要

The adoption of plastic substrate and the integration of peripheral circuitry on to the same substrate has become the trend of flat panel display. For highly integrated flexible displays, the industry will face severe challenges in yield improvement, reliability improvement, and lowering manufacturing testing cost in the near future.

For flat panel display, testing of the TFT array plays a very important role—ensuring that no defective TFT array proceeds to the assembly line can reduce unnecessary waste of other modules. Besides, thorough manufacturing testing also helps process monitoring and yield improvement, which is important especially for newly established fabrication line. As the pixel size continues shrinking and the display size growing, it will be more and more difficult to produce defect-free TFT arrays. Repair and defect-tolerance will be keys to maintain acceptable yield.

The ultimate goal of the proposed project is to develop, for flexible TFT arrays, defect tolerant techniques. In the first year, we will first investigate and propose suitable fault models for flexible TFT arrays. Then, we will develop design-for-test circuitry including charge sensing and test bus. In the second year, we will evaluate the developed DfT techniques, and propose line repair techniques. Finally in the third year, the proposed repair techniques will be evaluated and validated. Integration of the DfT and

repair circuitry will be conducted to reduce the area overhead. We will also investigate defect-tolerant pixel structure.

Flat panel display has become the next most important industry for Taiwan. With the competition from other countries in Asia, it is crucial that Taiwan stays ahead of others in the areas of TFT array DfT, repair, and defect tolerant techniques. The techniques developed in this project will help Taiwan's flat panel industry maintains their technology leadership, which is essential for Taiwan to become the top player in the global flat panel display market.

Keywords - flexible display, TFT array, design-for-test, repair, defect tolerant

三、前言

Flexible display devices are attracting growing attending as they have the characteristics of being conformal, light-weight, and highly portable.

To meet the consumers' demand of higher picture quality, the pixel size of the TFT array continues shrinking. For manufacturing testing, smaller pixels cause two problems. First, higher mechanical accuracy is required to establish concurrent and stable connection between the automatic test equipment (ATE) and the gate/data lines. Secondly, higher measurement accuracy is needed as per pixel charge decreases as well. For ATE vendors, both are great challenges to meet.

In addition to improving picture quality, the display size and pixel count are both growing. Not only handling and probing such displays becomes difficult, but also the test time increases. Furthermore, yield management becomes a significant issue. Besides enhancing the test quality so as to obtain the information needed for process tuning, self-repair and defect-resilient techniques for TFT array are also promising techniques for yield improvement in the future.

Integration of the TFT array peripheral and control circuits onto the same panel creates even more challenges. First of all, access to the gate and data lines are limited, and proper isolation will be needed if the conventional test items are to be performed. Secondly, testing the on-panel circuits, digital or mixed-signal, is non-trivial.

While the above issues are common to all TFT array based displays. Flexible displays have their own problems. Being flexible, these displays must endure constant bending, which could damage the devices or wires.

These testing and yield issues could easily become the manufacturing bottleneck if they are not considered in the early system design stage.

四、研究目的

As mentioned in the previous discussions, highly integrated flexible displays will pose serious challenges on manufacturing testing, yield, and reliability. To solve these problems, in this project, we will investigate design-for-test, repair, and error-resilient techniques for TFT arrays.

In addition to enhance test quality, self-testing is also essential for diagnosis and repair. During testing, the added design-for-test circuitry digitizes the analog quantities. This way, the requirement on ATE accuracy and performance is greatly reduced.

TFT array repair is intended to enhance yield and reliability. With redundant circuits and wiring, the repairable defects can be fixed by properly re-configure the TFT array. Before the LCD assembly process, repair

can enhance the yield. In the field, the built-in repair mechanism can be utilized to repair defects cause by constant bending.

Currently, TFT array repair techniques are limited to wire shorts or opens. No practical repair techniques exist for pixel defects. To lower the impact of pixel defects on yield, this project will focus on pixel fault-tolerant technique for common defects like TFT leakage, TFT defects.

五、文獻探討

A. Conventional TFT Array Testing

Traditional TFT array testing can be categorized into charge sensing, voltage imaging, and electron beam schemes [Freeman00][Lin05][Hunter05]. In voltage imaging and electron beam schemes, special array patterns are written using shorting bars (Figure 1) in order to reduce the required electrical contact. The pixel voltage map is then obtained using voltage imaging or electron beam. With the trend of larger display, higher pixel count, and smaller pixel size, ATE must be accurate and stable in both the mechanical and electrical construction.

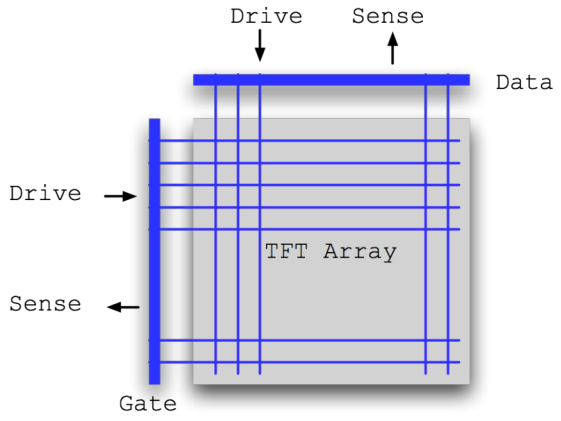

Figure 1 Shorting bar (1G1D).

During charge sensing testing, the electrical characteristics of each TFT transistor are obtained via voltage and current measurement. By comparing the amount of charge written into and read from each pixel, one can determine whether the pixel is defective or not. Not that, data and gate line open/short defects are detected at the same time. For fifth generation technology or beyond, charge sensing techniques are challenged by high ATE/probe cost, maintenance of stable electrical contact, and long test time.

Among the three approaches, charge sensing is more promising.

1. Optimized data pattern can be written to the pixels to achieve better defect detectability.
2. The required electrical contact can be reduced and simplified by adding design-for-test circuitry.

Thus, the proposed TFT array self-testing technique will be based on charge sensing testing.

B. DfT Techniques

In [Wright95], the authors proposed, for gate and data wire connectivity testing, a technique to reduce both the number of contact points and test time. The idea is to connect the wires under test head-to-tail via probe-card during testing (Figure 2). By comparing the measured current and voltages at “Top” and “Bottom” with the ideal values, one can determine the type and location of the defects. The drawbacks of this approach include (1) limited types of detectable defects, (2) limited diagnosis resolution, and (3) limited to wire defects.

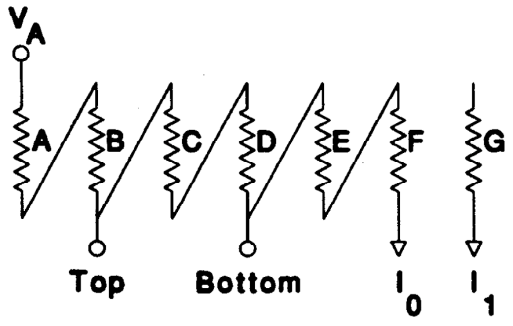

Figure 2 Connectivity testing in [Wright95].

In [Kodate99], the authors propose to lower the number of contact points by utilizing on-panel multiplexers. The drawback is that longer time is needed to write the pixel data.

In [Lin05], a DfT technique is proposed for testing of OLED pixel (Figure 3). Before the TFT array enters the OLED process, the driving transistor (T_{DV}) is un-testable. To solve this problem, an additional capacitor C_{TEST} is added.

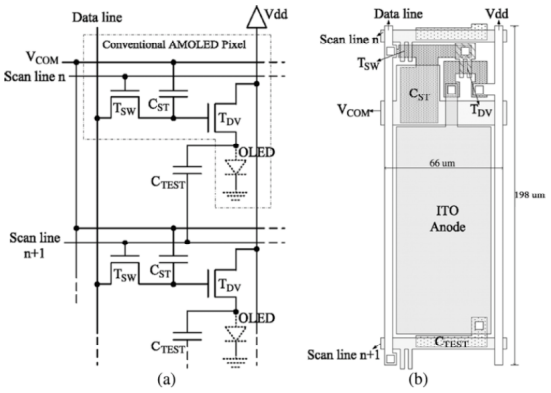

Figure 3 DfT technique for OLED pixel.

C. Repair Techniques

For high-density memory, adding redundancy for repair has become a must. For TFT array, the growing display size and shrinking pixel size also necessitates repair. However, as the relative physical locations of the pixels cannot be modified, memory repair techniques, e.g., redundant I/O, rows, in general are not applicable to TFT array. Currently, available TFT array repair techniques target the wire defects.

In [Wright98], the authors propose the "Active Line Repair (ALR)" technique to repair the line open defects. As shown in Figure 4, an open in the data wire is fixed by driving the lower segment using the bottom data drivers. In addition to the redundant drivers and wires, sophisticated control mechanisms (not shown) are needed to make the repaired array function correctly. Repairing wire short defects is more complicated. One has to apply laser cutting first to transform the short defect to open defects.

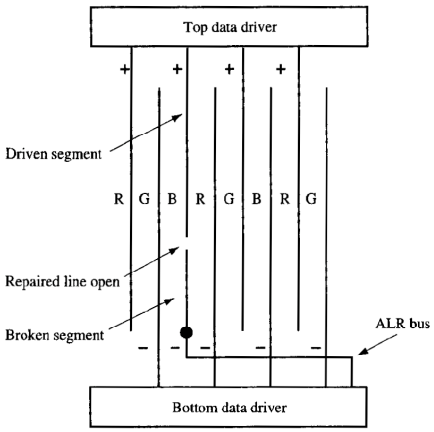

Figure 4 ALR technique in [Wright98].

D. Defect Resilient Techniques

Other than process tuning and repair, another way to elevate yield is to make the TFT array defect resilient.

Driving the data and gate lines from both ends (Figure 5) is the simplest wire open tolerant technique [Wright98]. The disadvantages of this method include the large amount of redundant drivers and wiring.

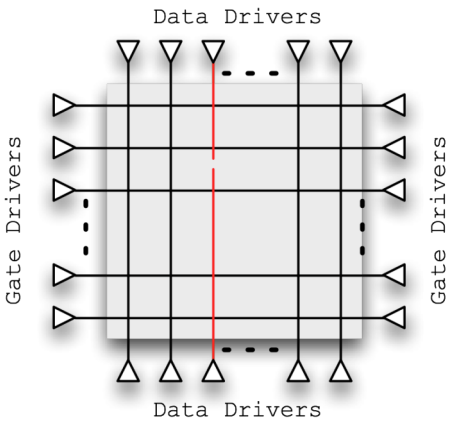

Figure 5 Wire open tolerant TFT array.

In [Kim95] and [Kim96], a dual gate line pixel design is proposed to tolerate gate line opens. In Figure 6 (a) and (b) are the single and double gate line pixels, respectively. This approach can tolerate all single gate line opens. To fix shorts between gate and

data lines, the gate line is cut at both sides of the defect.

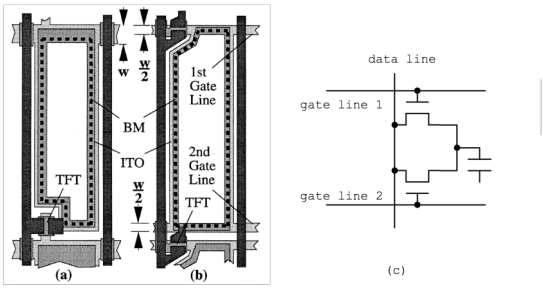

Figure 6 Dual gate line pixel design.

In [Kunii95] a double LDD TFT pixel is proposed to tolerate the common TFT leakage problem. As shown in Figure 7, the data line is connected to the pixel capacitor via two serially connected TFT devices driven by the same gate line. This pixel design can tolerate almost all defects related to TFT leakage.

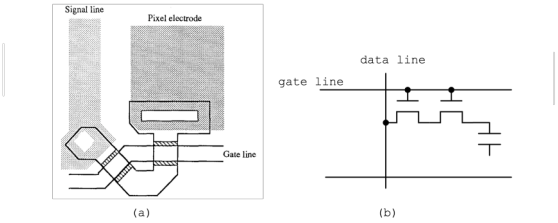

Figure 7 Double LDD pixel design.

六、研究方法

In the first year of this three-year project, the research items include survey of TFT array defect mechanisms and development of TFT array self-testing techniques.

1. Defect mechanisms
   In addition to the commonly used wire and pixel defect mechanisms, we will also study the stress-induced defects. A fault simulator will then be developed to evaluate the fault coverage of specific test items.
2. Self-testing techniques
   The goal is to realize the on-panel charge-sensing capability. To reach this end, we will first integrate the charge sensing capability into the data driver buffers. Than, an analog test bus will be developed so as to reduce the required self-testing circuits. Finally, on-panel ADC will be investigated to further reduce the ATE performance requirement.

七、結果與討論

We have developed a charge sensing capable buffer design. These buffers can also be connected to form an analog test bus to deliver the measurement results to a single output port.

A. The built-in charge sensing architecture

Figure 8 depicts the overall charge sensing architecture. It consists of the charge sensing capable buffers and the serial voltage readout circuitry. Both reuse the offset compensated analog buffers inside the source drivers.

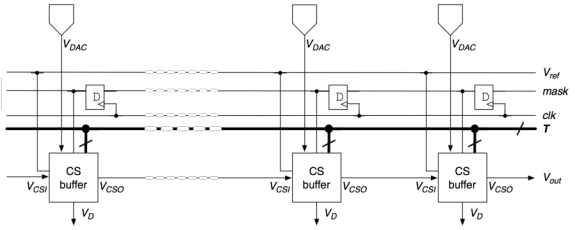

Figure 8 The charge sensing architecture.

The proposed charge sensing architecture allows three operation modes: the functional mode, the charge sensing mode, and the serial readout mode. In the functional mode, the CS-buffers act the same an offset compensated buffer. In the charge sensing mode, the CS-buffers perform the charge-to-voltage conversion. Finally, the serial readout mode supports serial readout of the charge sensing results.

The signals in Figure 8 are described below.

1. *T* is the CS-buffer control signal bus which is shared among all the CS-buffers.
2. V_{ref} is an analog bus shared among all the CS-buffers. Via this port,

the external tester supplies the test voltage and the charge sensing base voltage V_{base}.

3. To support serial voltage readout, the CS-buffers must be divided into two groups that are configured differently. The *mask* signal is used to differentiate between these two groups. A D-type flip-flop (DFF) is added to each CS-buffer to store its own copy of mask value. The DFFs are connected as a shift register, and the desired mask values are delivered to the CS-buffers via the shift operation.
4. The V_{out} port is the analog readout port where the charge sensing results can be measured by external testers. To speed up the readout process, one may utilize multiple readout ports.
5. The CS-buffers are concatenated by connecting the V_{CSO} port of each CS-buffer to the V_{CSI} port of the CS-buffer at its right-hand side. V_{CSO} of the last CS-buffer is then connected to the array's V_{out} port.

B. The charge-sensing buffer design

The proposed charge sensing capable buffer is illustrated in Figure 9. Compared to the offset compensated analog buffer in [Ker2006], four more switches are added. Among the switches, S_1 to S_6 facilitate the functional mode and charge sensing mode operations; the S_7 switch, on the other hand, is activated only during the serial readout mode.

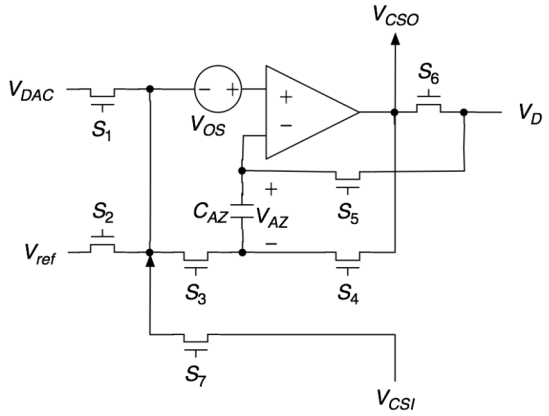

Figure 9 The proposed charge sensing capable buffer.

	functional		charge sensing			serial read out		
	AZ	WP	CWP	WDL	CTV	HV	RAZ	UB
S_1	1	1	0	0	0	0	0	0
S_2	0	0	1	1	1	1	0	0
S_3	1	0	0	1	0	0	1	0
S_4	0	1	1	0	1	1	0	1
S_5	1	0	0	1	1	0	1	0
S_6	1	1	1	1	0	0	1	0
S_7	0	0	0	0	0	0	1	1

Table 1 Control Signal Summary

The control signal values in different operations configurations are summarized in Table 1.

1. In the functional mode, the two configurations are auto-zero (AZ) and write-pixel (WP).
2. In the charge sensing mode, the CS-buffer performs the following operations: charge-sensing-write pixel (CWP), write-data-line (WDL), and charge-to-voltage (CTV). A complete charge sensing operation involves four configurations in the following order:

   AZ => CWP => WDL => CTV
3. The basic idea of the serial readout operation is depicted in Figure 10. After the charge-to-voltage operation, the voltage is available at each CS-buffer's opamp output terminal. The output voltage V_1

can be directly read out from the V_{out} port. To read out V_2, we configure the first CS-buffer as a unit buffer and let its input be from the V_{CSI} terminal. This way, V_2 is made available at the V_{out} port for measurement. Note that offset compensation must be performed to compensate for the opamp offset voltage. Similarly, to read out V_3, we configure the first and second CS-buffers as unit buffers. To summarize, to transfer a CS-buffer's charge sensing result to V_{out}, all the CS-buffers between it and V_{out} are configured as unit buffers.

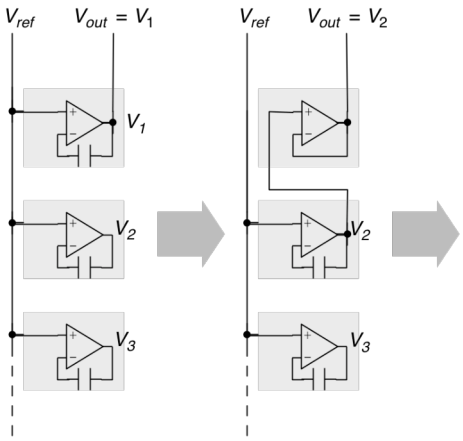

Figure 10 The serial voltage readout scheme.

To validate the proposed technique, Verilog-A simulation has been performed using the setup listed in Table 2, and the simulation results are shown in Figure 11. The simulation results agree with the theoretical analysis.

parameter	value	comments
C_{DL}	500 fF	data line capacitance
C_{pix}	700 fF	pixel capacitance
C_{AZ}	700 fF	auto-zero capacitance
V_{OS}	-1.5 V	opamp offset voltage
G_{OP}	150 V/V	opamp DC gain

Table 2 Simulation Setup

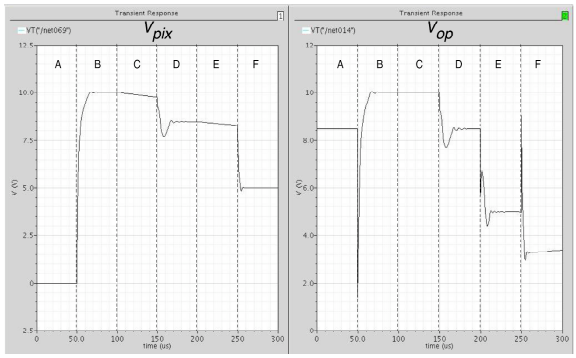

Figure 11 The simulation waveform

In summary, we have presented (1) a built-in charge sensing technique to enable on-panel charge sensing testing, and (2) a serial voltage readout scheme to output the charge sensing results via a single analog port. Both reuse the offset compensated analog buffer to reduce area overhead. We are currently implementing a prototype design for further validation of the proposed technique.

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出席國際學術會議心得報告

計畫編號	NSC95-2220-E-002-021-
計畫名稱	子計畫五：適用於軟性顯示器TFT陣列的缺陷容忍技術之開發(1/3)
出國人員姓名 服務機關及職稱	黃俊郎 / 助理教授 / 台大電子所
會議時間地點	2007/11/20 ~ 2007/11/23 日本福岡
會議名稱	亞洲測試會議 / Asian Test Symposium
發表論文題目	A Random Jitter Extraction Technique in the Presence of Sinusoidal Jitter

一、參加會議經過

搭乘20日早上的飛機，大約中午時抵達福岡國際機場。搭乘地鐵加上約二十分鐘的路程到達位於會場斜對面的下榻旅館。

議程第一天的keynote的演講者為Advantest America的P. D. Roddy。以ATE vendor的角度提出未來full wafer tester與design-verification tester的重要性與發展趨勢。 下午的social event為sumo，地主國的教授很熱心的為我們講解比賽的一些傳統與細節。議程第二天的keynote的演講者為I. Pomeranz。講題為low power相關議題。下午報告所發表的論文。第三天只有早上有technical sessions，搭乘中午的班機回國。

二、與會心得

今年的ATS投稿接受率約為50%（63/127）。大陸、歐洲與北美的被接受率分別為24%（5/21）、45%（9/20）與61%（20/33），而台灣的被接收率約為59%(10/17)，高於平均值，表現相當不錯。

今年參加的session主要為類比與高速界面的測試。在ADC/DAC的測試方面，使用loopback或低解析度的測試信號以降低對測試儀器的需求已成為最近的主流。在jitter的測試方面，使用loopback也是如Intel等大廠的解決方案。整體看來，把重要而且需要校正的測試用電路放在load board上的built-off test是一個比built-in self-test更可以被接受的解決方案。

A Random Jitter Extraction Technique in the Presence of Sinusoidal Jitter

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Abstract

In this paper, a random jitter (RJ) extraction technique in the presence of sinusoidal jitter (SJ) is proposed for on-chip jitter tolerance testing applications. First, the period-tracking technique [4] is utilized to derive the SJ frequency and amplitude information. Then, using the same design-for-test (DfT) circuitry, samples from the total jitter cumulative distribution function (CDF) are taken. From the SJ information and CDF samples, a binary search method is utilized to obtain the RJ sigma value. The features of the proposed technique include low delay line resolution requirement and high process variation tolerance. Simulation results are performed and shown to validate the proposed technique.

Keywords—sinusoidal jitter, random jitter, jitter decomposition, jitter tolerance, design-for-test, built-in self-test.

1 Introduction

For high-speed serial link (HSL) systems, one of the factors that determine the overall quality is jitter which is the deviation in a signal's edge transitions from their ideal positions. Among the various jitter-related performance requirement, the jitter tolerance specification is defined as the jitter amplitude in UI (unit interval) versus jitter frequency. To confirm that the device under test (DUT) meets the minimum or lower limit of the jitter tolerance requirement, a sweep of the jitter mask is applied at the DUT input while checking there are no bit errors at the output.

To reduce the cost associated with jitter tolerance testing, a DfT architecture is proposed and shown in Figure 1. The DfT circuitry consists of the jitter Tx and the SJ/RJ extraction circuit. The former performs phase modulation (with v_{mod} as the modulating signal) on the bit stream (from the regular serializer)—by adjusting the frequency and amplitude of v_{mod}, the desired sinusoidal jitter can be injected to the bit stream. The jitter transmitter output may then be utilized to perform jitter tolerance test on the the de-serializer of the same chip (via internal or external loopback) or another chip. However, process variations and other non-ideal factors could affect the jitter transmitter performance, e.g.,

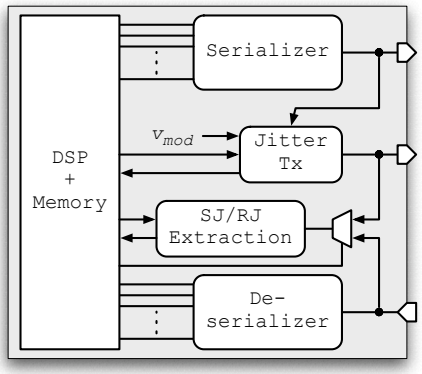

Figure 1. A SerDes DfT scheme.

RJ components and deviations in SJ amplitude. In [4], an SJ extraction technique is reported which can characterize the SJ amplitude and frequency in the existence of RJ components. In this paper, we are interested in characterizing the RJ components after the SJ information is available.

Several techniques to separate RJ in the presence of deterministic jitter components have been proposed in the past. In [13], a pattern marker is used as as the measurement reference to derive DCD and ISI from the mean edge transition locations. PJ and RJ, on the other hand, are calculated through spectral analysis of the edge locations. In [5], an RJ extraction technique via tail fitting is proposed. With RJ probability density function (PDF) and the total jitter PDF available, the DJ extraction technique in [10] utilizes deconvolution to derive the DJ PDF. In [17], the authors present the $\Delta\phi$ method to derive the instantaneous phase error of the signal under test. From the instantaneous phase error, all desired jitter characteristics can be derived. In [16, 18, 14], extensions to the $\Delta\phi$ method are proposed for high-speed applications. In [15], the authors propose a real-time jitter measurement board which converts the instantaneous jitter information into an analog voltage waveform. After digitizing the analog waveform, DSP techniques are applied to derive the desired jitter characteristics. In [3], an on-chip version of the technique is fabricated and verified. The technique in [6] utilizes on-chip single-shot time measurement unit to measure the signal periods. Sample time estimation, period estimation, and

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FFT are then applied to the sequence of measured periods to derive the SJ amplitude and frequency. In [8] and [7], the technique is extented to handle ultra high-speed signals and extract RJ components. In [12], a random jitter test technique is proposed. The technique has very low self-jitter, but requires a high-quality sampling clock. In [1], a fast comparator sampling technique for random jitter extraction is proposed. To make accurate measurements, it is critical that the effective sampling resolution be a fraction of the jitter's standard deviation.

In this paper, a DfT technique for RJ component extraction in the existence of SJ is proposed for jitter tolerance testing applications. Previously, we have presented a period-tracking technique [4] which extracts the amplitude and frequency information of SJ components. The proposed RJ extraction technique utilizes the same core DfT circuitry, including a variable delay line and a phase comparator, to sample the jitter's CDF. Based on the SJ information and the CDF samples, a binary search algorithm is employed to derive the RJ sigma.

The main advantage of the proposed technique is low DfT circuitry complexity and accuracy requirement. In the proposed technique, the more sensitive part of the DfT circuitry includes the variable delay line and the phase comparator which digitize the desired jitter information. Relying on a simple delay line calibration technique, the post-processing algorithm can tolerate the offset and nonlinearity associated with the delay line. Furthermore, the delay line resolution does not have to be a fraction of the RJ sigma, which makes the proposed technique promising for high-speed applications. The low resolution requirement also reduces the number of delay taps which lowers both the hardware complexity and the test time. Numerical simulations have been conducted to validate the proposed technique. For a wide range of RJ sigma, the proposed technique yields accurate results.

The paper is organized as follows. In Sec. 2, related background is briefly reviewed. The proposed technique is then illustrated in Sec. 3. Simulation results are presented in Sec. 4 and we conclude this work in Sec. 5.

2 Preliminaries

Depending on the applications, jitter may be interpreted in different ways, e.g., period jitter, cycle-to-cycle jitter, and time interval error (TIE). Among the different views, period jitter measurement is the most direct because it does not require any external reference. Therefore, the proposed RJ extraction technique extracts the period jitter information.

2.1 Period comparison

Although period jitter measurement is more direct, complex TMU is still needed to measure the cycle length. Instead of using a full-blown TMU, the proposed technique utilizes a simple one-bit period comparator to determine whether the length of a cycle is greater than a delay value or not.

The block diagram of the period comparator is shown in Fig. 2(a). Consisting of a variable delay line and a phase comparator, it was previously adopted by [11, 2, 15, 3]. The phase comparator determines the phase relationship (lead or lag) between the rising edges of SUT (the signal under test) and SUT' (the delayed SUT). Let A and B be two consecutive rising edges on SUT, and A' the rising edge on SUT' that corresponds to A. If the delay line value τ is less than the current cycle length T_{AB} as shown in Fig. 2(b), B will lag A' and the phase comparator's lag output is one; otherwise, the $lead$ output is one. The period comparator can be viewed as a high-throughput one-bit time digitizer.

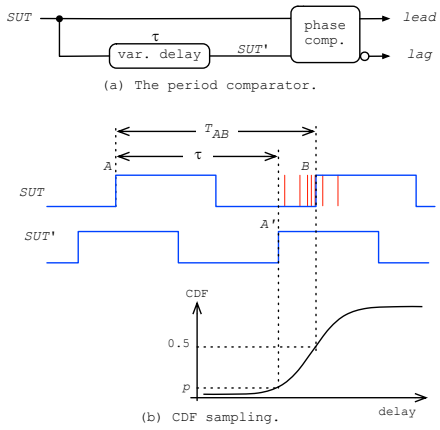

Figure 2. The period comparator (a) and CDF sampling (b).

2.2 Jitter CDF sampling [11, 2]

In the proposed technique, the period comparator is employed to sample the jitter CDF. The idea is depicted in Fig. 2(b). If SUT is jitter free, the phase comparator's output should be constant depending on the delay line value and the cycle length. However, due to jitter, the position of B will deviate from its ideal position; as a result, the period comparator output is no longer constant. If one performs a sufficiently large number of period comparisons, the probability p that the $lead$ output equals one is the probability that SUT's cycle length is less that the delay value and corresponds to a sample of the jitter CDF as shown in Fig. 2(b). More CDF samples can be obtained by varying the delay line value.

3 The RJ sigma extraction technique

The proposed RJ sigma extraction technique can be applied to both clock and bit-stream signals. For the latter, the $\cdots 010101 \cdots$ sequence is used as the data pattern. This way, the ISI and DCD components have no effect on the extraction results.

3.1 The basic idea

To better illustrate the idea of the proposed technique, let's consider the simplified case when only the RJ component is present. In Fig. 3, the solid curve is the CDF of SUT's RJ component. Assuming that two delay values d_1 and d_2 are utilized for CDF sampling, the information available for RJ sigma derivation then includes (1) p_1 and p_2, the CDF values of d_1 and d_2 respectively, and (2) Δd, the difference between d_1 and d_2. Note that d_1 and d_2 are derived using the oscillation approach. Because the incurred offset is unknown, only Δd is utilized for RJ sigma extraction.

From Fig. 3, one can observe that, with the same p_1 and p_2, Δd increases monotonically with jitter sigma—it is smaller/larger for the steeper/gentler dashed curve which corresponds to a smaller/larger sigma. (In fact, Δd is proportional to sigma in this example.) For ease of explanation, let Δd^0 be the actual delay difference and $\Delta d\,(\sigma)$ be the Δd value if the RJ sigma value is σ. Then, jitter sigma estimation can be achieved by identifying σ such that $\Delta d\,(\sigma) = \Delta d^0$.

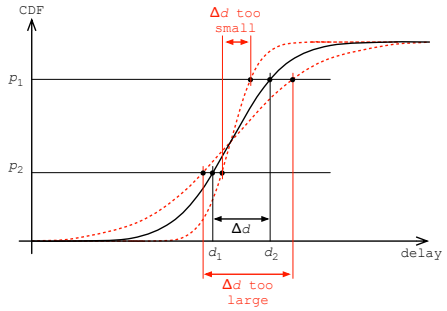

Figure 3. The basic idea.

However, RJ sigma estimation via Δd^0 matching is more complicated in the existence of SJ components because the monotonicity relationship may not exist. Thus, as will be shown later, more than two delay values are used for CDF sampling, and a pair of delay values is utilized to derive the RJ sigma only if it satisfies certain selection criteria.

3.2 Inputs of the RJ extraction algorithm

As shown in Fig. 4, the inputs to the jitter extraction algorithm include:

Delay line values: The oscillation-based approach is utilized to measure the delay line values [9]. Note that the measurement results contain a DC offset inherent in the oscillation method.

SJ amplitude: The SJ amplitude is obtained from the SJ extraction technique. A piecewise linear approximation of the SJ PDF is derived from the SJ amplitude.

CDF samples: Using the period comparator, the CDF value with respect to each delay tap of the variable delay line is obtained.

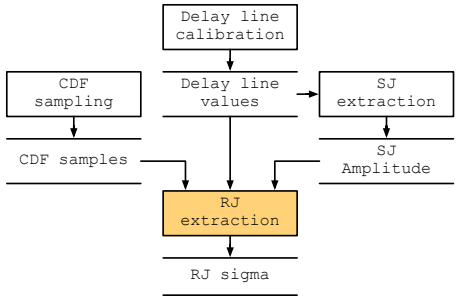

Figure 4. RJ extraction algorithm inputs.

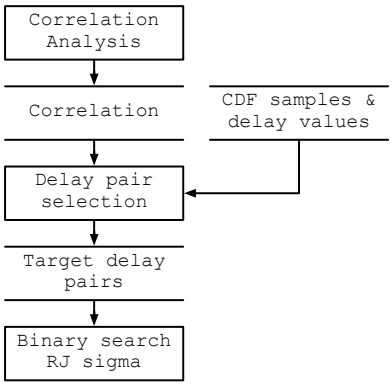

Figure 5. The RJ extraction algorithm flow.

3.3 The RJ extraction algorithm flow

The overall RJ extraction algorithm flow is shown in Fig. 5. It consists of the "correlation analysis", "delay pair selection", and "binary search RJ sigma" phases.

Correlation analysis: In this phase, the correlation between Δd (of a pair of p_i's) and RJ sigma is computed. In our technique, the derived correlation is used as one of the criteria for delay pair selection. Note that the correlations only have to be computed once, and the results are saved in a two-dimensional table $\mathcal{R}$.

Delay pair selection: For each pair of delay lines d_i and d_j, their corresponding CDF values p_i and p_j are used to look up the correlation table $\mathcal{R}$ nd obtain the Δd vs. RJ sigma correlation. A pair of delay lines will be utilized for RJ sigma estimation if the following conditions are satisfied.

$$\mathcal{R}\,(p_i, p_j) \geq r_{th} \quad (1)$$

$$0.003 \leq p_i \leq 0.997 \quad (2)$$

$$0.003 \leq p_j \leq 0.997 \quad (3)$$

Binary search RJ sigma: In this phase, a binary search method is utilized to search for the RJ sigma such that the actual and derived sums of delay differences coincide.

3.4 Delay pair selection

Although the idea discussed in Sec. 3.1 works for RJ only cases, direct application of the idea in the existence of

SJ components does not guarantee to yield correct results. The main problem is that, with SJ, the relationship between Δd and RJ sigma is not necessarily monotonic.

The proposed algorithm utilizes correlation instead of monotonicity as the delay pair selection criterion, and use multiple delay pairs for RJ sigma estimation due to the following reasons.

1. Non-monotonicity is not a problem if the RJ sigma estimation can somehow be brought close enough to the actual value. Using monotonicity as the sole criterion may miss delay pairs that are highly correlated with and sensitive to RJ sigma in the vicinity of the actual RJ sigma.

2. Using multiple delay pairs help lower the negative impact of the finite sample size. In practice only finite period comparisons are made due to the test time and test cost limitations. As a result, the obtained p_i's are only approximations and the error is Gaussian. Using multiple delay pairs helps average out the CDF sampling errors.

3. Based on the above analysis, the correlation between Δd and RJ sigma is used as the delay pair selection criterion. It may be viewed as a less stringent but more global requirement on monotonicity. Thus, a delay pair is selected for RJ sigma estimation if its Δd vs. RJ sigma correlation is greater than the specified threshold r_{th} which is set to be 0.9.

In addition to the Δd vs. RJ correlation, another selection criterion is that p_i and p_j have to be within $[0.03, 0.997]$ because CDF values beyond this range correspond to rather few samples in the combined jitter distribution of SJ and RJ and thus are less accurate.

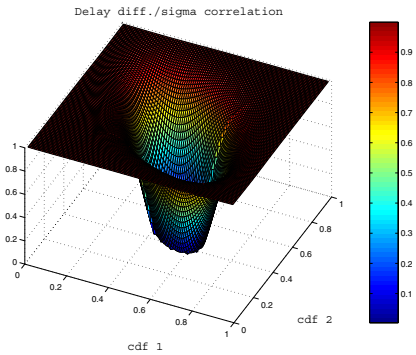

Figure 6. Δd vs. RJ sigma correlation.

3.5 Correlation analysis

To derive the correlation table $\mathcal{R}$, a set of uniformly distributed CDF pairs are generated according to the desired correlation table resolution. Then, for each pair of CDF values, Δd is computed for a set of uniformly distributed RJ sigma values. The corresponding Δd vs. RJ sigma correlation is then derived. Since there is no closed form expression for the combined CDF of RJ and SJ, a piecewise linear estimation is constructed and utilized to derive the delay value with respect to a given CDF value.

Prior to constructing the correlation table, the piecewise linear approximation of the normalized SJ PDF, i.e., SJ amplitude equals one, is generated. Then, the procedure of computing Δd of a CDF value pair (p_i, p_j) with respect to a given RJ sigma is as follows.

1. Derive the piecewise linear approximation of the Gaussian PDF with respect to the given RJ sigma.

2. Derive the combined PDF of RJ and SJ by performing convolution on the normalized SJ PDF and the RJ PDF obtained in step 1.

3. Derive the combined CDF of RJ and SJ from the PDF obtained in step 2.

4. Using the CDF obtained in step 3 to find x_i and x_j such that the corresponding CDF values are p_i and p_j, respectively.

5. $\Delta d = x_i - x_j$.

Note that only one table has to be built, i.e., for the normalized SJ. Δd obtained from the table is normalized to the SJ amplitude.

Fig. 6 shows the correlation analysis results. In this figure, the x and y-axis are CDF values ranging from 0 to 1 and the z-axis is the computed Δd to RJ sigma correlation. For a fairly large portion of CDF pairs, the correlation is close to one.

3.6 Binary search RJ sigma

Let $\Theta = \{\theta_1, \theta_2, \ldots, \theta_n\}$ be the set of n delay pairs that have been selected for RJ sigma estimation. The actual and derived sums of delay differences are denoted by

$$\Delta D^0 = \sum_{i=1}^{n} \left|\Delta d^0(\theta_i)\right| \quad (4)$$

$$\Delta D(\sigma) = \sum_{i=1}^{n} \left|\Delta d(\theta_i, \sigma)\right| \quad (5)$$

where the subscript 0 represents the measured values. The goal the RJ estimation is then to find σ such that

$$\Delta D^0 - \Delta D(\sigma) = 0 \quad (6)$$

In the proposed technique, a binary search method is utilized to identify σ.

It should be noted that

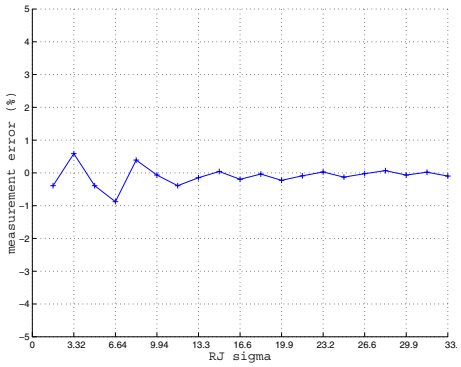

Figure 7. Errors w.r.t. different RJ sigma.

- ΔD^0 is derived directly from the delay line calibration results. The offset associated with the measured delay values is cancelled out and has no effect on ΔD^0.

- To derive $\Delta D\,(\sigma)$, the same procedure as the correlation analysis phase is used to derive the estimated delay difference of each delay pair with respect to the given σ.

4 Simulation results

Numerical simulations are performed to validate the proposed idea. The simulation setup is as follows:

- The signal frequency is set to be 3 GHz which corresponds to a period about 333 ps.

- The number of phase comparisons per CDF sampling is $N = 2^{20}$.

- The SJ amplitude is set to 33.2 ps.

- The delay line resolution is 16.6 ps, and the minimum and maximum delay line values are $333 - (33.2 \times 2)$ and $333 + (33.2 \times 2)$ ps, respectively. For small RJ sigma, the specified delay line resolution is rather coarse.

- To simulate the effects of process variations, the same random offset is added to all delay taps and individual random variation is added to each delay tap. The maximum value of both are set to be 10% of the delay line resolution.

4.1 RJ estimation results

Using the above setup, the measurement error percentage is plotted in Fig. 7 for RJ sigma that ranges from 1.66 to 33.2 ps. For this setup, the measurement errors are less than 1%. In addition, a trend of growing error percentage with respect to decreasing RJ sigma is also observed in the plot.

4.2 Further analyses

To gain further insight into the proposed technique, experiments with modified simulation parameters are performed and the results are listed in Table 1.

1. In the first experiment, the delay span, i.e., the difference of the maximum and the minium delay values, is reduced by half to be 2 times SJ amplitude (66.4 ps), and the delay line resolution is two times the RJ sigma (6.64 ps). Accurate estimation of RJ sigma is obtained.

2. A large RJ sigma value is assigned. RJ sigma estimation cannot proceed in the case because no delay pair satisfies the selection criterion.

3. The setup is similar to case 2 but with a larger delay span. This setup is unstable. Sometimes, due to delay line offset, no delay line pair is selected and no estimation is made. However, if the delay pair set is non-empty, the estimation result is quite accurate.

4. The SJ sigma is small and the delay span is reduced. This is also an unstable setup. The error is either around -4% or -90%. Note that this case is just for the purpose of verifying the algorithm's stability—implementation of the required delay line resolution is impractical.

5. The sigma is small but the delay span is normal. This setup is stable and yields an error of about 2.5%. Similar to the previous case, this setup only serves to validate the algorithm stability.

From the simulation results, the proposed technique performs the best for RJ sigma ranging from 10% to 100% of the SJ amplitude. Within this range, it is rather tolerant to delay line span and delay line variations. Beyond this range, however, more stringent requirement on on the delay span and the delay resolution is required to yield stable and accurate results.

4.3 Discussion

The main advantage of the proposed technique is low hardware complexity and high process tolerance. As we have shown, the variable delay line in the period comparator does not have to be linear and its resolution does not have to be a fraction of the RJ sigma. Thus, the required number of delay taps can be reduced and process variation is better tolerated.

However, there are still some issues remained to be solved. First, the DfT circuitry induced jitter will certainly affect the RJ estimation results and must be taken into account. Enhancement of the algorithm's stability for lower-end RJ sigma is also important as the serial link data rate continues growing. The process of deriving $\Delta d\,(\theta_i, \sigma)$ is

Table 1. Case studies for modified simulation setup.

	RJ sigma	delay span	delay res.	error (%)	comment
1	3.32	66.4	6.64	0.59	low sigma, low delay span, coarse delay line
2	39.84	66.4	79.68	NA	sigma too large, no delay pair selected
3	39.84	132.8	79.68	-0.31*	large sigma, normal delay span
4	1.66	66.4	1.66	-4.29*	low sigma, reduced delay span
5	0.664	132.8	0.664	2.54	low sigma, normal delay span

*: unstable

currently the most time consuming part. We will investigate more efficient and accurate methods.

5 Conclusion

In this paper, an RJ extraction technique in the existence of SJ components is proposed. To be a viable on-chip solution, the DfT circuitry is simple and does not have to be very accurate. Simulations show that the RJ sigma estimation algorithm returns quite accurate results for a wide range of RJ sigma. We will investigate techniques to enhance the accuracy for low RJ sigma values and to improve the computation efficiency.

Acknowledgement

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