# An Accurate Time-Domain Current Waveform Simulator for VLSI Circuits

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## Abstract

*A new charge-based current model for CMOS gates is presented in this paper. The current during a transition consists of three components : one occurs when the input changes and the others exist only when the output changes. So, this model can generate current waveform with negative values, like SPICE. These three components are characterized by triangular functions with four parameters which can be easily obtained after timing simulation. When comparing the results obtained by using SPICE with those by our model, we find agreement, especially on the time points at which maximum current occurs.*

## 1 Introduction

In large integrated circuits, current flow in power and ground buses leads to the problems of voltage drop and metal migration, which are the major reliability problems. The problems are especially important in the widely used CMOS technology, where switching transients from different parts of a circuit can occur almost simultaneously and thus, may generate large noise spikes (in the form of voltage drops) in the power/ground buses. Unrestricted voltage drops in the P/G buses may result in incorrect logic operation and degradation in switching speed. Restricting voltage drops to safe limits requires the knowledge of peak current in the P/G buses. A time-domain current waveform simulation is proposed in [1], where the current is approximated by an isosceles triangular current pulse. This model can achieve great accuracy when the load of each gate is small. Since the current pulse is asymmetric when the load is large, so this model will result in large errors. Also because of the asymmetry, the peak current obtained by this model will deviate from the real peak current, so the peak value of the total current supported by the power bus is not correct. We adopt another approach in [2] which is more complex, but it can give accurate results even when the load is very large. After analyzing the possible transition of a gate, the current waveform under one input vector excitation can be obtained with only four parameters.

No matter which model is used in previous works, simulation or estimation, only the current flowing during the rising and falling edges of the output signals of CMOS gates is considered. After developing the first current model [2], we find that large errors still exist in some large circuits. The primary reason is the neglect of the current flowing across the gate capacitance of CMOS gates. Currents flow across these gate capacitors when the input signals change, whether the gate changes state or not. So we develop another current model which takes this current into account. In this model, we decompose the total current supported by the $V_{DD}$ bus into three components. We try to calculate the individual charge for each of these three components, and then the total current is obtained.

## 2 Current Model

There are many parasitic capacitors existing inside a CMOS gate, e.g. $C_{gs}$. So there will be current flowing if the voltage drop of any two terminals of a MOS transistor changes. We assume that current flows only when the inputs of the gate change. This means that leakage currents are neglected. The current drawn from the $V_{DD}$ bus consists of three components : (1) gate capacitor differential current, (2) load capacitor charging current, and (3) short-circuit current. The last two components exist only when the output of the gate changes state. Let us consider the circuit shown in Fig.1(a). Let $B$ be HIGH, then this NOR gate will not change state no matter which state $A$ is in. When the input of the inverter increases from 0V to 5V, the voltage of node $A$ will decrease. We can find one current component in the NOR gate, t-



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wo current components in the first inverter, and three current components in the second inverter, as shown in Fig.1(b). All researchers [1,2,5-7] focus attention on the charging/discharging current and short-circuit current of CMOS gate, so only the currents $I_{13}$ and $I_{32}+I_{33}$ are considered. But owing to the change of the voltage drop across the gate capacito, there are currents $I_2$ and $I_{31}$ flowing from $V_{DD}$ to node $A$ across the gate capacitors, and $I_{11}$ flowing to $V_{DD}$ across the gate capacitor of the inverter gate. Notice that $I_1$ decreases and then increases due to the existness of $I_{13}$. So there will be large error if neglecting this current. Each current waveform can be represented as a triangle with four parameters ($T_s$, $T_p$, $T_e$ and $Q$), as shown in Fig.2. $Q$ is the total charge transferred to/from the $V_{DD}$ bus and is equal to the area of this triangle. These three time parameters designate the time when the current waveform begins, reaches its peak value and stops changing. We try to calculate the charge transferred and determine the values of these three time parameters from the voltage waveforms, then each current waveform can be obtained. After we sum each current waveforms up, the total current is obtained.

## 2.1 Capacitor Differential Current

To simplify the calculation, the currents flowing to/from $V_{DD}$ are considered only, though there are many parasitic capacitances existing inside the CMOS gate. This current can be calculated as $\frac{dCV}{dt}$. When the input increases(decreases), the current flows into(from) the $V_{DD}$ bus. Since $C_{gs}$ and $C_{gb}$ are input-dependent and nonlinear, so the total charge transferred due to this current can be calculated as :

$$Q = \int_{V_{DD}-V_s}^{V_{DD}-V_e} C(V) \cdot dV = C_{eff} \cdot (V_s - V_e), \quad (1)$$

where $V_s$ and $V_e$ are the initial and final values of the input during this transition, respectively. Its value is determined by the total capacitance considered, no matter how fast the input changes. If the source of the MOS is connected to $V_{DD}$, e.g. $M_1$, the capacitance is $C_{gs}+C_{gb}$. If the source of the MOS is not connected to $V_{DD}$ directly, e.g. $M_2$, then the capacitance is either $C_{gb}+C_{gs}$ if there is a conducting path connecting the source of this MOS to $V_{DD}$, or $C_{gb} + \frac{C_{gs}}{1+k}$ if no conducting path to $V_{DD}$, where $k$ is equal to $\frac{C_{gs}}{C_{sb}}$. So it is determined during the simulation process that how many parasitic capacitances needed considering. These capacitances are functions of the design parameters ($L$, $W$, ...), and these values can be measured using SPICE previously . If $V_s$ is smaller than $V_e$, $Q$ is negative and it means that the differential current flows into the $V_{DD}$ bus. This current is labeled as $I_1$ shown in Fig.2. Since this current is due to the change of the input, the values of $T_{s1}$ and $T_{e1}$ are set as the time when the input signal begins and stops changing respectively, as shown in this figure. The peak current occurs when the voltage slope of the input is at its maximum. So $T_{p1}$ is the time when the input is 2.5V approximately.

## 2.2 Capacitor Charging Current

Fig.3(a) shows the generic CMOS gate structure used in many literatures [6]. The output node capacitance is split into two lumped capacitors, $C_p$ and $C_n$. Only $i_{p1}$ and $i_{n1}$ are considered [6]. The primary problem in this model is how to split parasitic capacitors into $C_n$ and $C_p$? Not all capacitances are connected directly to $V_{DD}$ or $GND$, so the value of $C_p$ and $C_n$ is time-variant. Since the total charge transferred to the load during the transition is $V_{DD} \cdot C_{load}$, the point is how to calculate the load capacitance accurately. We use the circuit shown in Fig.3(b) to measure the input capacitance of a CMOS gate. We try to adjust the value of $C_{adj}$ to make voltage waveform $V_1$ coincide with $V_2$ and make $i_1 \approx i_2$, and then the input capacitance of the test gate at this input terminal is set to $C_{adj}$. The input capacitance is a function of the design parameters($L, W, \ldots$), and its value seems to be independent of what type of gate is. So the total charge transferred can be calculated as

$$Q = V_{DD} \cdot \sum C_{in}. \quad (2)$$

This current is labeled as $I_2$ shown in Fig.2. Since this current is due to the change of the output voltage, the values of $T_{s2}$ and $T_{e2}$ are set as the time when the output voltage begins and stops changing respectively. The peak current occurs when the voltage slope of the output is at its maximum. So $T_{p2}$ is the time when the output voltage is 2.5V approximately.

We want to find the total current supported by the $V_{DD}$ bus, so we are interested in the current on the low-to-high transition. Of course, the current will be larger than $i_{p1}$ or $i_{n1}$, as shown in Fig.3(a). But since $C_p$ is the gate capacitance at the next stage, there will be a capacitance-differential current flowing to $V_{DD}$. So the over-estimated current will be subtracted when we process the next stage. On the other hand, the current will be under-estimated on the high-to-low transition owing to our neglecting the discharging current. But because $C_n$ is the gate capacitance at the next stage, there will be a capacitance-differential current flowing from $V_{DD}$. So the under-estimated current will be also complemented.

## 2.3 Short-Circuit Current

During a transient on the input, there is a time period in which both the N-block and the P-block conduct, causing a current to flow from $V_{DD}$ to ground. This current flows as long as the input voltage is higher than a $V_{tN}$ above GND and lower than a $V_{tP}$ below $V_{DD}$. It is very difficult to describe the short-circuit current precisely, and the analytical solution of this current can be obtained only when the gate is a C-MOS inverter gate under some assumptions. The total charge transferred due to this current can be obtained previously with SPICE as follows:

$$Q = \int_{t_{start}}^{t_{end}} I_{V_{DD}} \cdot dt - Q_{diff} - Q_{load}, \qquad (3)$$

where $t_{start}$ and $t_{end}$ are the time when the input begins to change and the output stops changing. $I_{V_{DD}}$ is the current drawn from the $V_{DD}$ bus. $Q_{diff}$ and $Q_{load}$ are the charge due to the differential and charging current, respectively. This charge is a function of the total effective resistances $R_P$ and $R_N$ and can be modeled as

$$Q = \frac{A}{R_P} + \frac{B}{R_N} + C, \qquad (4)$$

where $A$, $B$ and $C$ are the fitting parameters. $R_P$ and $R_N$ are the total effective resistances of the P- and N-block, respectively. After assigning the ON/OFF state to each MOS according the states of inputs, we can obtain $R_P$ and $R_N$, then the charge $Q$ is obtained. This current is labeled as $I_3$ shown in Fig.2. The values of $T_{s3}$ and $T_{e3}$ are set as the time when the voltage difference of the input and the output are 4V and -4V respectively with the assumption that $|V_{tp}| = |V_{tn}| = 1V$. $T_{p3}$ is the time that the input voltage and the output voltage are equal.

## 2.4 Glitch

The accuracy of the current simulation depends strongly on the voltage waveforms. The glitch may occur when two adjacent events are so close that the second event occurs before the first event finishes, as shown in Fig.4(a). Glitches may draw significant amounts of currents and should not be neglected. When calculating the current waveform resulting from the first event, we assume that this event can reach its final state, so that the whole current waveform can be obtained. But since the second event occurs before the first event finishes, so the current waveform is cut at the time the second event occurs, as shown in Fig.4(b). We approximate the current waveform resulting from the second event according to the peak ratio, $\frac{V_Z}{V_{DD}}$, where $V_Z$ is the voltage swing of the glitch.

# 3 Simulation

This current model has been embedded into our timing simulator BTS [3, 8]. BTS uses a recursive technique to calculate the delays in the series-parallel MOS circuits [4]. The results of BTS are accurate because BTS uses an accurate delay calculation method that computes the switching delays and slopes with the considerations of the effects of the internal charges [8]. Fig.2 shows the voltage and current waveforms at the second stage of a 3-stage inverter chain. When the timing simulation finishes, the event list at the output of each gate can be obtained. The input of this inverter begins to decrease at $2.25ns$ and its slope is $-7.14 \cdot 10^9 V/sec$. The output increases at $2.74\ ns$ and its slope is $8.62V/ns$. Since the input decreases, the current waveform consists of three components. The areas of these three components can be obtained using Eqn.(1), (2) and (4). These time parameters can be obtained from the voltage waveform as described in previous sections and their values are :

$$\begin{array}{lll} T_{s1} = 2.25ns & T_{p1} = 2.6ns & T_{e1} = 3.7ns \\ T_{s2} = 2.74ns & T_{p2} = 3.03ns & T_{e2} = 3.97ns \\ T_{s3} = 2.43ns & T_{p3} = 2.86ns & T_{e3} = 3.33ns \end{array}$$

The time-domain current waveform supported by the $V_{DD}$ bus is the summation of the current waveforms of each block. The current waveform of each block consists of a series of triangular pulses, and is represented as a current source to the $V_{DD}$ bus. Since the metal resistance is negligibly small within a subcircuit, we can combine several sources in a subcircuit into a single current source, which represents the power-bus current drawn by the subcircuit. Let the addition of a triangle to the waveform be a basic unit of calculation. And let $M$, $N$, and $K$ be the total event number of all blocks, the total event number of all primary inputs of this circuit, and the total event number of the primary outputs of this circuit, respectively. When we calculate the current waveforms, the number of the addition operation required are follows :

| | |
|---|---|
| $M - N$ | for capacitor differential current |
| $\frac{1}{2} \cdot (M - N - K)$ | for load capacitor current |
| $M - N$ | for short circuit current. |

So the total number of the addition is $\frac{5}{2}M - \frac{3}{2}(N+K)$. Because $M$, in general, is larger than $N+K$, the CPU-time overload of the current calculation to the timing simulation is strongly dependent on the event number, no matter how large the circuit.

## 4 Results and Conclusions

The simulator has been tested extensively for basic modules such as counters, decoders, adders and ALUs. The CPU time comparisons are summarized in Table 1. The CPU time consists of the time that the timing simulator BTS used and that the current calculation used on a SUN SPARC station 1+. Since BTS considers the effects of the internal charges, the simulator is not as fast as other timing simulators, but the waveforms it derives are more accurate. It is very important that the accuracy of the current waveform calculation is strongly coupled to the accuracy of the timing information. In Table 1, we list three more error values, DC, $Max\_I$ and $Max\_T$. DC error is the relative error between the average current $I_{avg.SPICE}$ and $I_{avg.BTS}$. $Max\_I$ is the relative error between the value of the peak current $I_{peak.SPICE}$ and $I_{peak.BTS}$. $Max\_T$ is the absolute error about the time that the peak current occurs. Fig.5 shows the current comparisons of an encoder SN74147 with SPICE's result. For the purpose of comparison, the current waveform is the summation of all the currents from individual subcircuits. If a circuit is implemented based on some restricted design styles, such as full complementary CMOS, Pseudo-NMOS, Dynamic CMOS, etc., the circuit can be simulated by using BTS and then the current waveform can be obtained. Fig.6 shows the voltage and current waveforms of a 4-bit carry-lookahead adder. The carry gate of this circuit is implemented as a domino CMOS gate.

A current model is presented which can be used to generate the time-domain transient current waveforms in the power bus lines. The simulated waveforms in general differ by no more than 10% from those simulated by SPICE. Its speed is $10^2 \sim 10^3$ times faster than that of SPICE for circuits with hundreds of transistors, and the speed ratio is expected to be even more significant for larger-scale circuits. At the cost of a little speed ratio, the results are more accurate, especially the time at which the peak current occurs.

Table 1 :Comparisons between BTS and SPICE3

| Ckt. | Error | | | CPU time(sec) | |
|---|---|---|---|---|---|
| | DC | $MaxI$ | $MaxT$ | BTS | SPICE |
| 74381 | 0.56% | -8.52% | -8.2e-11 | 1.48 | 1478.7 |
| 7483 | -1.71% | -4.15% | -6.4e-13 | 1.38 | 282.37 |
| 74147 | 1.78% | 5.76% | 7.0e-10 | 1.11 | 121.55 |
| Inv | 2.2% | -7.43% | -4.2e-12 | 0.70 | 100.7 |

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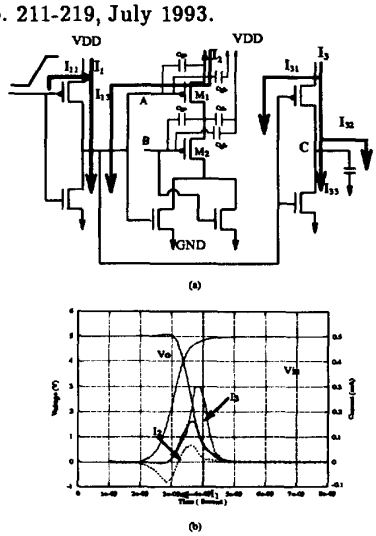


Figure 1: (a) A 3-stage CMOS circuit and (b) the voltage and current waveforms obtained by using SPICE.

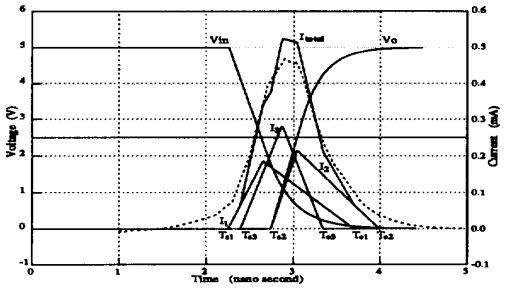


Figure 2: Each current waveform is modeled as a triangle, $I_1$, $I_2$ or $I_3$. $I_{total}$ is the summation of these current triangles. The dashed line is obtained using SPICE.

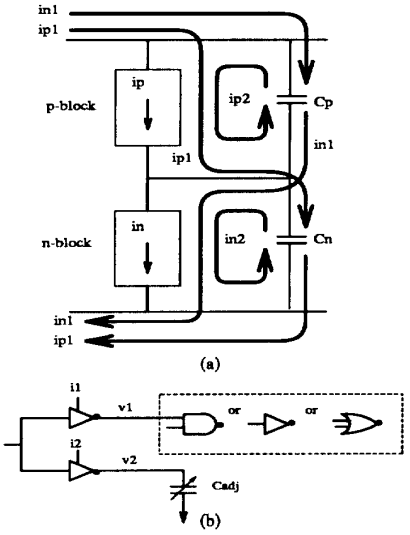


Figure 3: (a) A generic CMOS gate and (b) the method used to measure the input capacitance of C-MOS gate.

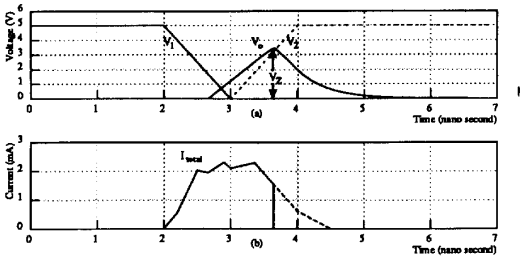


Figure 4: Voltage waveforms with glitch. (a) the voltage waveforms of an two-input NOR gate and (b) the waveform of the total current. Since the second event occurs, so the dashed tail is cut.

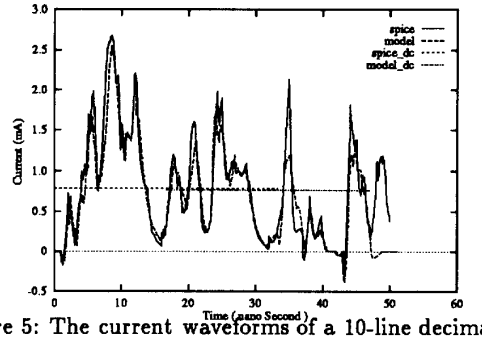


Figure 5: The current waveforms of a 10-line decimal to 4-line BCD encoder SN74147.

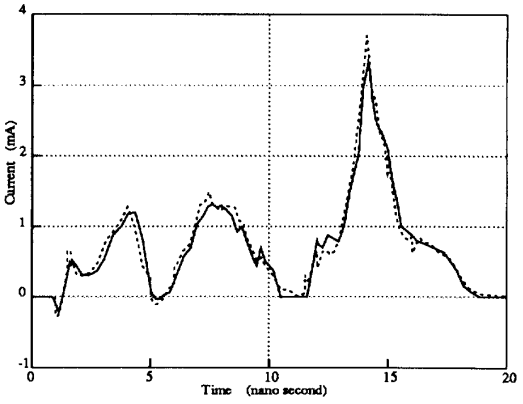


Figure 6: The current waveforms of a 4-bit carry-lookahead adder which is implemented using the domino logic, where the dashed lines are the results obtained by SPICE.