1.5V CMOS full-swing energy efficient logic (EEL) circuit suitable for low-voltage and low-power VLSI applications

C.C. Yeh, J.H. Lou and J.B. Kuo

Indexing terms: VLSI, CMOS integrated circuits, Logic circuits

A 1.5V full-swing energy efficient logic circuit is reported that is suitable for next-generation low-power VLSI applications using a low supply voltage. At 25MHz and at 1.5V, the power consumption of the EEL circuit is 70% of that for an ECRL circuit and 47% of that for the static circuit.

Introduction: For next-generation deep-submicron CMOS VLSI circuits, low supply voltage and low power are the trend. Adiabatic CMOS logic circuits have been reported for their potentials for low-power VLSI applications [1 – 4]. Early adiabatic logic circuits used diodes or diode-connected devices for the purpose of precharge [2], which may have limited their advantages. Recently, an efficient charge recovery logic (ECRL) circuit using a cascode voltage switch logic concept [3, 4] has been reported to give a better performance. Since its output is not full swing, it is not appropriate for low-voltage operation. In this Letter, a 1.5V full-swing energy efficient logic circuit suitable for low-voltage low-power VLSI is described. It will be shown that it has better noise immunity and a higher operation frequency.

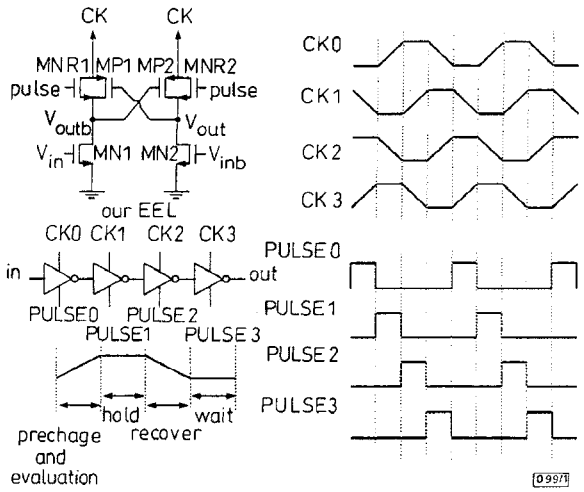

Fig. 1 *1.5V CMOS energy efficient logic (EEL) circuit*

1.5V energy efficient logic (EEL) adiabatic circuit: Fig. 1 shows the 1.5V CMOS full-swing energy efficient logic (EEL) circuit which is derived from the ECRL circuit. As shown in the Figure, four clocks connected to the power supply are required, each having four phases. The four phases of each clock are (i) precharge and evaluate, (ii) hold, (iii) recover and (iv) wait. In the precharge and evaluate phase. the clock voltage gradually increases from 0V to V_{dd}. If the input V_{in} is high and the complementary input $\overline{V_{in}}$ is low, the NMOS device *MN*1 is on and the NMOS device *MN*2 is off. Therefore, the complementary output node $\overline{V_{out}}$ is discharged to ground by *MN*1. Consequently *MP*2 turns on. As a result, the output node V_{out} increases as the supply clock (*CK*) rises. When the supply clock (*CK*) enters the hold phase, both outputs (V_{out} and $\overline{V_{out}}$) maintain their previous values. When CK decreases from V_{dd} to ground it is in the recovery phase, where charge previously stored in the load capacitance at the V_{out} node flows upwards to the CK supply. When CK is low, it is in the wait phase where the circuit is idle. Unlike the ECRL circuit, the EEL circuit has added the NMOS devices *MNR*1/*MNR*2 between the output node and the CK supply. When PULSE is high, *MNR*1/*MNR*2 are on. Therefore, during the wait phase, the remaining charge at the output node, which is not able to be discharged via the PMOS device, can be discharged to the CK supply via *MNR*1/*MNR*2. Consequently, the output voltage can reach 0V: full-swing of the output can be attained. In addition, more charge can be returned to the CK supply- a higher energy efficiency for the EEL circuit. (Note that without *MNR*1 and *MNR*2 as in the ECRL circuit, during the recovery phase. due to the threshold voltage of the PMOS device, the output voltage cannot drop to 0 V as CK falls: the output is not full-swing. As a result, the noise margin of the ECRL circuit may not be good.)

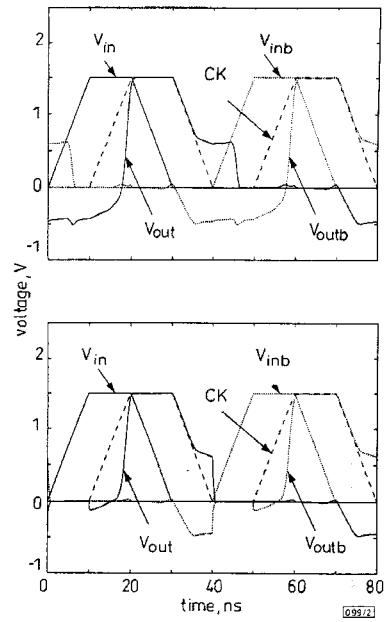

Fig. 2 *Transient waveforms of ECRL and EEL circuits*

Frequency = 25MHz
a ECRL
b EEL

Performance evaluation and discussion: To evaluate the performance of the EEL circuit, a logic system with four EEL circuits has been designed based on a 0.8μm CMOS technology. The aspect ratio of the PMOS devices is 10/0.8. The aspect ratios of the NMOS devices MN1/MN2 and *MNR*1/*MNR*2 are 5/0.8 and 2/0.8, respectively. A capacitive load of 10fF is placed at the output nodes. Fig. 2 shows the transient waveforms of *a* the ECRL circuit and *b* the EEL circuit using a 1.5V clock. Owing to the threshold voltage of the PMOS device, during the recovery phase, the output voltage V_{out} of the ECRL circuit cannot follow CK to reach the ground level. Since the NMOS device *MN*1 is off during both the recovery and wait phases, the complementary output node $\overline{V_{out}}$ is floating. Owing to clock feedthrough. the output voltage may drop to < 0V. During the following precharge and evaluate phase, when the PMOS device *MP*1 turns on, the consumed power of MP1 is large since the voltage drop between its source and drain is large ($V_{CK} - \overline{V_{out}}$). In the EEL circuit, during the wait phase, the complementary output node $\overline{V_{out}}$ is no longer floating. Owing to the NMOS devices *MNR*1 and *MNR*2, both output nodes (V_{out}, $\overline{V_{out}}$) are pulled to the same voltage level as the CK supply,

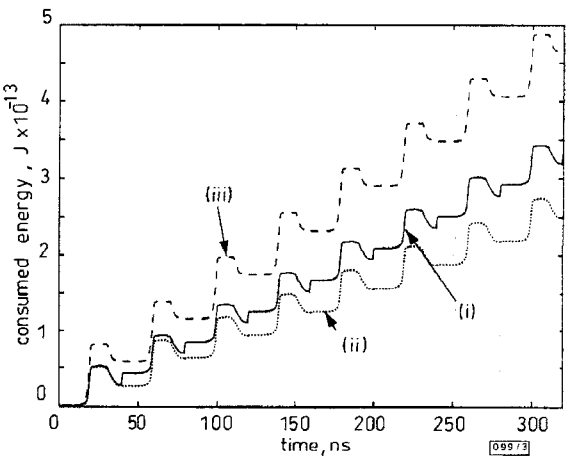

Fig. 3 *Consumed energy time during transient of ECRL and EEL circuits*

Frequency = 25MHz
Supply voltage = 1.5 V
(i) our EEL with PULSE driver
(ii) our EEL without PULSE driver
(iii) ECRL [9]

i.e. 0V. Therefore, in the following precharge and evaluate phase, the voltage drop between the source and the drain of the PMOS device *MP*1 is smaller than that in the ECRL circuit. Consequently, the consumed energy of *MP*1 in the EEL circuit is smaller than that in the ECRL circuit. From a power consumption point of view, a higher operation frequency can be obtained for the EEL circuit. Fig. 3 shows the consumed energy during the transients of ECRL and EEL circuits. Owing to the attachment of *MNR*1 and *MNR*2, the consumed energy of the EEL circuit is smaller than that of the ECRL circuit. Including the power consumption of the circuit used to generate the PULSE signal [4], and within a time window of 320ns. the EEL circuit consumes 3.3×10^{-13} *J*, which is 70% of that for the ECRL case (4.66×10^{-13} *J*).

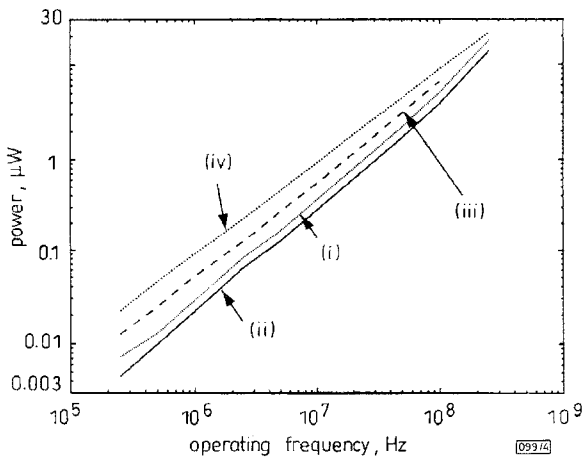

Fig. 4 *Consumed power against operating frequency of ECRL, EEL, and static circuits at 1.5 V*

Supply voltage = 1.5V
(i) our EEL with PULSE driver
(ii) our EEL without PULSE driver
(iii) ECRL [9]
(iv) static

Excluding power consumption used to generate the PULSE signal, the EEL circuit consumes 2.5×10^{-13} J, which is 54% of that for the ECRL case. Fig. 4 shows the consumed power against the operating frequency of the ECRL, EEL, and the static circuits at a 1.5V clock. As shown in the Figure, when the operating frequency is lowered. among three cases, the drop in the consumed power of the EEL circuit is largest. At 250KHz, the ECRL circuit consumes 10.9nW, the static circuit consumes 21.9nW, and the EEL circuit, including/excluding the power consumption of the circuit used to generate the PULSE signal, consumes 7.3/5.6nW. As for the maximum operation frequency, the EEL circuit can operate at the highest speed: 250MHz. Therefore, the EEL circuit can operate at the lowest supply voltage and highest speed; hence it is suitable for low-voltage operation.

Conclusion: In this Letter, a 1.5V full-swing energy efficient adiabatic logic circuit has been described. At 25MHz and at 1.5V, the EEL circuit has an energy consumption that is 70% of that for the ECRL circuit and 47% of that for the static circuit.

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2–46.5GHz quasi-static 2:1 frequency divider IC using InAlAs/InGaAs/InP HEMTs

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Indexing terms: High electron mobility transistors, Integrated circuits, Dividing circuits

The authors report a 2–46.5GHz quasi-static frequency divider IC using InAlAs/InGaAs/InP HEMTs. Wideband clock/data buffers and an HLO (high-speed latching operation)-type T-FF were incorporated to enhance the operating range. The IC was mounted on a dedicated IC package and operated up to 45.2GHz.

Introduction: High-speed frequency divider ICs with a wide operating range are a key component in broadband optical fibre communications systems. To date, 40GHz-class static frequency divider ICs have been developed using several compound semiconductor devices [1, 2]. The record operating frequency is 40.4GHz [1], which is not acceptable for 40GHz operation in real systems. With the advent of the dynamic operation, the maximum frequency can be increased to > 50GHz, but minimum frequency is sacrificed for any increases in maximum frequency beyond 25GHz [3]. Assuming a typical 40Gbit/s-class optical receiver configuration, including up to 1:8 data demultiplexing, operation over 40GHz with a wide frequency range of over one octave is required for the frequency divider IC.

Process technology: We used a 0.1μm gate length InAlAs/InGaAs/InP HEMT process [4]. The typical device parameters are the same as those reported in [5]. The average threshold voltage (V_{th}) is –0.5V with a standard deviation of less than 40mV for a 2in wafer). The average transconductance, f_T, and f_{max} are 950mS/mm, 174GHz, and 500GHz, respectively. The IC accommodates a standard interconnection process with double-layered Au-metal interconnection lines and air-bridges.

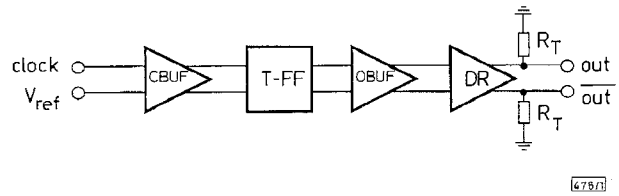

Fig. 1 *Circuit block diagram of 2:1 frequency divider IC*

CBUF: clock buffer, OBUF: output buffer, DR: driver, R_T: termination resistor

Circuit design: The circuit block diagram of the IC is shown in Fig. 1. To increase the maximum frequency and maintain a wide operating range, an HLO (high-speed latching operation)-type toggle flip-flop (T-FF) [6] was adopted for the core circuit. The gate width of the data latch circuit was set at one half of the data read circuit (20μm) to increase the maximum frequency while maintaining quasi-static operation from near 1GHz. Capacitive peaking was incorporated into the source followers of all the circuit blocks, which compensates for the loss at high frequencies and results in higher speed operation. The clock buffer consists of a two-stage inductor peaking differential buffer. A capacitively-coupled resistive divider was introduced as a low-loss passive RF level shifter, instead of a source follower. The lower cutoff frequency of the divider was designed at less than 1GHz so that a wide operating range from 1 to 50GHz was obtained. The internal