65GHz LTCC Probing Interface Design and Optimization

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Introduction

Probes present both a resistive (dc) and capacitive (ac) loads to the circuit under test. As expected, larger probes generally have larger tip capacitances that will affect the circuit being measured and result in measurement errors [1]. As frequency goes higher, the probe pitch should be made smaller to reduce its capacitive effect. Generally, a 400-μm probe pitch is used to measure frequency range up to 40GHz, and a 200-μm probe pitch is for V-band/W-band applications.

On the other hand, the low-temperature co-fired ceramic (LTCC) technologies have been successfully implemented for millimeter-wave applications [2]-[4]. To minimize the transmission line loss, a wide line-width, like 8-mil microstrip line-width for two-layer LTCC, is selected for the 50 Ω line design [5]. However, for V-band applications, like 60GHz WLAN, the 8-mil microstrip line-width can not match the 200-μm V-band probe pitch, so a 4-mil microstrip line-width should be selected for the probe interface design. Nevertheless, there is a discontinuity between the 8-mil microstrip and the 4-mil microstrip probe interface. This paper presents the design and optimization for the transition performance between 4-mil LTCC line and 8-mil LTCC line. The high frequency performance can be improved by adding vias connecting ground of the 4-mil microstrip and ground of 8-mil microstrip. We further adjust number of vias and their relative positions to achieve a return loss better than 20dB form DC to 65GHz.

Test Circuit Structure

The LTCC consists of DuPont 951 substrate with the silver via and silver microstrip inside. Each layer has a relative permittivity of 7.8 and a thickness of 3.54mil which yields the reasonable 50Ω transmission line.

Fig. 1(a) illustrates the top view of the back to back transition test circuit, and Fig. 1(b) is its side view. This structure is constructed by adding the two 4-mil microstrips between the probe interface and the center 8-mil microstrip. In the following discussions, as shown in Fig. 1(a) row represents a line parallel to the microstrip and column represents a line orthogonal to the microstrip. For example, Fig. 1(b) illustrates three rows and five columns.

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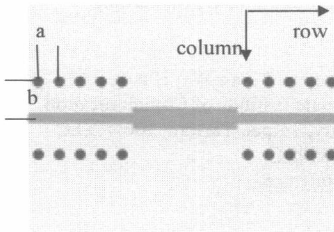


Fig. 1(a) top view of the back to back transition test circuit, via diameter = 4mil, a = via distance from center to center = 8mil

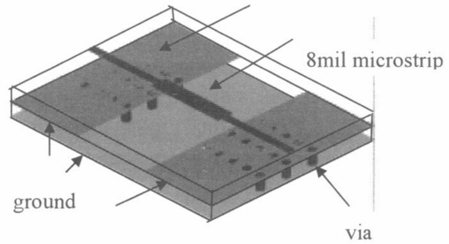


Fig. 1(b) side view of the test circuit

Design Optimization

A. Changing the number of columns of vias

Fig. 2 fixes the row distance 'b' as 14mil and compares two cases: 4 columns and 5 columns of vias. It is clear that increasing the number of vias parallel to the microstrip improves high frequency performance as to yield a return loss less than -20dB. Such condition is especially noted at frequency higher than 55GHz.

B. Changing the number of rows of vias

Fig. 3 fixes the row distance 'b' as 8 mil and compares three cases: 3 rows, 5 rows and 9 rows of vias. They have similar performance from 35GHz to 50GHz. It is noted that the zero frequency, which corresponds to the dip in the return loss, goes higher as frequency increases, and this results in the better return loss at 65GHz. From the simulation we know that the more vias, the smaller return loss. Three rows are enough since we can improve the high frequency performance by changing the distance between adjacent rows of vias, as discussed in the following paragraph.

C. Changing the distance of rows of vias

Fig. 4 fixes the number of rows of via as 3 and compares three cases, row distance 'b' of 10mil, 14mil and 18mil. The result shows that a close spacing may deteriorate electrical performance of the circuit and 14mil and 18mil both meet the goal of return loss better than 20dB at 65GHz (LTCC effective permittivity=5.5, so at 60GHz, 10 mil via edge-to-edge column spacing = 12% λ_g,). Then, we chose 14-mil via column spacing.

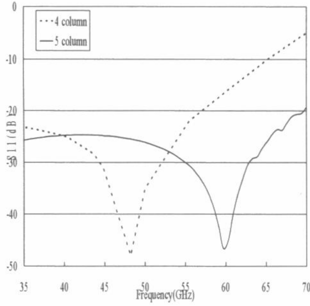


Fig. 2 different number of columns of vias

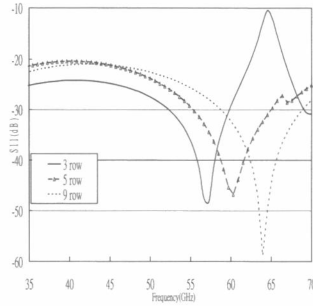


Fig. 3 different number of rows of via

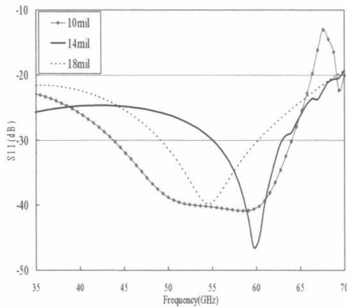


Fig. 4 different distance between adjacent two rows of vias.

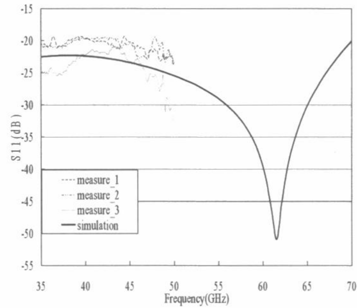
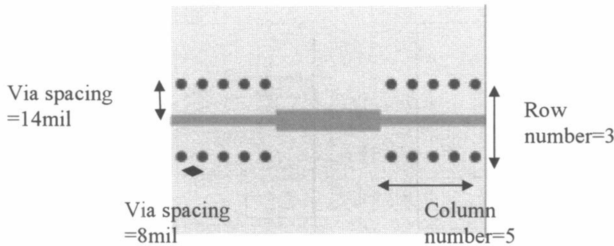


Fig. 5 simulation and the measurement result of the optimized design

Experiment Results

From simulation comparisons, we know that there are some ways to improve the high frequency performance. Firstly, vias along the microstrip should be arranged compactly, the design rule of minimum via spacing is 8mil, so we have 5 columns here. Secondly, along the line orthogonal to microstrip, better result can be achieved with increasing via number, and 3 rows can achieve better than 20dB, so it is chosen. Last, spacing between two row should be higher than 14mil to guarantees the 65GHz performance. Fig. 6 shows such an optimized structure: 5 columns, 3 rows of vias and distance between adjacent rows of vias is 14mil. Fig. 5 shows the measuring result and simulation result of the optimized structure, which has excellent agreements from 35GHz to 50GHz.



Conclusion

A 65GHz back to back transition test circuit is provided. By adding vias connecting grounds on different layers, we compensate the capacitive effect caused by the transition between probe and 8-mil microstrip line. Several factors, which may affect return loss, like number of vias, and distance between vias are simulated and compared. We carefully optimize the circuit to achieve a return loss better than 20dB at 65GHz and that measured data has an excellent agreement with the simulation results.

Acknowledgement

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