shown in Fig. 3. The amplifying function of STG2A in Fig. 2 is distributed to the first stage (STG1B) and the second stage (STG2B) of the two-stage AGC, and the STG2A of Fig. 2 is eliminated. In STG1B, as shown in Fig. 4, the sampling capacitors, b^3C (where b = 1/8dB), are connected to '*Vin*1' (= *INT*1 – *INC*1) when the MSB of the GCBs is '0' while the capacitors, $(b^{128} \times b^3)C$, are connected to '*Vin*1' with '1' of the MSB during the sampling mode. The feedback capacitors are selected by switches S0-S3 depending on the first and second LSBs. During amplification mode, the selected sampling capacitors connected to '*Vin*2' (= *INT*2 – *INC*2), and the voltage difference, '*Vin*1' – '*Vin*2', are amplified with the gain obtained equal to the ratio between the sampling and feedback capacitors selected by the MSB and the two LSBs. In contrast, the sampling capacitors of STG2B are selected by the capacitor-segment combination logic with four middle bits while the feedback capacitors are controlled by the third LSB.

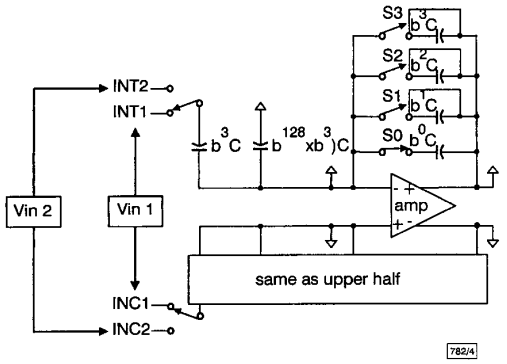

Fig. 4 *First-stage (STG1B) architecture of two-stage AGC during sampling mode*

*Vin*1: output from SHA1 of CDS
*Vin*2: output from SHA2 of CDS
b: gain step

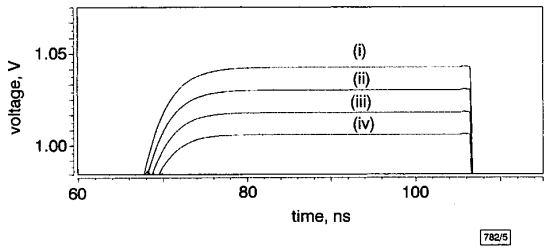

Fig. 5 *Simulated STG1B outputs depending on 1st and 2nd LSBs with MSB set to '1'*

(i) 11
(ii) 10
(iii) 01
(iv) 00

In the proposed two-stage AGC, the feedback capacitance varies depending on the three LSBs of the GCBs, which means that the feedback gains of operational amplifiers may not be constant during amplification mode. However, since the ratio of the sampling capacitance to the feedback capacitance varies within 6% according to the GCBs, the variation in feedback gain can be ignored and hardly influences the settling time for the AGC. As shown in Fig. 5, the simulated STGIB outputs in the amplification mode with an input voltage of 0.16V demonstrate that the settling times of the output voltages are almost constant. By applying the two-stage AGC to the front-end system, the power consumption and chip area are reduced by ~20% without performance degradation in parameters such as speed.

Conclusions: Digitally-controlled AGCs eliminating conventional extra DACs have been proposed. The video-speed operation with low-power consumption of the AGCs is achieved by the proposed capacitor-segment combination technique. The two-stage AGC architecture minimises power consumption and chip area with identical performance to that of a three-stage AGC.

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Dual-input RC integrator and differentiator with tuneable time constants using current feedback amplifiers

Jiin-Long Lee and Shen-Iuan Liu

A dual-input RC active integrator and a differentiator with tuneable time constants are described. They are suitable for analogue signal processing applications, and have been implemented using a commercially available current feedback amplifier. Experimental results confirm theoretical prediction.

Introduction: Active RC integrator and differentiator networks are commonly used in analogue signal processing applications, such as waveform shaping, process controller design, and calibration circuits, etc. [1, 2]. Many active RC networks with tuneable time constants have been reported [3, 4]. There are some disadvantages to the use of conventional operational amplifiers as active elements. First, the finite gain bandwidth product of the op-amp will limit the accuracy and decrease the operating frequency range [3, 4]. A building block called a current feedback amplifier (CFA) can offer wider bandwidth and better accuracy than conventional operational amplifiers [5, 6]. Dual-input integrators and differentiators are needed in signal processing applications [3, 4, 7]. In this Letter a new dual-input integrator and a differentiator with tuneable time constants are presented.

Circuit description: In general, a CFA is a four-terminal network, and its characteristics can be described by the following:

$$V_x = V_y \qquad i_z = \pm i_x \qquad i_y = 0 \quad \text{and} \quad V_o = V_z \qquad (1)$$

where the plus and minus signs denote a noninverting CFA and an inverting CFA, respectively.

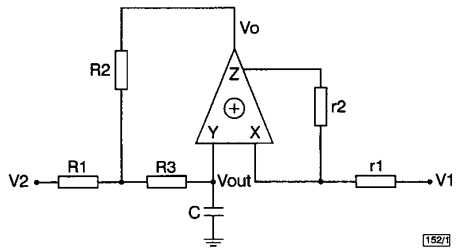

Fig. 1 *Dual input integrator employing non-inverting CFAs*

(i) *Integrators*: The proposed integrator using a CFA is shown in Fig. 1, and a routine analysis yields

$$V_{out} = \frac{V_2\frac{R_2}{R_1} - V_1\frac{r_2}{2r_1}}{SC\left(R_3\left(1+\frac{R_2}{R_1}\right)+R_2\right)-\left(\frac{r_2}{2r_1}-\frac{R_2}{R_1}\right)} \quad (2)$$

If the implementation condition for an integrator is $R_2/R_1 = r_2/2r_1$, then the transfer function of a dual input integrator can be expressed

$$\frac{V_{out}}{V_2 - V_1} = \frac{1}{s\tau} \quad (3)$$

where

$$\tau = kCR_1 \qquad k = \left[1 + R_3\left(\frac{1}{R_1}+\frac{1}{R_2}\right)\right]$$

The nominal value of the time constant is multiplied by a factor k. It is obvious that R_3 can be changed to obtain various time constants.

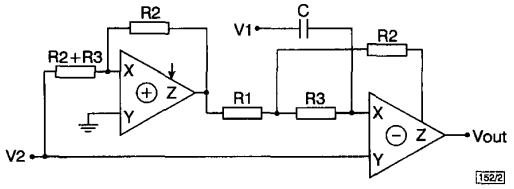

Fig. 2 *Dual input differentiator using CFAs*

(ii) *Differentiator:* The proposed differentiator using CFAs is shown in Fig. 2. Routine analysis gives

$$V_{out} = V_2\left(\alpha - \frac{R_2}{R_3}(1-\alpha)\right) + SC(V_1 - V_2)\left[R_2 + R_1\left(1+\frac{R_2}{R_3}\right)\right] \quad (4)$$

If $\alpha = R_2/(R_2+R_3)$, then eqn. 4 can be rewritten as

$$\frac{V_{out}}{V_1 - V_2} = s\tau \quad \text{and} \quad \tau = CR_2\left(1 + R_1\left(\frac{1}{R_2}+\frac{1}{R_3}\right)\right) \quad (5)$$

If we make $R_2 = R_3 = R$ and $R_1 = n_R$, then the time constant in eqn. 5 can be expressed as

$$\tau = (2n+1)CR \quad (6)$$

Obviously, we can obtain various time constants by changing R_1.

Experimental results: To verify the theoretical analysis of the proposed network, the configurations have been realised with commercially available CFAs (AD844). A practical inverting CFA has been constructed using two AD844s.

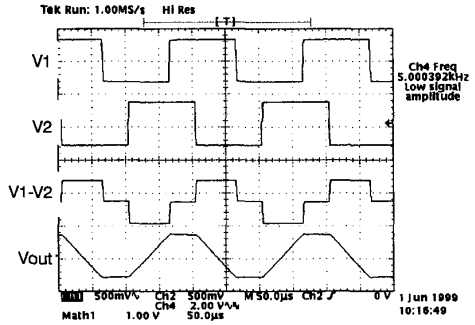

Fig. 3 *Experimental results of Fig. 1*

(i) *Integrator:* Fig. 3 shows a typical result for the integrator. The rectangular waveform V_1 (channel 1) with 0.65V peak-to-peak and V_2 (channel 2) with 0.65V peak-to-peak at 5kHz were applied to the circuit of Fig. 1, with $C_1 = 953$pF, $R_1 = 4.98$kΩ, $R_2 = 5$kΩ, $R_3 = 4.98$kΩ, $r_2 = 5$kΩ, $r_1 = 2.5$kΩ. The waveform of $V_1 - V_2$ (channel 3) is also shown in Fig. 3. The horizontal scale is 50µs/div. The output waveform of the proposed dual-input integrator is shown in the lowest trace of Fig. 3. The operating frequency range is 450Hz–1MHz with a phase error of 5°.

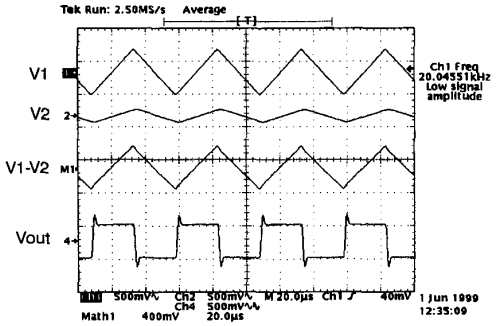

Fig. 4 *Experimental results of Fig. 2*

(ii) *Differentiator*: Fig. 4 shows a typical result for the differentiator. Two triangular waveform V_1 (channel 1, 0.68V peak-to-peak) and V_2 (channel 2, 0.2V peak-to-peak) at 20kHz were applied to the circuit of Fig. 2 with $C = 857$pF, $R_1 = 4.99$kΩ, $R_2 = 4.99$kΩ, $R_3 = 5.01$kΩ, $R_4 = 10.02$kΩ, $R_5 = 10$kΩ, $R_6 = 3$MΩ, $C_2 = C_3 = 4.5$pF. The waveform of $V_1 - V_2$ (channel 3) is also shown in the Fig. 4. The horizontal scale is 20µs/div. The output waveform of the dual input differentiator is shown in the lowest trace of Fig. 4. The operating frequency range is 1–100kHz with a phase error of ±10°. This error is due to the finite gains and parasitic capacitors of the active elements.

Conclusion: A dual-input active RC integrator and a differentiator with tuneable time constants have been developed. In both circuits the time constants can be increased by adjusting a single resistor. The use of CFAs as the active element can enable a better frequency response to be obtained than that for a voltage mode operational amplifier. Experimental results have been presented which prove the feasibility of the proposed networks.

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