A Period Tracking Based On-Chip Sinusoidal Jitter Extraction Technique

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Abstract

In this paper, an on-chip sinusoidal jitter extraction technique based on period tracking is presented. The proposed technique is a viable on-chip solution. It utilizes a variable delay line and a phase comparator to track the signal's cycle lengths without external reference. Digital signal processing techniques are then applied to the obtained signal period sequence to derive the amplitudes and frequencies of the sinusoidal jitter components. Numerical simulations are performed to validate the idea. The results show that the proposed approach can achieve high amplitude and frequency estimation accuracy and is robust in the presence of random jitter components and delay line variations.

Keywords—sinusoidal jitter, jitter decomposition, built-in self-test, built-in self-diagnosis.

1 Introduction

To fulfill the growing data bandwidth demand, high-speed serial link (HSL) systems have become the mainstream. For HSL systems, one of the factors that determine the overall quality is jitter which is the deviation in a signal's edge transitions from their ideal positions. Due to the high timing resolution and accuracy requirements, jitter measurement and characterization usually rely on expensive automatic test equipment (ATE) and are time-consuming. The problems get more severe as the trend of system integration onto a single chip or package continues. For IC's that possess tens or even hundreds of HSL channels, testing all the channels in parallel will require prohibitively expensive test equipment.

Separating and identifying the jitter components is essential for both communication system testing and diagnosis. Depending on the underlying mechanisms, jitter is divided into two categories: random jitter (RJ) and deterministic jitter (DJ). The main difference is that the former is unbounded and the latter is bounded. DJ is further divided into inter-symbol interference (ISI), duty cycle distortion (DCD), and periodic jitter (PJ). The impacts of distinct jitter components on the system performance, e.g., bit-error-rate (BER), are different. For instance, most clock recovery circuits in the receiver end can tolerate a fair amount of low-frequency PJ. However, the same amount of RJ can be catastrophic and cause system failure. As a result, it is misleading and often inaccurate to estimate the system performance based on the overall jitter characteristics like mean and variance.

In this paper, we are interested in extracting the amplitude and frequency information of sinusoidal jitter (SJ) components. In [14], a jitter decomposition technique is presented. Using a pattern marker as the measurement reference, DCD and ISI are derived from the mean edge transition locations. PJ and RJ, on the other hand, are calculated through spectral analysis of the edge locations. The limitation of this method is that the required measurements must cover the full length of the repeatedly transmitted pattern. In [15], the $\Delta\phi$ method is proposed to extract the peak-to-peak and RMS values of a sinusoidal jitter. Using frequency division, the $\Delta\phi$ method is further extended to handle 10 GHz clock in [16]. The above SJ extraction techniques are more suitable for external test equipment, and cannot be easily adapted for on-chip applications.

In [7], an on-chip SJ extraction algorithm is presented. Under the assumption that an on-chip single-shot time measurement unit (TMU) is available, the signal period is measured once in a pre-specified number of cycles, determined by the TMU throughput. After a sufficient number of signal periods are collected, the list of periods are low-pass filtered to remove the RJ components. Then, sample time estimation, period estimation, and FFT are applied to the resulting list to derive the SJ amplitude and frequency. In [8], the durations of multiple instead of a single period are measured to extend the method's capability to handle ultra high-speed signals. The limitation of [7, 8] is the TMU performance. Many on-chip TMU solutions have been proposed [3, 2, 11, 12, 13, 1]. To achieve high timing resolution, most TMU solutions are explicitly or implicitly based on the vernier delay line concept which leads to low throughput.

The contribution of this work is a low-cost on-chip SJ extraction technique. Compared to previous techniques, the proposed method has the following advantages:

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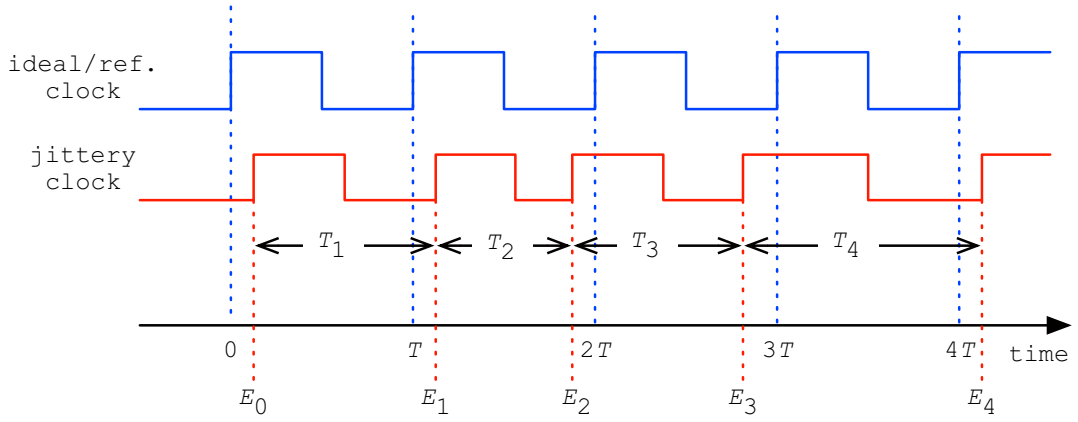

Figure 1. Notations for jitter definitions.

Low hardware complexity: The required analog circuitry includes a variable delay line and a phase comparator. Together with the digital controller, they digitize the period variation information. Post processing involves digital signal processing (DSP) procedures that can be realized on-chip if sufficient digital resources are available or off-chip by low-cost PC-based ATE.

Robustness: The proposed approach is rather insensitive to RJ components and delay line variations—both are essential for it to be a practical on-chip solution.

Numerical simulations are performed to validate our idea. For a wide range of RJ strength, delay line variations, and SJ frequencies, the SI frequency estimation error is less than 1% and the amplitude estimation error is less than 5%.

The rest of the paper is organized as follows. In Sec. 2, a brief description of related background is given. In Sec. 3, the proposed SJ extraction technique is illustrated in details. Experimental results are presented in Sec. 4. Practical issues are discussed in Sec. 5 and we conclude this work in Sec. 6.

2 Preliminaries

2.1 Jitter definitions

Depending on the applications, jitter may be interpreted in different ways, e.g., period jitter, cycle-to-cycle jitter, and time interval error (TIE). The notations for defining jitter is illustrated in Fig. 1. The upper waveform is an ideal (or reference) clock of which the period is T, and the lower one is a jittery clock signal. Four consecutive cycles of the two clock signals are shown. E_i's correspond to the rising edge locations and T_i's the actual periods of the jittery signal. Jitter is then defined as follows.

Period jitter J^P: Period jitter is the deviation of the actual periods from the ideal (average) period, i.e., $J_i^P = T_i - T$.

Cycle-to-cycle jitter J^{CC}: Cycle-to-cycle jitter is the difference in the periods of adjacent cycles, i.e., $J_i^{CC} = T_i - T_{i-1}$.

Time interval error J^{TIE}: Time interval error is the deviation of the actual rising edges from ideal/reference edges, i.e., $J_i^{TIE} = E_i - i \cdot T$.

Since the above definitions are just different ways of interpreting the same phenomenon, they can be derived from each other; however, the corresponding measurement requirements are not the same.

Period jitter measurement is the most direct because it does not require any external reference. Many high-resolution time measurement techniques are available to measure the signal periods from which period jitter can be derived. For high-speed signals, one may under-sample the signal periods if the TMU does not have sufficient throughput, or measure the aggregate length of several cycles instead.

TIE measurement, on the other hand, requires an external reference generated by hardware or software. The requirement of external reference makes TIE measurement a less viable on-chip solution because the chip I/O pin bandwidth and signal path parasitic effects limit the delivery of high-quality reference signals into the chip.

Based on the above observations, our SJ extraction technique extracts the period jitter information.

2.2 Period comparison

To reduce the complexity of the required analog circuitry, our SJ extraction technique utilizes a period comparator instead of a high-resolution TMU to digitize the jitter information. The comparator can be made simple because it only determines whether a cycle length is greater than the threshold or not.

The block diagram of the period comparator is shown in Fig. 2. Consisting of a delay line and a phase comparator, it was previously adopted by [10, 5, 6]. The phase comparator determines the phase relationship (lead or lag) between the rising edges of SUT and SUT', the delayed SUT. Let A and B be two consecutive rising edges on SUT, and A' the rising edge on SUT' that corresponds to A. If the cur-

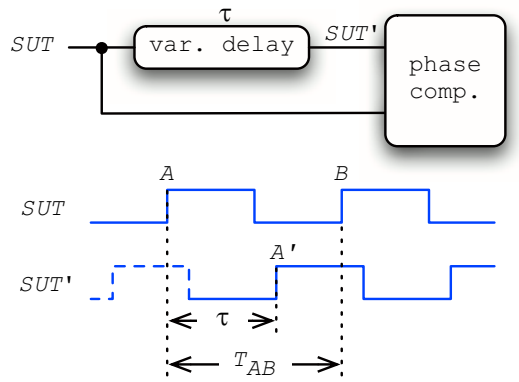

Figure 2. The period comparator.

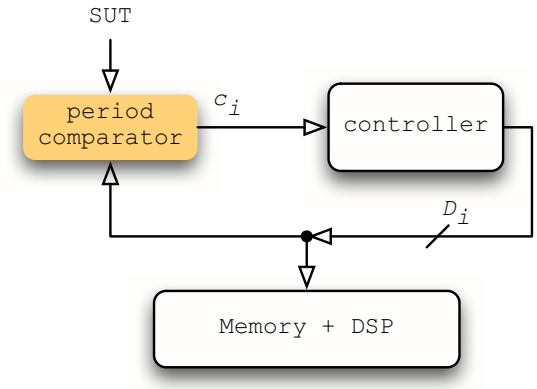

Figure 3. SJ extract circuit.

rent cycle duration T_{AB} is longer than the delay line value τ (as shown in Fig. 2), B will lag A' and the phase comparator output is one; otherwise, the phase comparator output is zero. The period comparator can be viewed as a high-throughput one-bit digitizer.

3 The proposed SJ extraction technique

3.1 The SJ extraction circuit

The architecture of the SJ extraction circuit is depicted in Fig. 3. It consists of a period comparator and a controller, and relies on DSP resources for post-processing. The only analog block in the SJ extraction circuit is the period comparator. The functions of the blocks are as follows:

The period comparator: The inputs to the period comparator include the signal under test (SUT) and the delay control signal D_i where i is the cycle index. Let's use $delay_i$ to denote the delay line value at the i-th cycle. The comparator output c_i at the i-th cycle is one if the i-th period T_i is greater than $delay_i$; otherwise, c_i is zero. Not shown in Fig. 2, reconfiguration circuits and wiring are added to allow delay line calibration using the oscillation-based method.

The controller: Depending on the comparator output, the controller adjusts D_i such that the delay line value *tracks* the signal period, called *period tracking*. With the period tracking process, the delay line value sequence approximates SUT's period sequence. Details of the period tracking process will be discussed later.

Memory + DSP: During period tracking, the D_i sequence is stored in the memory. To extract the SJ information, D_i's are first translated to $delay_i$'s according to the delay line calibration results. DSP procedures are than applied to the $delay_i$ sequence for SJ extraction.

3.2 The SJ extraction flow

The proposed SJ extraction algorithm consists of three phases: (1) delay line calibration, (2) period tracking, and (3) post-processing.

3.2.1 Delay line calibration

In the delay line calibration phase, one may utilize the oscillation-based approach to measure the delay line values. Detailed analysis of the approach can be found in [9]. In summary, the main error sources include numerical rounding error, systematic and random errors of the observation time window, and time and temperature variations. Except for the time and temperature variations which have to be solved through circuit design techniques, the negative effects of the other sources can be reduced to an acceptable level by lengthening the observation window.

One systematic error of this method is the delay associated with the circuits that reconfigure the delay line into an oscillator. This error introduces an DC offset to the $delay_i$ sequence. During spectral analyses, the DC offset becomes the DC component and may affect the amplitude accuracy of low frequency SJ due to spectral leakage.

3.2.2 Period tracking

The *period tracking* process is intended to obtain SUT's period vs. time information, and is realized by the variable delay line, the period comparator, and the controller.

The flow of the period tracking procedure is shown in Fig. 4. In each iteration, w period comparisons are made with respect to the same delay line value to obtain one period sample, and the procedure continues until enough samples are collected. If the periods of more than $w/2$ cycles are greater/less than current delay value, the delay line value shall be increased/decreased in next iteration. This information is stored in the inc variable—1 for increment and -1 for decrement. Note that the reason of making more than one phase comparison per iteration is to alleviate the negative impact of RJ components. One side benefit is that except for the counter that records the lead/lag counts, the rest of the controller does not have to operate at the same speed as the symbol rate. The drawback of this approach is reduced period sampling rate which degrades the SJ measurement bandwidth.

To better track the signal periods, the amount of delay

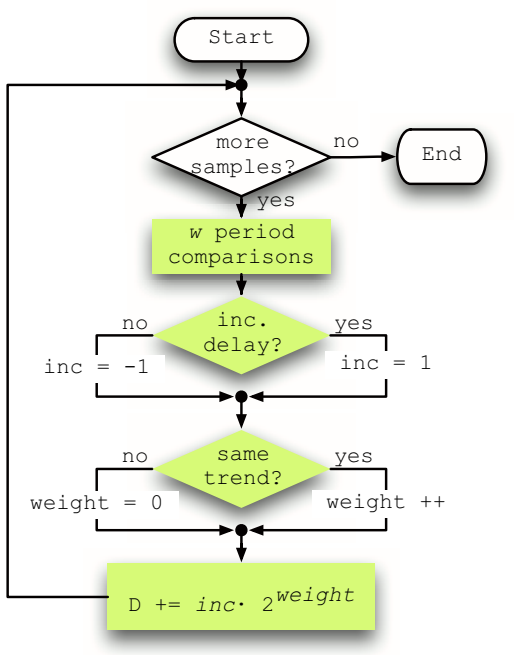

Figure 4. The period tracking algorithm.

value change is dynamically adjusted. If the same trend is observed, i.e., inc is the same as that of the previous iteration, the amount of change will be doubled. The amount of change is controlled by the weight factor $weight$. It is incremented if the current inc value is the same as that of previous iteration; otherwise, it is reset to zero.

Finally, the delay line input is updated as follows:

$$D_{i+1} = D_i + inc \cdot 2^{weight}$$

If the resulting value exceeds the delay line range, it is replaced by the maximum or minimum delay value. Note that real delay lines take finite time to settle to a new value. During the settling time, period comparisons should be skipped or ignored.

A period tracking example is shown in Fig. 5. For ease of explanation, each sample is obtained by making only one period comparison, i.e., $w = 1$, and no RJ component is added. In this figure, the x-axis corresponds to the sample index, and the y-axis is the cycle period. The square dots represent the SUT cycle lengths. In this example, we assume that the variable delay line has seven different delay values, $\tau_0, \tau_1, \tau_2, \ldots, \tau_6$. The inc and $weight$ waveforms are shown at the bottom of the figure, and the round dots represent the delay line values. Note that, in practice, $weight$ can be greater than 1 for higher frequency SJ components.

3.2.3 Post-processing

In reality, period tracking results are not as good as that in Fig. 5 due to RJ components which introduce high frequency variations in cycle lengths. Making multiple period comparisons in each iteration does not completely eliminate the negative impact. In addition to the tracking quality, the spectral leakage effect must also be taken into account because coherent sampling is in general not possible.

To ensure high SJ estimation accuracy, the following DSP procedures are applied to the collected delay line value sequence: (1) Blackman-Harris windowing, (2) spectral peak interpolation, and (3) amplitude compensation.

Blackman-Harris windowing: Application of the general purpose Blackman-Harris windowing to the tracking sequence reduces the spectral leakage at the cost of a wider main lobe.

Spectral peak interpolation: To accurately estimate the SJ frequency, we utilize the Gaussian interpolation method [4]. Let S_{i-1}, S_i, and S_{i+1} be the three highest spectral coefficients, and $s_i = \log S_i$. The amplitude A and frequency f are estimated by

$$f = f_i + \frac{s_{i-1} - s_{i+1}}{2\left(s_{i+1} - 2s_i + s_{i-1}\right)} \quad (1)$$

$$A = s_i - \frac{\left(s_{i-1} - s_{i+1}\right)^2}{8\left(s_{i+1} - 2s_i + s_{i-1}\right)} \quad (2)$$

where f_i is the frequency of the i-th spectral bin.

Amplitude compensation: One side effect of applying the windowing technique prior to FFT analysis is the reduced power. Once the the SJ frequency is known, the corresponding compensation factor is obtained from a pre-computed lookup table, and applied to the previously computed amplitude.

4 Experimental results

To validate the proposed technique, numerical simulations are performed. The default simulation setup is as follows: (1) The signal frequency is 3 GHz which corresponds to a period of about 333 ps. (2) SJ contains two tones, 100 KHz and 1 MHz, both of which have the same amplitude of 33.2 ps. (3) The standard deviation of RJ is 12 ps. (4) $w = 8$ period comparisons are made to collect a cycle length sample. (5) The ideal delay line resolution, i.e., 1 LSB, is 8 ps.

The SJ extraction results are shown in Table 1. The first column lists the total number of cycles, denoted by N. In columns two and three, the mean and 3σ values of the amplitude error percentages are shown. Columns four and five are the frequency error percentages. It is observed that the amplitude and frequency errors at $N = 2^{15}$ are relatively larger. The reason is that when $N = 2^{15}$ the FFT bin separation is about 91 KHz which is close to the low frequency SJ component. The low spectral resolution degrades the estimation accuracy. For N greater than 2^{17}, the amplitude errors are less than 1.5%, and the frequency errors are less than 0.2%.

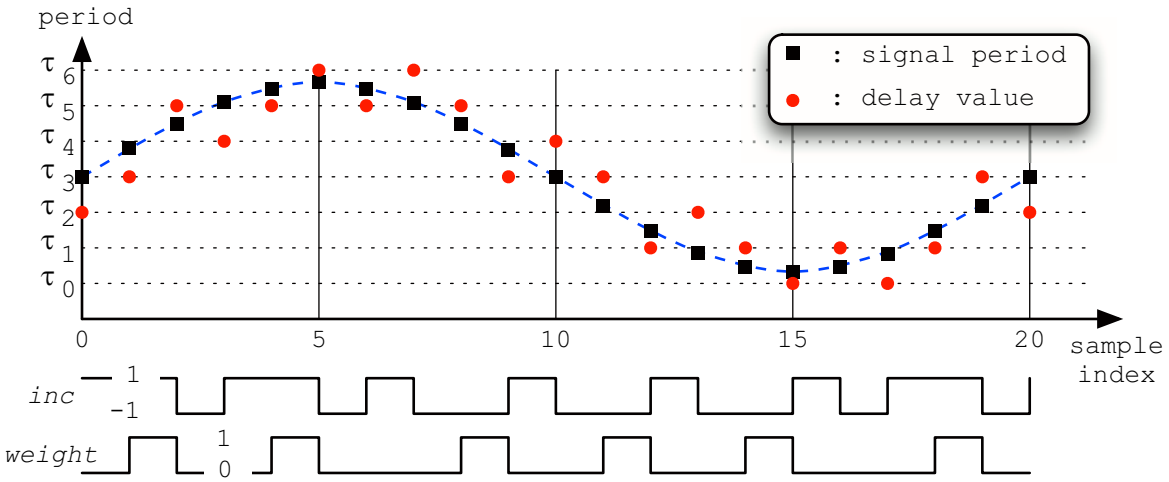

Figure 5. The period tracking process.

Table 1. SJ extraction results.

	amplitude error		frequency error	
N	mean (%)	3σ (%)	mean (%)	3σ (%)
2^{15}	2.248	3.232	14.048	0.935
2^{16}	1.761	2.267	0.716	0.455
2^{17}	1.145	1.536	0.050	0.172
2^{18}	1.263	1.103	0.047	0.062
2^{19}	1.328	0.761	0.018	0.024
2^{20}	1.353	0.518	0.008	0.008

To validate the technique's tolerance to RJ components, N is fixed at 2^{17} and we increase RJ σ from 12 to 96 ps. (The remaining setup parameters are kept the same as the default.) The results are shown in Table 2. Except for the first column which lists the RJ σ's, the notations are the same as those in Table 1. One can see that RJ strength has a larger impact on amplitude than frequency estimation. Although the mean amplitude error is small, the 3σ value increases substantially, implying that N should be increased to reduce the RJ effect.

Table 2. Impact of RJ strength.

	amplitude error		frequency error	
RJ σ	mean (%)	3σ (%)	mean (%)	3σ (%)
12 ps	1.145	1.536	0.050	0.172
24 ps	1.185	2.452	0.081	0.295
48 ps	1.164	5.057	0.143	0.519
72 ps	1.445	6.460	0.157	0.618
96 ps	0.715	8.605	0.313	1.184

In Table 3, the delay line resolution (1 LSB) is varied from 8 to 80 ps. Similar to the previous experiment, the delay line resolution has a larger impact on the amplitude than frequency estimation. Note that the delay line non-linearity is not a problem for our technique because the delay line is characterized in the calibration phase.

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Table 3. Impact of delay line resolution.

	amplitude error		frequency error	
LSB	mean (%)	3σ (%)	mean (%)	3σ (%)
8 ps	1.191	1.412	0.049	0.157
16 ps	0.919	1.631	0.057	0.203
24 ps	1.306	1.844	0.068	0.240
32 ps	-0.608	2.276	0.064	0.244
40 ps	3.152	2.850	0.094	0.284
48 ps	5.589	3.441	0.092	0.315
56 ps	0.410	4.334	0.096	0.337
64 ps	-7.418	4.248	0.086	0.347
72 ps	-9.293	3.598	0.118	0.428
80 ps	-2.191	3.678	0.114	0.406

SJ components is varied from 200 KHz to 30 MHz, and the results are shown in Table 4. While the frequency estimation remains accurate, the amplitude estimation error grows substantially beyond 20 MHz.

Table 4. Impact of SJ frequency.

	amplitude error		frequency error	
f_2	mean (%)	3σ (%)	mean (%)	3σ (%)
200 KHz	0.793	1.558	0.087	0.233
1 MHz	1.210	1.361	0.055	0.175
2 MHz	1.234	1.581	0.075	0.149
3 MHz	1.238	1.356	0.043	0.118
6 MHz	1.530	1.371	0.057	0.125
12 MHz	3.042	1.728	0.049	0.170
18 MHz	3.883	1.748	0.057	0.201
24 MHz	9.247	2.341	0.068	0.255
30 MHz	19.922	4.090	0.092	0.336

In summary, the simulation results show that (1) frequency estimation is robust if only sufficient samples are collected, and (2) the amplitude estimation is relatively more sensitive; however, the errors are within 5% for most of the cases.

5 Practical considerations

Delay line and phase comparator induced jitter: The inevitable circuit noise in the variable delay line and the phase comparator introduce jitter to the signal under test. Since the noise induced jitter component is in general Gaussian, from the results of Table 2, it has little effect on the SJ extraction results.

Delay line variation and non-linearity: Although circuit design techniques may be utilized to reduce the impact of process deviations on the delay line values, the non-linearity issue still exists. Since the post-processing stage directly utilizes the delay line values, i.e., $delay_i$'s, obtained in the calibration stage, if only the delay values are sufficiently accurate (which can be achieved by lengthening the calibration time), the delay line non-linearity or variation induced error is insignificant. In fact, the measurement offset of $delay_i$'s caused by the oscillation method, is a more severe problem. During spectral analysis, the offset in delay line values becomes a DC component in the frequency spectrum which may affect the extraction results due to spectral leakage. More sophisticated post-processing may be adopted to remove the DC component for more accurate results.

Control circuit design: In practice, it is very difficult to design a controller that operates at GHz level. In our technique, this issue is resolved by making phase comparisons for w cycles with the same delay line value. Although the original purpose is to lower the effect of RJ component and make the tracking sequence smoother, it turns out to relax the controller operation frequency at the same time, i.e., the controller generates the delay control signal, D_i, every w cycles. Note that the counter that keeps track of the lead/lag count still has to operate at the symbol rate.

6 Conclusion

A sinusoidal jitter extraction technique based on period tracking is reported in this paper. The proposed technique is a viable on-chip solution because it relies on simple BIST circuitry to digitize the SJ information, and DSP techniques to extract the SJ information. Furthermore, the algorithm is rather insensitive to process variations and the BIST circuitry induced random jitter. A series of simulations are performed to validate the technique. The results show that both the frequency and amplitude estimations are accurate for a wide range of input conditions and circuit parameters. In the future, we will extend the proposed technique to handle other DJ components and extract RJ information.

Acknowledgement

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