SiC vs. Si: Two-Dimensional Analysis of Quasi-Saturation Behavior of DMOS Devices Operating at Elevated Temperatures

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Abstract

This paper reports a 2D analysis of the quasi-saturation behaviorof 6H-SiC DMOS devices considering surface trapping effect. Based on the study, in the pre-quasi-saturation region, the drain current is predominantly determined by the surface trapping effect. In the quasi-saturation region, the drain current is mainly influenced by the electron mobility in the substrate region.

Summary

6H-SiC material is receiving a lot of attention for high-temperature and high-power applications owing to its large bandgap, high thermal conductivity, and high breakdown voltage [1][2]. Using 6H-SiC, MOS devices have been fabricated [3]. For DMOS devices, quasi-saturation behavior is important [4]. In this paper, a 2D simulation study on the quasi-saturation behavior of 6H-SiC DMOS devices considering surface trapping effect is reported. It will be shown that in the pre-quasi-saturation region, the drain current is predominantly determined by the surface trapping effect. In the quasi-saturation region, the drain current is mainly influenced by the electron mobility in the substrate region. In the following sections, the device structure of the 6H-SiC DMOS under study is described first, followed by the quasi-saturation behavior.

Consider the cross section of a 6H-SiC DMOS device [4] as shown in Fig. 1. The DMOS device has an N^- epi region of 11μm with a doping concentration of $1 \times 10^{16}cm^{-3}$ and an N^+ polysilicon gate with an oxide thickness of 500Å and a double-diffused channel of 1.3μm. In order to simplify the analysis, only half of the device is studied. In order to facilitate 2D device simulation for the 6H-SiC DMOS device, in the PISCES program, appropriate models [5] as shown in Fig. 2 have been used. As shown in Eq. (1) of Fig. 2, the energy bandgap of the 6H-SiC is much larger than that of Si. Due to a much larger bandgap, the intrinsic carrier concentration of the 6H-SiC is much smaller as shown in Eq. (2), as compared to Si. For 6H-SiC, incomplete ionization of donors (Eq. (3)) cannot be neglected since $E_D - E_{fn}$ is smaller. Compared to Si, the permittivity of 6H-SiC is smaller.

The electron mobility model in the 6H-SiC DMOS device is different from that in the Si DMOS device. In the bulk of the 6H-SiC DMOS device, the electron mobility model is similar to that for Si as shown in Eqs. (5)(6). Compared to Si, it has a larger saturated velocity and a smaller mobility-a much larger critical electric field. As for Si, as temperature goes up, the saturated velocity and the mobility becomes smaller. As for Si, an electric field dependent mobility model has been used (Eq. (7)). In the lateral channel region, the mobility model is different. In the lateral channel region of the 6H-SiC DMOS device, Al has been used as the p-type dopant [6]. During oxide growth, Al is incorporated into oxide, thus, "slow" electronic trapping centers are formed at the oxide interface. Carriers in the lateral channel may be trapped by these trapping centers. As a result, the effective mobility is much lowered. As the ambient temperature is raised, the heated electrons in the lateral chanel may stand against being trapped by the trapping centers. Therefore, as the temperature goes up to within certain range, the effective channel mobility may increase. In order to show the influence of the surface trapping effect, 2D device simulation of the 6H-SiC DMOS device has been carried out with and without considering surface trapping effect.

Fig. 3 shows the I_D vs. V_{GS} curves of the 6H-SiC DMOS device biased at V_{DS} = 10V, 30V, 50V, operating at an ambient temperature of 100C, 150C, and 200C. Solid lines show the results considering the surface trapping effect and dashed lines are for without considering it. At 100C, considering surface trapping effect, the drain current is much smaller, as compared to the case without considering

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it. Without considering surface trapping effect, quasi-saturation behavior: "As V_{GS} is greater than a certain value, the drain current is almost independent of V_{GS}" can be observed. Considering surface trapping effect, no quasi-saturation can be seen – only pre-quasi-saturation exists at 100C. As reported in the previous paper [4], in the pre-quasi-saturation region, the drain current is predominantly determined by the lateral channel and in the quasi-saturation region, the drain current is mainly determined by the current conducting region in the bulk. Therefore, in the pre-quasi-saturation region, the drain current is mainly influence by the surface trapping effect and, in the quasi-saturation, it is determined by the electron mobility in the substrate region. As shown in the figure, as the temperature is raised, without considering the surface trapping effect, the drain current is lowered. At a higher temperature, considering surface trapping effect, the pre-quasi-saturation region is shrunk. As reflected in the slope in the pre-quasi-saturation, the effective mobility is raised at a higher temperature since the positive surface trapping effect. As shown in the figure, as the temperature is raised to 200C, the drain current for the cases with and without considering surface trapping effect gets similar. Therefore, at a certain high temperature, for the 6H-SiC DMOS device biased at quasi-saturation, the surface trapping effect becomes less important in determining the drain current.

Fig. 4 shows the electron density profiles in the vertical direction at the right side of the 6H-SiC DMOS device, biased at V_{GS} = 30V and V_{DS} = 10V, 30V, 50V, operating at ambient temperature of 100C, 150C, and 200C. Different from that in the Si DMOS device, in the area away from the surface region, the electron density distribution is uniform and smaller than its doping density. This is due to a much larger critical electric field in 6H-SiC– in the vertical substrate direction, the velocity of travelling electrons is difficult to reach its saturated velocity. In addition, due to a smaller $E_{fn} - E_D$, incomplete ionization of donors exists in the substrate region of the 6H-SiC DMOS device. As shown in the figure, ionization of donors increases at a higher temperature.

References

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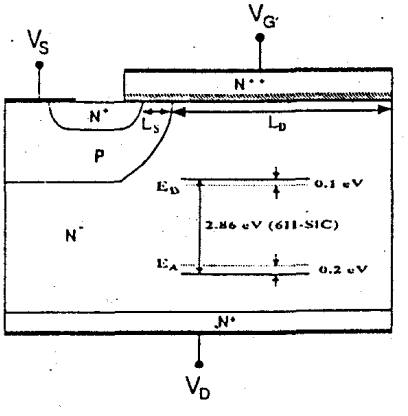

Fig. 1. Cross section of the 6H-SiC DMOS Device.

$$E_g = 2.86 - 3.3 \times 10^{-4}(T - 300K) \quad eV \qquad (1)$$

$$n_i = \sqrt{N_c N_v}\, exp(-\frac{E_g}{kT}) \qquad (2)$$

$$N_c = 2.5 \times 10^{19}(\frac{T}{300K})^{1.5} \quad cm^{-3}$$

$$N_v = 2.5 \times 10^{19}(\frac{T}{300K})^{1.5} \quad cm^{-3}$$

$$\frac{N_D^+}{N_D} = \frac{1}{1 + 2exp(\frac{E_{F_n} - E_D}{kT})} \qquad (3)$$

$$\epsilon_{sic} = 9.66 \qquad (4)$$

$$v_{sat} = 2 \times 10^7 (\frac{T}{300K})^{-0.87} \quad cm/s \qquad (5)$$

$$\mu_n = 20 + \frac{380}{1 + (\frac{N_D}{4.5 \times 10^{17}})^{0.45}} (\frac{T}{300K})^{-3} cm^2/Vs \qquad (6)$$

$$\mu_{neff} = \mu_n (\frac{1}{1 + (\frac{E_{ps}}{v_{sat}})^2})^{\frac{1}{2}} \qquad (7)$$

Fig. 2. Important device models for 6H-SiC.

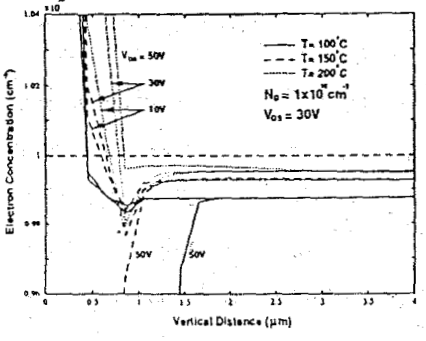

Fig. 4. The electron density profiles in the vertical direction at the right side of the 6H-SiC DMOS device, biased at $V_{GS} = 30V$ and $V_{DS} = 10V, 30V, 50V$, operating at ambient temperature of 100C, 150C, and 200C.

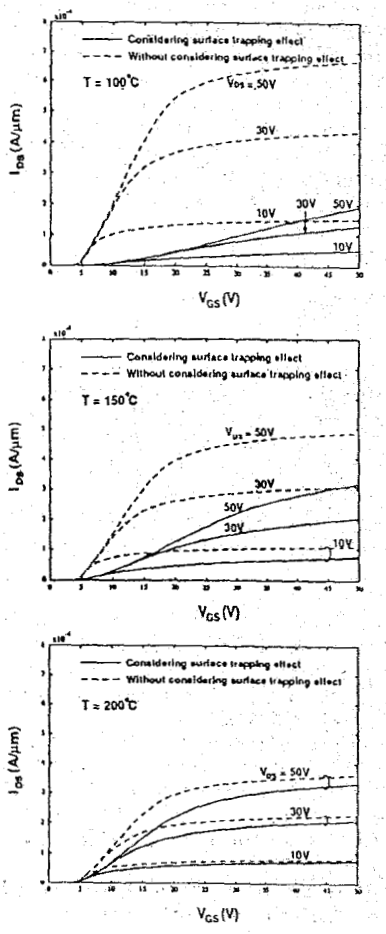

Fig. 3. The I_D vs. V_{GS} curves of the 6H-SiC DMOS device biased at $V_{DS} = 10V, 30V, 50V$, operating at an ambient temperature of 100C, 150C, and 200C.