Characterization of Asymmetrical Half Bridge Flyback Converter

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Abstract – Flyback derived converters are attractive because of their simple capacitive output filter when compared with other converters used in multiple-output or cost-sensitive applications. This paper analyzes the detailed circuit behavior of the asymmetrical half bridge flyback converter. Several practical issues, including the specific relationships between the duty cycle and the different types of energy in the energy-storage elements, and the zero voltage switching (ZVS) conditions of the power switches have been thoroughly examined. Mathematical equations have also been given. A 5V/20A prototype has been built to verify the analytical results.

I. INTRODUCTION

The conventional flyback converter is attractive where multiple-output or cost-sensitive applications are concerned, thanks to its simple capacitive output filter. Nevertheless, hard switching operation of the power switch results in high switching loss, high EMI noises, and high switch voltage stress. Various kinds of soft switching techniques have been proposed for flyback converters [1-8]. Among them, the resonant converter [1-2], the active-clamp circuit [3-5], and the asymmetrical half bridge converter are probably the most well known converters. Resonant converter can reduce the switching losses and EMI noises. However, the voltage and/or current stresses increase and result in high conduction losses. Incorporation of active clamp network provides the benefit of ZVS operation of the power switches in the active clamp flyback converter [3-5]. However, the drawback that we will have to bear is the high voltage stresses on the power switches.

The asymmetrical half bridge flyback converter, which can achieve ZVS operations of the power switches, is gaining popularity. The switch voltage stresses are no more than the input voltage can be achieved. In the previous works [6-8], the role of the blocking capacitor in the process of energy storing has been overlooked. When only the magnetic components are being considered as the energy-storage elements in the studied converter, a 50% duty cycle constraint has been derived [8]. However, in the present paper, it has been proved that the 50% duty cycle constraint does not occur. This is because the blocking capacitor also stores energy when the output rectifier is off. The specific relationships between the duty cycle and the various types of energy in the energy-storage elements have been examined in depth.

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Fig. 1 shows the simplified circuit diagram of the asymmetrical half bridge flyback converter. The ZVS conditions for the power switches, *S1* and *S2*, have not yet been discussed before. In fact, the ZVS mechanisms of them are quite different. One of them is just a linear charging process. The ZVS operation of this power switch, *S2*, can be maintained simply when there is a sufficiently long dead time between *S1* and *S2*. However, the ZVS operation of the other switch, *S1*, is achieved only when the energy stored in the resonant inductor is greater than that of the output capacitors of these power switches.

A 5V/20A prototype has been built to verify the analytical results. With the assistance of the given design equations, the power switches can maintain ZVS from no-load to full-load situations.

II. STEADY-STATE OPERATION

Fig. 1 shows the simplified circuit diagram of the asymmetrical half bridge flyback converter. The inductor L_r denotes the combination of the leakage inductance of T_X and the external inductor. To describe the basic operational principles, several assumptions are made.

- The converter has reached a steady-state operation.
- L_r is much less than L_M.
- The resonant period of C_b and L_r is much greater than the off time of *S1*.

To facilitate the analysis of the asymmetrical half bridge flyback converter, Fig. 2 and Fig. 3 show the seven topological stages of the converter during a switching cycle and its key waveforms, respectively. The operations of this converter can be explained as follows:

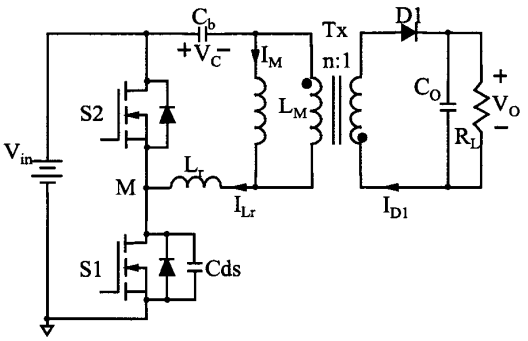

Fig. 1. Simplified schematic of the asymmetrical half bridge flyback converter.

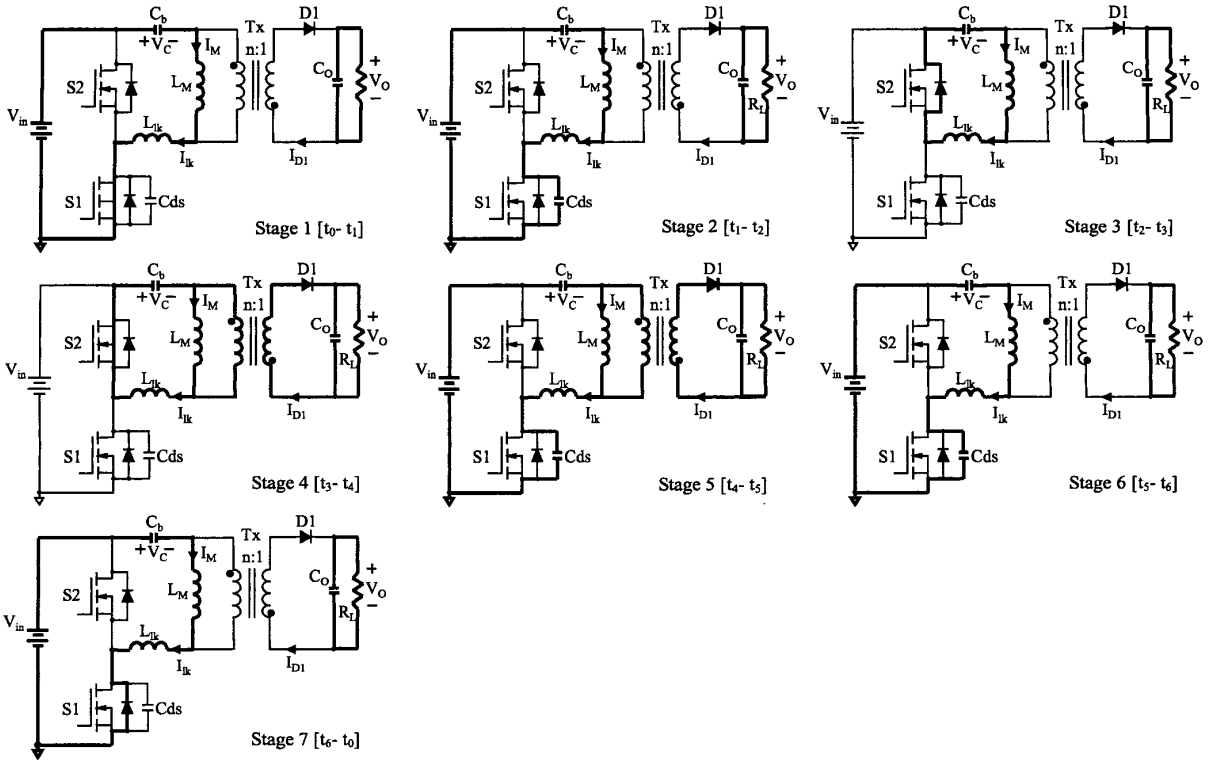

Fig. 2. Asymmetrical half bridge flyback converter topological states.

Stage 1 [t_0-t_1]: At t_0, *S1* is on and *S2* is off. *D1* is reversed biased in this stage. The dc input power source charges C_b, L_M, and L_r. The charge time is brief compared with the time constant of this resonant tank, leading to an approximately linear charging characteristic. The following equations can be obtained:

$$(L_M + L_r)\frac{di_{Lr}}{dt} = V_{in} - v_C \tag{1}$$

$$C_b \frac{dv_C}{dt} = i_{Lr} = i_M . \tag{2}$$

After solving (1) and (2), we have:

$$i_{Lr}(t) = \frac{V_{in} - v_C(t_0)}{Z_1}\sin[\omega_{r1}(t-t_0)] + i_{Lr}(t_0)\cos[\omega_{r1}(t-t_0)] \tag{3}$$

$$v_C(t) = V_{in} - [V_{in} - v_C(t_0)]\cos[\omega_{r1}(t-t_0)] + i_{Lr}(t_0)Z_1\sin[\omega_{r1}(t-t_0)] \tag{4}$$

where $Z_1 = \sqrt{\frac{L_M + L_r}{C_b}}$ and $\omega_{r1} = \frac{1}{\sqrt{C_b(L_M + L_r)}}$. This stage ends when *S1* turns off.

Stage 2 [t_1-t_2]: C_b, L_M, L_r, and C_{ds} form a new resonant network after *S1* turns off at $t = t_1$. C_{ds}, which is the equivalent capacitance at point M, is charged by the current of L_r. In this stage, the state equations can be written as follows:

$$(L_M + L_r)\frac{di_{Lr}}{dt} = V_{in} - v_C - v_{ds} \tag{5}$$

$$C_b \frac{dv_C}{dt} = i_{Lr} = i_M \tag{6}$$

$$C_{ds} \frac{dv_{ds}}{dt} = i_{Lr} = i_M . \tag{7}$$

Solving (5) - (7) gives:

$$i_{Lr}(t) = \frac{V_{in} - v_C(t_1)}{Z_2}\sin[\omega_{r2}(t-t_1)] + i_{Lr}(t_1)\cos[\omega_{r2}(t-t_1)] \tag{8}$$

$$v_C(t) = [V_{in} - v_C(t_1)]\frac{C_b // C_{ds}}{C_b}\{1 - \cos[\omega_{r2}(t-t_1)]\} + \frac{i_{Lr}(t_1)}{\omega_{r2}C_b}\sin[\omega_{r2}(t-t_1)] + v_C(t_1) \tag{9}$$

$$v_{ds}(t) = [V_{in} - v_C(t_1)]\frac{C_b // C_{ds}}{C_{ds}}\{1 - \cos[\omega_{r2}(t-t_1)]\} + \frac{i_{Lr}(t_1)}{\omega_{r2}C_{ds}}\sin[\omega_{r2}(t-t_1)] \tag{10}$$

where $Z_2 = \sqrt{\frac{LM + L_r}{C_b // C_{ds}}}$ and $\omega_{r2} = \frac{1}{\sqrt{(C_b // C_{ds})(L_M + L_r)}}$.

This stage ends when the antiparallel diode of *S2* starts to conduct.

Stage 3 [t_2-t_3]: After the antiparallel diode of *S2* starts to conduct at t_2, C_b resonates with L_r and L_M. The voltage across L_M decreases. Before the current of L_r changes direction, *S2* can be turned on under ZVS.

In this stage, the current of L_r charges C_b. The voltage across C_b increases due to the transfer of the energy from L_r and L_M. The state equations can be written as follows:

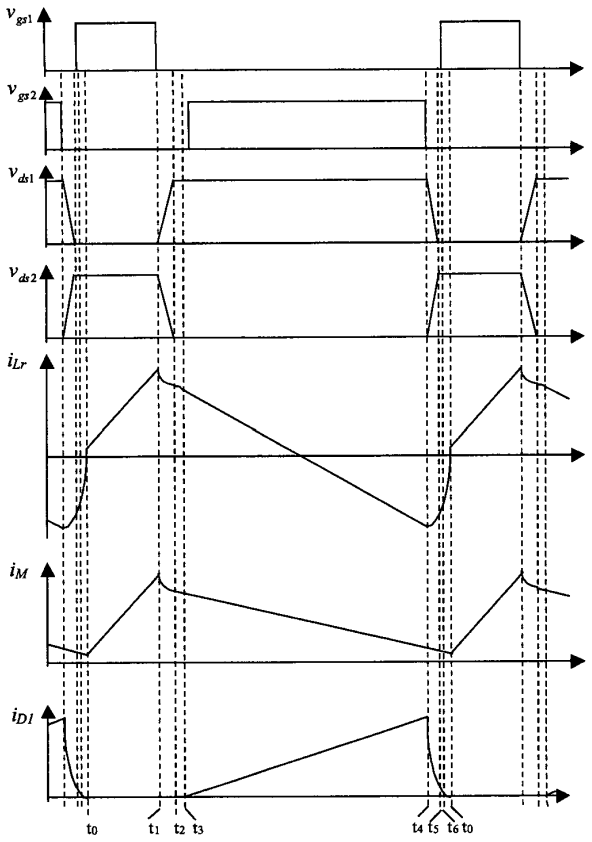

Fig. 3. Steady state waveforms of the asymmetrical half bridge flyback converter.

$$(L_M + L_r)\frac{di_{Lr}}{dt} = -v_C \tag{11}$$

$$C_b\frac{dv_C}{dt} = i_{Lr}. \tag{12}$$

Solving (11) and (12), we have:

$$i_{Lr}(t) = -\frac{v_C(t_2)}{Z_1}\sin[\omega_{r1}(t-t_2)] + i_{Lr}(t_2)\cos[\omega_{r1}(t-t_2)] \tag{13}$$

$$v_C(t) = v_C(t_2)\cos[\omega_{r1}(t-t_2)] + i_{Lr}(t_2)Z_1\sin[\omega_{r1}(t-t_2)]. \tag{14}$$

Stage 4 [t_3-t_4]: After the output rectifier starts to conduct at t_3, i_{D1} is the difference between i_M and i_{Lr} multiplying by the turns ratio of T_X. The state equations can be written as follows:

$$L_M\frac{di_M}{dt} = -nV_O \tag{15}$$

$$L_r\frac{di_{Lr}}{dt} = -v_C + nV_O \tag{16}$$

$$C_b\frac{dv_C}{dt} = i_{Lr}. \tag{17}$$

Solving (15) - (17) yields:

$$i_M(t) = i_M(t_3) - \frac{nV_O}{L_M}(t-t_3) \tag{18}$$

$$i_{Lr}(t) = \frac{nV_O - v_C(t_3)}{Z_3}\sin[\omega_{r3}(t-t_3)] + i_{Lr}(t_3)\cos[\omega_{r3}(t-t_3)] \tag{19}$$

$$v_C(t) = nV_O - [nV_O - v_C(t_3)]\cos[\omega_{r3}(t-t_3)] + i_{Lr}(t_3)Z_3\sin[\omega_{r3}(t-t_3)] \tag{20}$$

where $Z_3 = \sqrt{\frac{L_r}{C_b}}$ and $\omega_{r3} = \frac{1}{\sqrt{C_b L_r}}$.

Stage 5 [t_4-t_5]: *S2* turns off at t_4. The current of L_r discharges C_{ds}, and V_{ds} decreases. This stage ends when the antiparallel diode of *S1* starts to conduct at t_5. The output rectifier still conducts at t_5 because the resonant inductor limits the discharging rate of i_{Lr}. The state equations can be written as follows:

$$L_M\frac{di_M}{dt} = -nV_O \tag{21}$$

$$L_r\frac{di_{Lr}}{dt} = V_{in} - v_C + nV_O - v_{ds} \tag{22}$$

$$C_b\frac{dv_C}{dt} = i_{Lr} \tag{23}$$

$$C_{ds}\frac{dv_{ds}}{dt} = i_{Lr}. \tag{24}$$

Solving (21) - (24) yields:

$$i_M(t) = i_M(t_4) - \frac{nV_O}{L_M}(t-t_4) \tag{25}$$

$$i_{Lr}(t) = \frac{-v_C(t_4) + nV_O}{Z_4}\sin[\omega_{r4}(t-t_4)] + i_{Lr}(t_4)\cos[\omega_{r4}(t-t_4)] \tag{26}$$

$$v_C(t) = [-v_C(t_4) + nV_O]\frac{C_b // C_{ds}}{C_b}\{1-\cos[\omega_{r4}(t-t_4)]\} + \frac{i_{Lr}(t_4)}{\omega_{r4}C_b}\sin[\omega_{r4}(t-t_4)] + c_v(t_4) \tag{27}$$

$$v_{ds}(t) = [-v_C(t_4) + nV_O]\frac{C_b // C_{ds}}{C_{ds}}\{1-\cos[\omega_{r4}(t-t_4)]\} + \frac{i_{Lr}(t_4)}{\omega_{r4}C_{ds}}\sin[\omega_{r4}(t-t_4)] + V_{in} \tag{28}$$

where $Z_4 = \sqrt{\frac{L_r}{C_b // C_{ds}}}$ and $\omega_{r4} = \frac{1}{\sqrt{(C_b // C_{ds})L_r}}$.

Stage 6 [t_5-t_6]: At t_5, V_{ds} has dropped to zero and the antiparallel diode of *S1* is conducted. Before i_{Lr} changes direction, *S1* can be turned on under ZVS. The equations describing the circuit operation during this stage are as follows:

$$L_M\frac{di_M}{dt} = -nV_O \tag{29}$$

$$L_r\frac{di_{Lr}}{dt} = V_{in} - v_C + nV_O \tag{30}$$

$$C_b\frac{dv_C}{dt} = i_{Lr}. \tag{31}$$

Solving (29) - (31), we can obtain:

$$i_M(t) = i_M(t_5) - \frac{nV_O}{L_M}(t-t_5) \tag{32}$$

$$i_{Lr}(t)=\frac{V_{in}-v_C(t_5)+nV_O}{Z_3}\sin[\omega_{r3}(t-t_5)]+i_{Lr}(t_5)\cos[\omega_{r3}(t-t_5)] \quad (33)$$

$$v_C(t)=[V_{in}-v_C(t_5)+nV_O]\{1-\cos[\omega_{r3}(t-t_5)]\}+i_{Lr}(t_5)Z_3\sin[\omega_{r3}(t-t_5)]+v_C(t_5) \quad (34)$$

Stage 7 [t_6-t_0]: At t_6, *S1* turns on under ZVS. The resonant inductor current i_{Lr} increases rapidly. This stage ends when this current increases to the point where the output rectifier cuts off. The dc input power source begins to charge C_b, L_r, and L_M again. Another switching cycle starts.

III. ANALYSIS

According to the above analysis, this section will quantitatively analyze the key characteristics of this converter.

A. Energy-storage elements: The energy-storage elements in this converter consist of the blocking capacitor, the magnetizing inductor of T_X, and the resonant inductor.

Fig. 4 shows the simplified waveforms of the voltage across the blocking capacitor and the current of the resonant inductor. During the interval DT_S, the dc input power source charges C_b, L_M, and L_r, causing the increments in the voltage across C_b as well as the current of L_M and L_r. Energy stored in these elements can be expressed as:

$$E_{LM}+E_{Lr}=\frac{1}{2}(L_M+L_r)\left[{I_{Lr}}^2(DT_S)-{I_{Lr}}^2(0)\right] \quad (35)$$

$$E_{C_b}=\frac{1}{2}C_b\left[{V_{C_b}}^2(DT_S)-{V_{C_b}}^2(0)\right]. \quad (36)$$

The incremental voltage across C_b for this duration can be expressed as:

$$V_{C_b}(DT_S)-V_{C_b}(0)=\frac{1}{C_b}\int_0^{DT_S}i_{Lr}(t)dt=\frac{1}{C_b}\frac{I_O}{n}DT_S \quad (37)$$

$$I_{Lr}(DT_S)-I_{Lr}(0)=\frac{1}{L_M+L_r}\int_0^{DT_S}(V_{in}-v_c(t))dt=\frac{1}{L_M+L_r}\left(\frac{2V_{in}-V_{C_b}(DT_S)-V_{C_b}(0)}{2}\right)DT_S. \quad (38)$$

Inserting (38) into (35) yields:

$$E_{LM}+E_{Lr}=\frac{1}{2}\frac{I_O}{n}DT_S\left[2V_{in}-\left(V_{C_b}(DT_S)+V_{C_b}(0)\right)\right]. \quad (39)$$

Combining (36) and (37), we can obtain:

$$E_{C_b}=\frac{1}{2}\frac{I_O}{n}DT_S\left[V_{C_b}(DT_S)+V_{C_b}(0)\right] \quad (40)$$

From (39) and (40), the total energy stored during the interval DT_S is

$$E_{LM}+E_{Lr}+E_{C_b}=\frac{I_O}{n}DT_SV_{in}=P_OT_S. \quad (41)$$

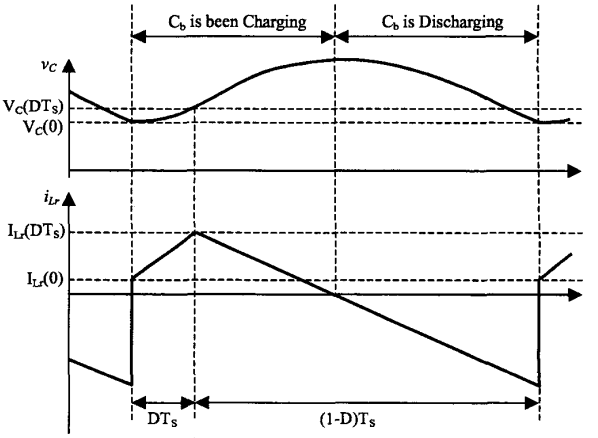

Fig. 4. Simplified waveforms of the voltage across the blocking capacitor and the current of the resonant inductor.

When the voltage ripple across the blocking capacitor is neglected, (39) and (40) can be further condensed into

$$E_{LM}+E_{Lr}\approx\frac{1}{2}\frac{I_O}{n}DT_S[2V_{in}-2V_{in}D]=P_OT_S(1-D) \quad (42)$$

$$E_{C_b}\approx\frac{1}{2}\frac{I_O}{n}DT_S(2V_{in}D)=P_OT_SD. \quad (43)$$

Equations (42) and (43) clearly describe the relationships between the amount of stored energy and the duty cycle.

During another interval $(1\text{-}D)T_S$, part of the energy stored in L_M and L_r transfers to the secondary side of T_X and the rest energy charges C_b. After the resonant inductor current changes direction, the energy stored in C_b transfers to the output capacitor via T_X.

B. ZVS condition: The ZVS mechanism of *S2* is alike a linear charging process. According to (10) in section II, the ZVS condition of *S2* can be obtained:

$$v_{ds}(t)=(V_{in}-v_C(t_1))\frac{C_b//C_{ds}}{C_{ds}}(1-\cos[\omega_{r2}(t-t_1)])+\frac{i_{Lr}(t_1)}{\omega_{r2}C_{ds}}\sin[\omega_{r2}(t-t_1)]\geq V_{in}. \quad (44)$$

For $C_b>>C_{ds}$ and $\omega_{r2}(t-t_1)$ small that $\sin[\omega_{r2}(t-t_1)]\approx\omega_{r2}(t-t_1)$ and $\cos[\omega_{r2}(t-t_1)]\approx1$, we get an approximate solution:

$$t-t_1\geq C_{ds}\frac{V_{in}}{i_{Lr}(t_1)}. \quad (45)$$

From (45), the ZVS operation of *S2* can always be maintained when a sufficiently long dead time between the two power switches is used. The required dead time to achieve ZVS operation of *S2* can be obtained by (45).

The ZVS condition of *S1* depends on the energy stored in L_r, which is quite different with *S2*. It can be obtained from (28) in section II:

$$v_{ds}(t)=(-v_C(t_4)+nV_O)\frac{C_b // C_{ds}}{C_{ds}}(1-\cos[\omega_{r4}(t-t_4)]) + \frac{i_{Lr}(t_4)}{\omega_{r4}C_{ds}}\sin[\omega_{r4}(t-t_4)]+V_{in}\le 0. \quad (46)$$

Owing to the angular frequency, ω_{r4}, is much bigger than ω_{r2}, we cannot assume that $1-\cos[\omega_{r4}(t-t_4)]\approx 0$ and omit this term just like the way in the previous case. However, this term can still be omitted because its coefficient is negligible when compared with that of the other terms. Therefore, (46) can be further simplified into

$$\frac{i_{Lr}(t_4)}{\omega_{r4}C_{ds}}\sin[\omega_{r4}(t-t_4)]+V_{in}\le 0 \quad (47)$$

We can rearrange (47) to give

$$\sin[\omega_{r4}(t-t_4)]\le -\frac{V_{in}}{i_{Lr}(t_4)}\omega_{r4}C_{ds}. \quad (48)$$

Solving (48), the ZVS condition of *S1* can be obtained:

$$\frac{1}{2}L_r i_{Lr}(t_4)^2 \ge \frac{1}{2}C_{ds}V_{in}^2. \quad (49)$$

From (49), the ZVS condition of *S1* depends on the energy stored in L_r.

IV. Experimental Results

To experimentally characterize the circuit behavior of the studied converter, a prototype was built to the specifications listed below:

- input voltage V_{in}: 400 Vdc;
- output voltage V_O: 5 Vdc;
- maximum load current: 20 A;
- switching frequency f_S: 60 kHz;
- ZVS range: 0% to 100% load.

The power stage consists of the following parameters:

- switches *S1* and *S2*: Toshiba 2SK2842;
- diode *D1*: 2×Toshiba 30GWJ2C42C;
- blocking capacitor C_b: 3.3uF/250V;
- input capacitor: 68uF/450V;
- Transformer:
  A_e of core: 1cm^2;
  primary: 36 turns of litz wire 20×0.1mm;
  secondary: 3 turns of litz wire 100×0.1mm;
  L_M: 280 uH, L_{lk}: 8 uH;
- resonant inductance, L_r : 18 uH
  (includes L_{lk} and an external inductance);
- dead time: 100us
  (between the turn-off of *S1* and turn-on of *S2*);

Some key experimental waveforms are shown in Fig. 5. These waveforms resemble closely those shown in Fig. 3. The ZVS operations of *S1* and *S2* can be noted form the waveforms shown in Fig. 6. From Fig. 6(a) and 6(c), the converter remains ZVS operations of *S1* and *S2* even under no load condition. The efficiency of the prototype is plotted in Fig. 7.

V. Summary

From the analytical and experimental results, several circuit features have been observed as follows:

A. Not only the magnetizing inductor of the transformer and the resonant inductor, but also the blocking capacitor store energy when the output rectifier is off. When the duty cycle increases, the energy stored in the blocking capacitor will also increase accordingly. However, the energy stored in the magnetizing inductor and the resonant inductor will decrease. Most of the energy is stored in the blocking capacitor when the duty cycle exceeds 50%.

B. The ZVS conditions of these two power switches are quite different. The ZVS operation of *S2* can always be maintain when a sufficiently long dead time between *S1* and *S2* is used. However, *S1* achieves ZVS only when the energy stored in L_r is larger than that of C_{ds}.

This paper describes the circuit behavior of the asymmetrical half bridge flyback converter. A detail analysis and mathematical equations have been given. A 5V/20A prototype has been built to verify the analytical results. The experimental results show that the power switches can maintain ZVS operations from no-load to full-load and that the efficiency can reach an optimum value of 80%.

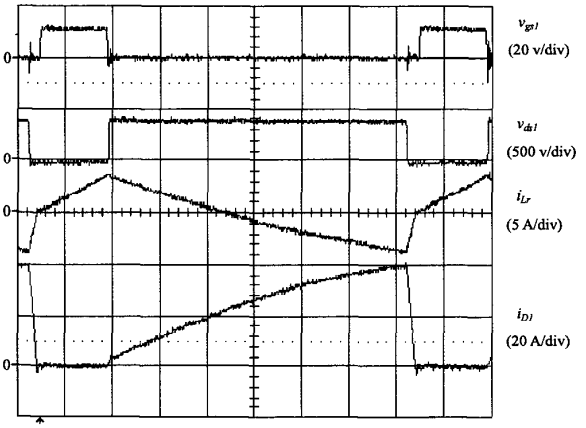

Fig. 5. Experimental waveforms. (Time scale is 2 us/div)

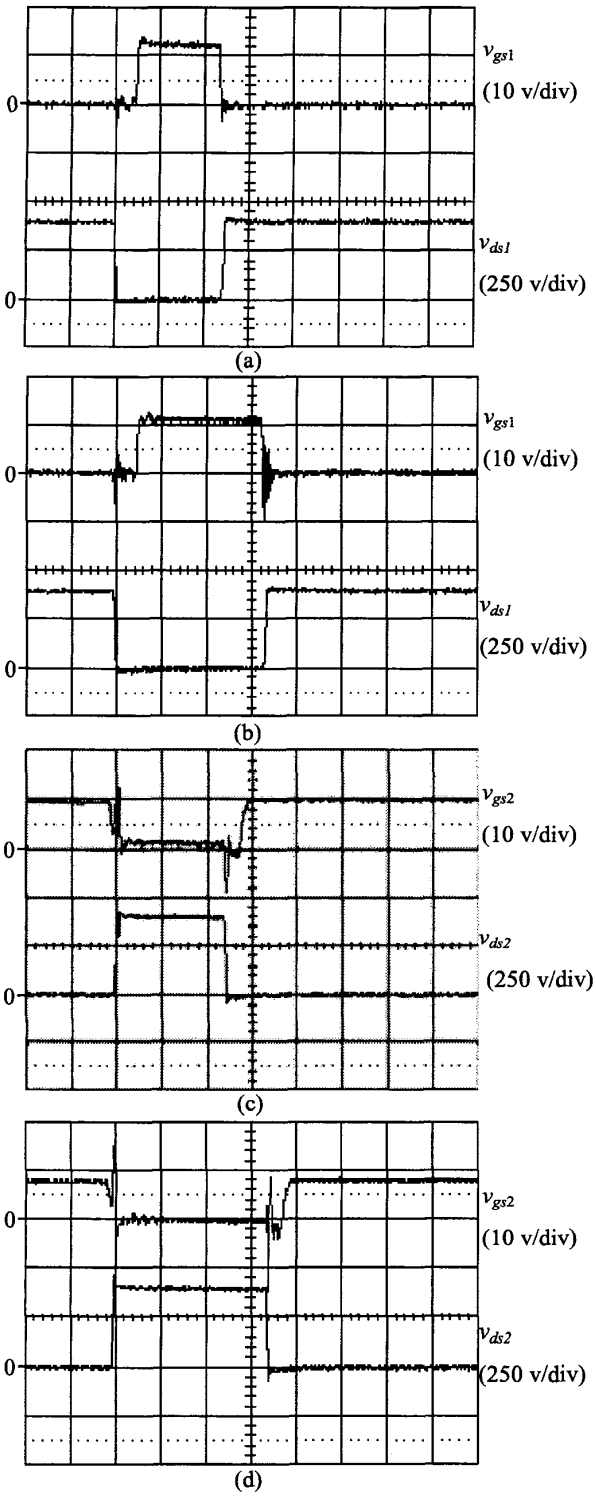

Fig. 6. Experimental ZVS waveforms. (Time scale is 1 us/div)
(a) S1 at no load; (b) S1 at full load; (c) S2 at no load ;(d) S2 at full load.

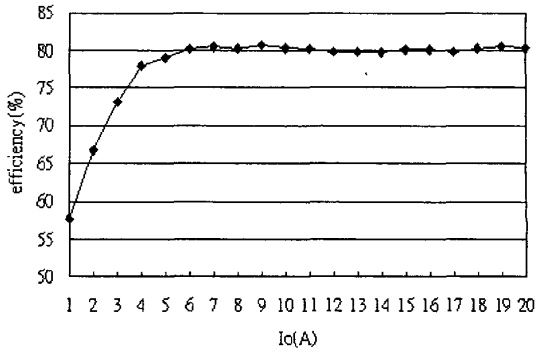

Fig. 7. Measured efficiency of the prototype. (V_{in} = 400v, V_o = 5v)

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