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Network Synchronization of an Orthogonal CDMA Satellite Communication System

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Abstract. This paper provides the network synchronization of an orthogonal CDMA geostationary satellite system for fixed service communications. It includes the synchronization procedures, the system architecture and the performance evaluation. The main objective is to provide network wide synchronization of all uplink orthogonal CDMA transmissions. This is achieved in steps; first by providing coarse synchronization using the uplink random access channel and then fine sync using innovative tracking control mechanisms. The uplink access channel receiver utilize a parallel/serial search method for rapid code acquisition, while the code tracking of the uplink orthogonal CDMA traffic channel is based on a delay feedback early-late gate in which the sych control resides in the receiver. The proposed system is designed to minimize the onboard complexity and satisfy the performance requirements. As shown in the performance section, the requirement that all uplink transmissions are synchronized to a reference time within 10% of the chip length can be achieved. In addition, the system analysis determines the design parameters values which optimize performance.

Keywords: Network synchronization, Orthogonal CDMA, Satellite communications

1. Introduction

Future geostationary satellite systems are expected to offer direct two-way communications between end satellite users having ultra small aperture terminals. Such service requires high system capacity, low bit error rates and low signal-to-noise ratio. These requirements can be achieved with a Satellite Switched CDMA (SS/CDMA), proposed in [1] and evaluated in [2]. The SS/CDMA uses orthogonal CDMA in both uplink and downlink. The orthogonal CDMA can reject the interference between the user Traffic channels and thus maximize the system capacity. However, the use of orthogonal CDMA in the uplink, requires a network wide synchronization of all satellite transmissions (global synchronization). The accuracy of the synchronization at steady-state and the speed at which synchronization is acquired depends on the propagation environment i.e., the channel condition, the mobility of the end user, the propagation delay, etc. There are several examples in which synchronous CDMA (orthogonal or quasi-orthogonal) attempted for use in the uplink or inbound channel. One such example is presented in reference [3] in which synchronous CDMA is proposed for mobile satellite applications. In another example presented in reference [4], orthogonal CDMA is recommended for the inbound and outbound links in terrestrial wireless applications. In this reference also shown (by simulation) that the required synchronization jitter from a reference time should

not exceed 10% of the chip length for orthogonal CDMA operation. This requirement can be achieved easily if the CDMA system has relatively narrow band and low user mobility. One such system presented in reference [5], has chip rate 0.65 Mc/s (or chip length $T_c = 1.538\,\mu$ s, corresponding to a propagation distance of 460 m) and the cell radius is 230 m. The synchronization subsystem to meet the above requirement may then be simple. On the other hand a wideband orthogonal CDMA requires substantial effort in acquiring and maintaining synchronization, especially in mobile environment. The above referenced systems however, only assume that a synchronization subsystem is in place without presenting one. In this paper we provide the procedures and the system design which can achieve synchronization in a goestationary satellite orthogonal CDMA for fixed service communications.

As described in [1], the multibeam satellite common interface provides Signaling control and user Traffic channels within each satellite beam. The control channels are used for the acquisition of the user Traffic channel. The downlink control channels are, the Pilot, Sync and Paging broadcast channels and are defined by PN-code and orthogonal codes. In the uplink there is an asynchronous Access channel which has an assigned beam PN-code. The Access channel operation is based on a spread-spectrum random access (SSRA) protocol described in the next section. The Traffic channels are defined by the user orthogonal code and the beam orthogonal and/or PN codes.

The network synchronization basically consists of the initial acquisition of the satellite downlink control channels, the Access channel code acquisition, the system wide synchronization of all Traffic channels and the process of retaining and tracking the network sync once it has achieved. Since in general, uplink transmissions are asynchronous, the main part of this process is the synchronization of all uplink Traffic channels. This is required in order to align all uplink orthogonal codes to a reference time upon arrival at the satellite despreaders and thus provide orthogonality between the Traffic channels. This alignment however may not be ideal but it is required that the time offset of each signal from the reference time does not exceed 10% of the chip length, see [4]. The factors which prohibit perfect synchronization include the long satellite propagation delay, the propagation delay variation due to satellite slow drift motion as well as channel conditions such as rain fade etc. The synchronization system has also to consider that the complexity of the onboard signal processing is limited by the available mass and power of the spacecraft.

The proposed synchronization system although is designed and evaluated for this particular application may also be adapted and used in other application (terrestrial or satellite) which have orthogonal CDMA for uplink access. Limited user mobility may also be allowed, depending on the CDMA spreading rate and the properties of the codes used. A particular set of quasi-orthogonal codes are may be less sensitive to alignment jitter. For example, preferentially phased Gold codes may allow timing jitter of up to 50% of the chip length.

The system evaluation is focused on the performance of the Access channel code acquisition and the performance of the tracking control loop. The Access channel, based on a spread spectrum random access protocol, carries control messages from the end user to the satellite while at the same time provides the timing delay (PN phase offset) of the user code for the purpose of synchronizing the uplink orthogonal codes of the Traffic channel. The proposed code acquisition is a serial/parallel scheme adjusted to meet the packet delay requirements. Related work on the subject is found in references [6] and [7]. The analysis of the tracking loop examines the loop stability and its steady state error. Related work can be found in references [8] and [9]. The proposed loop however, is quite different since its tracking part resides in the

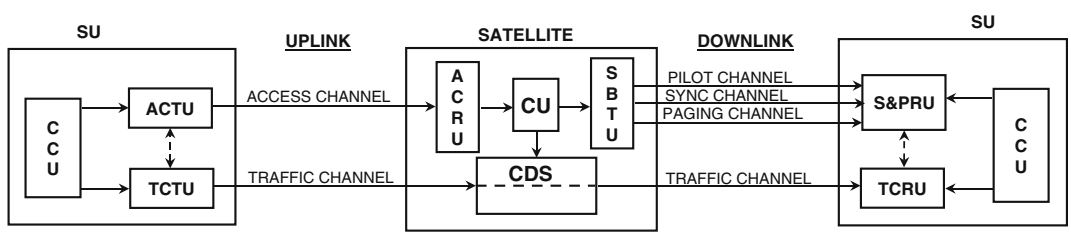
satellite receiver while the control part in the user's transmitter. Thus, the tracking loop model also includes the satellite propagation delay.

This paper is organized as follows: The synchronization procedures and the system design are presented in the next section. In Section 3 we provide the system performance evaluation. The performance analysis for the Access channel and the tracking loop are presented in Appendices A and B respectively.

2. System Description

The system architecture of the satellite switched CDMA system is illustrated in Figure 1. The satellite common interface provides control channels (Access in the uplink and Pilot, Sync and Paging in the downlink) and Traffic channels. The Traffic channels are based on orthogonal CDMA and provide direct links between the end subscriber units (SUs) without onboard decoding. The control channel provide the communication links between the satellite and the SUs and are used for both signaling and synchronization purposes. Control channels have an assigned frequency band different from the bands assigned to Traffic channels. The spreading bandwidth of all bands is the same.

In describing the synchronization procedures of the system we first identify the PN and orthogonal codes of each channel that we use in the process. These codes are: The PN code $g_{\mathrm{p}}(t)$ defining the downlink pilot signal which has rate R_{c} and is transmitted continuously in the frequency band of the downlink control channels ($g_{\mathrm{p}}(t)$ is transmitted with given phase offset Δ_i corresponding to satellite beam i). The uplink Access channel in beam i is identified by the PN code $a_i(t)$, has a chip rate R_{c} and operates in an assigned frequency band. Traffic channels are defined by the user orthogonal codes W_k $(k = 1, 2, \ldots)$. the beam PN-codes $g_i(t)$ $(i - 1, 2, \ldots)$ and the beam orthogonal codes W_i $(i = 1, 2, 3, 4)$. The Traffic channel spreading operation shown in Figure 2. The codes W_i having chip rate $R_{\mathrm{c}} = 4R_{\mathrm{c1}}$, provide orthogonal isolation between four adjacent beams. Beam PN-code g_i and user orthogonal code W_k have rate R_{c1}. All uplink Traffic Channels codes are required to arrive synchronously at the satellite despreaders in order to maintain the orthogonality between users within the beam as well as between beams. That is, the starting time of all orthogonal codes should be aligned upon arriving at the satellite despreader.



ACRU: Access Channel Receiver Unit
ACTU: Access Channel Transmitter Unit
CCU: Call Control Unit
CDS: Code Division Switch
CU: Control Unit
SBTU: Satellite Broadcast Transmitter Unit
S&PRU: SYNC & Paging Receiver Unit
SU: Subscriber Unit
TCTU: Traffic Channel Transmitter Unit
TCRU: Traffic Channel Receiver Unit

Figure 1. The SS/CDMA system architecture.

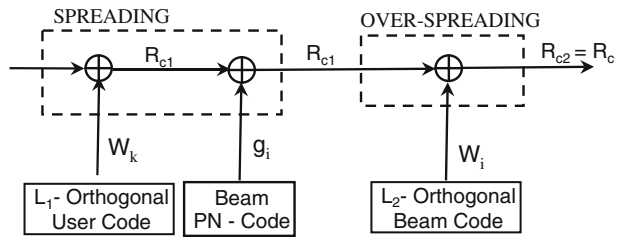


Figure 2. The spreading operation in the Traffic channel.

2.1. The Synchronization Procedure

The process that provides network wide synchronization consist of a number of steps described bellow:

1. *Initial Synchronization*: Upon Power-On the SU acquires synchronization to the Pilot PN sequence using the serial search acquisition circuit in the Sync and Paging receiver unit (S&PRU). See Figure 1. The S&PRU in the SU will then acquires the corresponding Sync channel in the beam. Based on the system information supplied by the Sync channel the SU will receive the orthogonal code W_i of the Paging channel (in the downlink) and the PN code a_i of the corresponding Access channel (in the uplink). The SU then acquires and monitors the Paging channel.
2. *Access Channel Acquisition*: The SU will then make an access attempt in the Access channel. The first message transmitted by the SU_{ki} (SU k in beam i) and received successfully at the ACRU will be used to establish the time delay (phase offset) $\Delta\tau_{ki}$ from the reference arrival time (τ_o). i.e., $\Delta\tau_{ki} = \tau_{ki} - \tau_o$. This message may arrive at the satellite despreader at any possible phase offset of the sequence $a_i(t)$. An array of K parallel Access Channel Detection Circuits (ACDC) are then used to cover all phase offsets of the code a_i (as described in Section 3) in order to acquire and despread the code. $\Delta\tau_{ki}$ may provide a resolution of T_c (one chip length), $T_c/2$, $T_c/4$ (T_c/ℓ is called chip cell, $\ell = 1, 2,$ or 4); That is, $\Delta\tau_{ki} = x_{ki}T_c/4$. The value of $\Delta\tau_{ki}$ will then be sent back to the SU via a Paging channel.
3. *Traffic Channel Acquisition*: The SU will use the value of $\Delta\tau_{ki}$ to establish Coarse Synchronization to the satellite Reference Arrival Time. This is done by advancing (or delaying) x_{ki} chip cells the starting point of the code from its original position at the successful message transmission. Then, the SU aligns each orthogonal and PN code of the uplink Traffic channel to the code a_i and begins transmission. (The traffic channel orthogonal and PN codes W_k, W_i, g_i in the uplink, and W_ℓ, W_j, g_j in the downlink, are supplied to the SU by the onboard control unit.)
4. *Fine Sync Control*: After the SU begin transmitting on the Traffic channel a feedback Tracking Loop will provide fine alignment of the uplink codes with the reference arrival time at the satellite despreaders. This feedback loop extends between the satellite to the SU and is described in detail in Section 2.2. Its transient and steady state response is derived analytically in Section 3.
5. *Sync Retention Control*: After steady state has been reached, another Sync control circuit will be used to retain the fine Sync attained in the previous step. This circuit consist of the downlink (Traffic channel) Tracking circuit and uplink SYNC control described in Section 2.2.

2.2. The System Design

In step 1 of the above procedure, the synchronization requirements to the Sync and Paging receiver unit (S&PRU) are provided by the Pilot PN code which is acquired using a serial search acquisition circuit (in the S&PRU). (The Pilot PN-code is a common cover (beam) code for all other downlink control channels which are defined with known orthogonal codes).

In step 2 of the procedure, the Access channel provides coarse synchronization for the orthogonal uplink Traffic channel. This is an additional function of the Access channel which comes at no extra cost. Its main function is to provide access for call set-up signaling messages. The Access channel operates as an asynchronous random access channel. Its transmissions obey the *Spread Spectrum Random Access* (SSRA) protocol. According to SSRA, there is one PN code $a_i(t)$ for all users in beam i. Each user may begin transmitting a message at any time instant (unslotted channel). Each message consists of a preamble (containing no data) and the message information data field. The transmitted preamble signal will arrive at the receiver at any phase offset of the PN-code. Signals arriving at the receiver more than one chips apart will be distinguished and received. Messages that have (uncorrected) errors due to interference or noise will be retransmitted randomly after the time out interval, while messages that are successfully received will be acknowledged. The Access Channel Receiver Unit (ACRU) consists of a non-coherent detector, an array of parallel Access Channel Detection Circuits (ACDC) and a pool of parallel data decoders. The array of parallel ACDCs, shown in Figure 3, provide a combination of parallel with serial acquisition circuits. Each ACDC, shown in Figure 4a, searches for synchronization of the message by correlating over a window of w chips, during the message preamble. The serial search method utilize a typical double dwell algorithm shown in Figure 4b. Given L chips the length of PN code a_i, and K the number of ACDCs the window size will then be, $w = L/K$, $(1 \leq w \leq L)$. For example if $L = 1204$ chips and $K = 16$, then $w = 64$ chips. The correlation process takes place during the message preamble. The actual number of parallel ACDCs K is determined by the required length of the preamble interval. In the serial search (double dwell) method, the length of the dwell time γ_1 and γ_2 as well as the thresholds (Θ_1 and Θ_2), are determined so that the requirements for the false alarm and detection probabilities are met. Also, the Access channel is assumed to operate at low traffic load in order to offer high probability of successful message transmission with the first attempt. (See performance analysis in Section 3.1).

In step 4, the proposed mechanism for fine sync control is shown in Figure 5. It consists of the on-board SYNC Tracking circuit the downlink feedback path, the SU SYNC control circuit and uplink Traffic channel timing jitter control. The On-board tracking consist of an Early-Late gate that provides the timing jitter Z_Δ. The timing jitter value Z_Δ will be inserted in a message and sent to the CCU in the SU via the Paging channel. See Figure 6. The SU

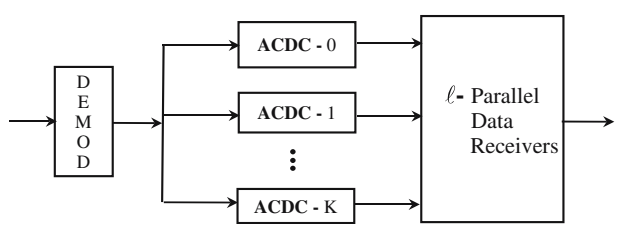


Figure 3. Array of parallel access channel detection circuits (ACDC) in the ACRU.

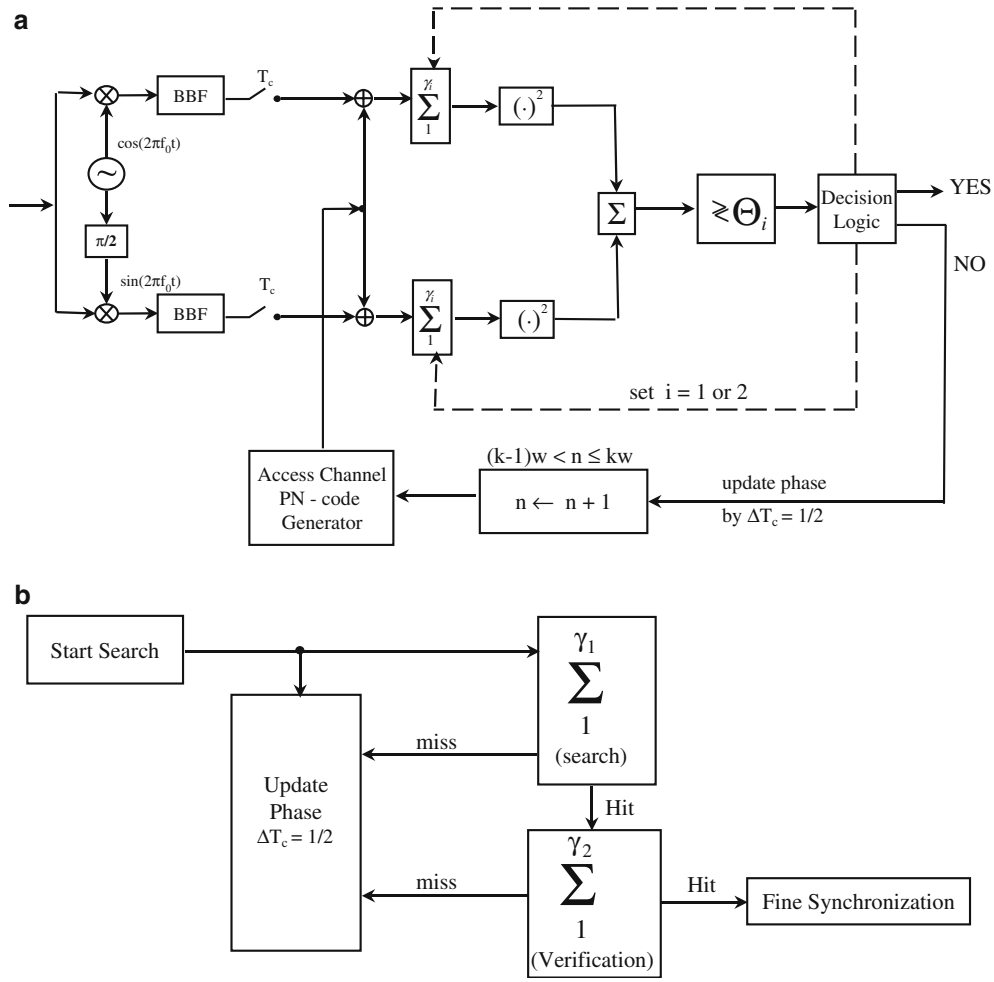


Figure 4. (a) The ACDC Implementation with double dwell serial search. (b) ACDC double dwell decision logic.

SYNC Control circuit will then take Z_Δ as input to make the timing adjustment on the uplink Traffic channel. The Early or Late despreading circuits may rely on the highest chip rate beam code W_i, i.e., $W_i(t \pm \Delta T_c)$ (The other codes g_i and W_k have chip length $T_{c2} = 4T_c$). Hence, the design of the proposed tracking loop differs from the typical one since the timing adjustment takes place at the transmitter(SU), not the receiver. This is nessassary in order to allign the transmitted orthogonal code to the reference time (at the satellite) at which all other transmissions have been alligned with. This tracking loop however introduces delays both in the feedback (downlink) as well as in the forward (uplink) path. This delay is equal to the satellite round trip propagation delays which is of about 250 ms. The delay also varies slowly because the satellite has a drift motion of about 2.5 m/s. The performance evaluation of this tracking loop have been provided in Section 3.2.

The last step of process is required in order to maintain the fine sync achieved in the previous step without making use of the the on-board sync tracking circuit. The onboard tracking circuit will become available (after a steady state is reached) for reuse in another call and thus reduce the onboard hardware. The sync retention control circuitry consists of the downlink

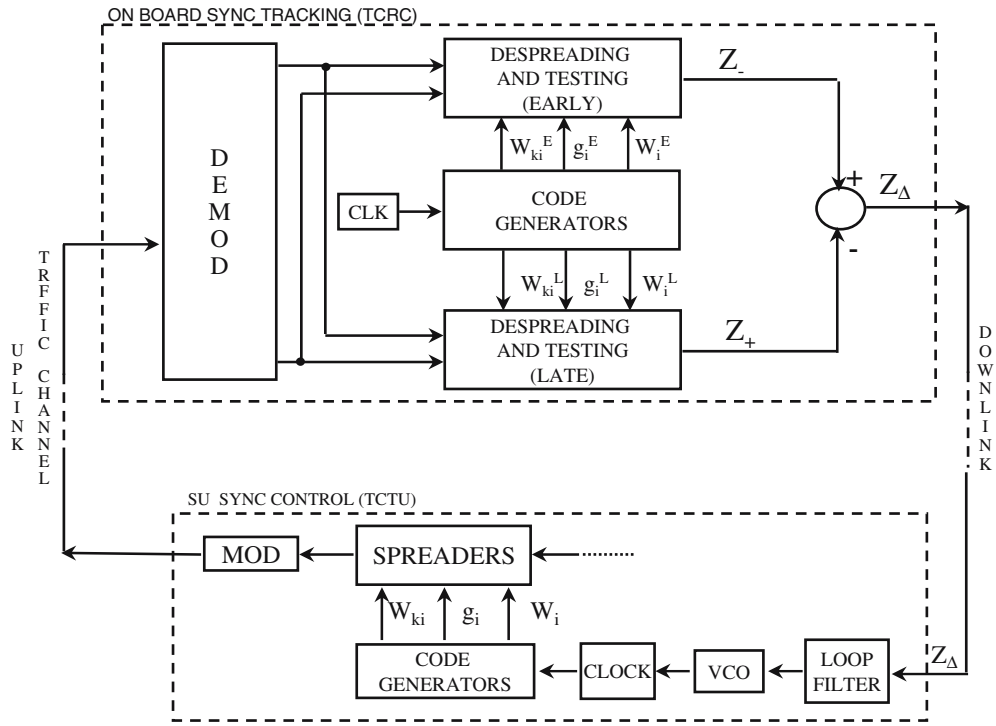


Figure 5. Sync and Tracking feedback control loop.

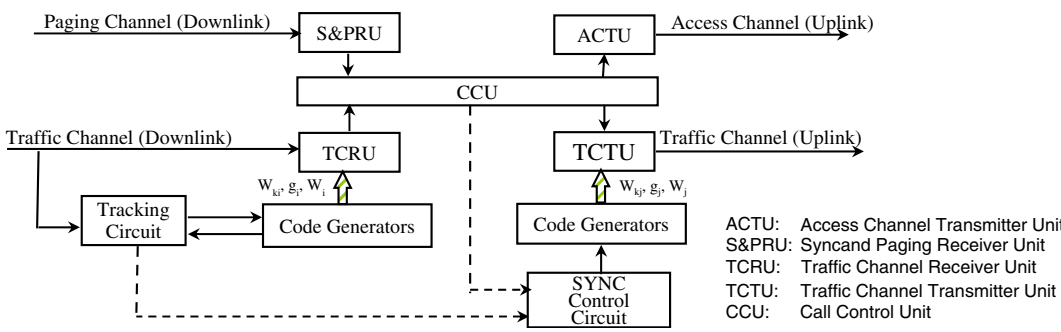


Figure 6. The SU tracking and Sync control circuits.

Traffic channel tracking circuit and the SYNC control circuit shown in Figures 6 and 7. As shown in Figure 7, the feedback signal Z_Δ of the tracking circuit of the downlink Traffic channel will also feed the input of the SU Sync control circuit. Hence, any change in the satellite propagation delay with respect to the established timing, by $\Delta\tau_p$ (resulting from satellite drift motion) will be indicated at the downlink Traffic channel tracking circuit. The $\Delta\tau_p$ timing jitter will then be used (by the SU Sync control circuit) to compensate the uplink transmission by advancing or delaying by $\Delta\tau_p$ using the SYNC control circuit.

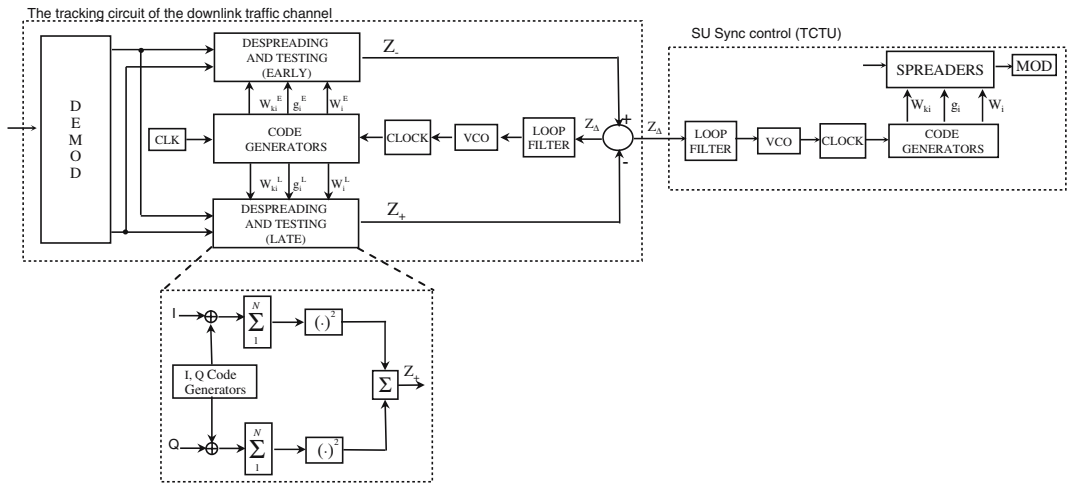


Figure 7. The fine Sync and Tracking Control used in the last step of the process.

3. Performance Evaluation

3.1. The Access Channel Performance

Considering the long round trip satellite propagarion delay, the main performance requirement of the Access channel is to provide high probability of success with the first transmission attempt. The probability of a successful message transmission depends (a) on the probability of PN code acquisition during the message preamble, (b) on the probability of message collision and (c) on the probability of no bit errors in the message after channel decoding (called Retention probability).

(a) The performance analysis presented in Appendix A, determine the design parameters for a serial/parallel aquisition circuit which maximizes the probability of acquiring successfully (P_{acq}) within the preamble interval. These parameters deternine the minimum preamble interval and the optimum window size ω for a given code length of L chips and known interference noise conditions. The probability P_{acq} refer as the *aquisition confidence*, is given by:

$$P_{\text{acq}} = Pr[T_{\text{acq}} \leq T_h] = \int_0^{T_h} f_{T_{\text{acq}}}(\tau)d\tau = F_{T_{\text{acq}}}(T_h). \tag{1}$$

Where, T_{acq} is the aquisition time for the window size of ω chips and T_h is the minimum allowed length of the message preamble which satisfies the aquisition confidence. The probability distribution $f_{T_{\text{acq}}}$ or the cumulative distribution $F_{T_{\text{acq}}}$ functions of the acquisition time is derived in Appendix A.

(b) Collision of two or more packets will occur if they are overlapping and have the same PN code phase offset when they arrive at the despreader. This is based on the assumption that the channel is unslotted (continuous time) and a signle PN code has been used for all users in the channel. Also we assume that all packets arrive at the despreader with approximatelly equal power. The probability that i packets collide given k_{o} packets are overlapping at any time instant, is given by:

$$P_{\text{coll}}(i\,|k_{\text{o}}) = \binom{k_{\text{o}}}{i} (1/L)^i (1-1/L)^{k_{\text{o}}-i} \quad \text{for} \quad 2 \le i \le k_{\text{o}}. \tag{2}$$

Where, $1/L$ is the probability that i packets have exactly the same phase offset of the PN code. The number of all possible phase offsets is assumed to be L, equal to the length of the code (in number of chips). (If the phase offset is less than a chip we assume that collision takes place)

The probabilty that k_{o} packets overlap is given by

$$P(k_{\text{o}}) = \frac{(2t_{\text{p}}G)^{k_{\text{o}}}}{k_{\text{o}}!} e^{-2t_{\text{p}}G}. \tag{3}$$

In the above expression t_{p} is the packet length and G in the total offered traffic load which includes both the newly arrived and retransmitted packets. (Two or more packets will overlap if they arrive in the interval $2t_{\text{p}}$)

The probability of collision then will be

$$P_{\text{coll}} = \sum_{k_{\text{o}} \ge 2} \sum_{i=2}^{k_{\text{o}}} P_{\text{coll}}(i\,|k_{\text{o}}) P(k_{\text{o}}). \tag{4}$$

(c) The probability of packet retention P_{ret}, is the probability of having no errors in the packet's information field after FEC. That is, if the packet length is n bits then $P_{\text{ret}} = (1-P_{\text{e}})^n$, where P_{e} is the bit error probability.

The probability of successful packet transmission then is given by

$$P_{\text{succ}} = P_{\text{acq}}(1 - P_{\text{coll}}) P_{\text{ret}}. \tag{5}$$

In the above equation however we assumed that there is always a receiver available to decode the data in the packet. If there are ℓ parallel data receivers available (as shown in Figure 3) then the probability of not finding an available one is $P_{\text{un}}(\ell) = \sum_{k_{\text{o}} \ge \ell} P(k_{\text{o}})$; Where $P(k_{\text{o}})$ is the probability of having k_{o} packets overlapping at the reception at a given load G (given in (3)). Then $P'_{\text{succ}} = P_{\text{succ}}[1 - P_{\text{un}}(\ell)]$.

3.1.1. Performance Results

In order to determine the values of T_h corresponding to the required acquisition confidence (as in (1)), we first derived the cdf of the acquisition time $F_{T_{\text{acq}}}$, (see Appendix A). Figure 8 shows an approximation of the cdf when $E_{\text{c}}/I_0 = -10\,dB$, $\gamma_1 = 54$ and $\gamma_2 = 137$ chips.

In Tables 1 and 2 shown below, we presented the serial/parallel acquisition circuit performance results for code lengths $L = 1024, 512$ and for $K = 32, 16$ parallel circuits. The false alarm probabilities used are $P_{\text{F1}} = 0.01$, $P_{\text{F2}} = 0.1$ and the corresponding penalty γ_{p} is equal to the PN code period L. The mean acquisition time $E[T_{\text{acq}}]$ varies from 0.3 to 1.4 ms depending on the values of the (E_{c}/I_0) (chip energy to interference ratio), L and K. The dwell occumulation values γ_1 and γ_2 are optimized for each case. The required preamble length T_h is provided in each case in number of code lengths ($\times L$) and in msec assuming the chip rate is $R_{\text{c}} = 9.8304$ Mc/s. The T_h values given in the tables represent the minimum preamble length required to achieve acquisition confidence 95%. As shown, the minimum required preamble length T_h varies from 0.73 to 3.65 ms for $L = 1024$ and from 0.16 to 1.83 ms for $L = 512$ depending on the channel conditions (E_{c}/I_0) and the number of parallel ACDCs (K). The packet delays introduced by these preamble lengths are then feasible and acceptable even with delay sensitive traffic.

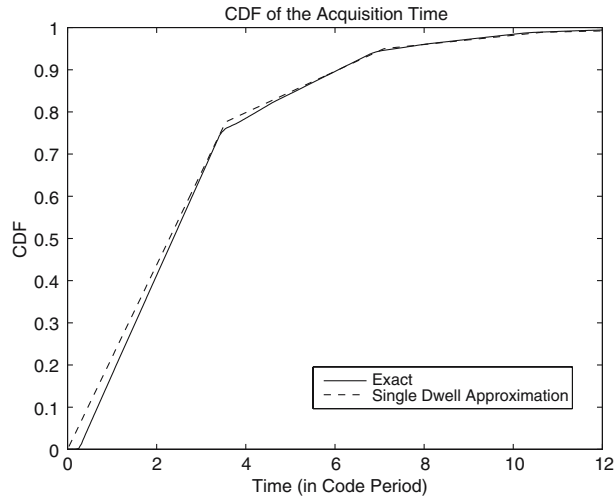


Figure 8. The cumulative distribution function of the acquisition time.

Table 1. Acquisition performance for $L = 1024$

K	E_c/I_0 (dB)	γ_1 (Chips)	γ_2 (Chips)	$E[T_{acq}]$ (ms)	T_h ($\times L$)	T_h (ms)
32	−10	54	137	0.3069	7.1002	0.7396
32	−12	85	243	0.4845	11.1816	1.1648
32	−14	135	371	0.7643	17.6459	1.8382
16	−10	54	141	0.5959	14.1483	1.4738
16	−12	85	243	0.9383	22.2378	2.3165
16	−14	135	371	1.4811	35.1115	3.6576

Table 2. Acquisition performance for $L = 512$

K	E_c/I_0 (dB)	γ_1 (Chips)	γ_2 (Chips)	$E[T_{acq}]$ (ms)	T_h ($\times L$)	T_h (ms)
32	−10	54	137	0.3695	7.0937	0.1611
32	−12	87	183	0.2537	11.2253	0.5847
32	−14	138	290	0.4015	17.7618	0.9251
16	−10	54	137	0.3044	14.0784	0.7333
16	−12	86	204	0.4811	22.2688	1.1599
16	−14	136	332	0.7609	35.1989	1.8334

Assuming acquisition confidence $P_{acq} = 0.95$ and bit error rate 10^{-5} (after FEC), we have also evaluated and plotted the probability of successful packet transmission P_{succ} versus the offered load (packets/s) for packet lengths of $n = 256$ and $n = 512$ encoded bits (or 128 and 256 information bits assuming FEC rate 1/2) the with $\ell = 1, 2, 3$ parallel data receivers (channel decoders). The period of the encoder is 512. The plot is shown in Figure 9. As shown, the P_{succ} is near 0.95 for a wide range of packet load (up to 10 packets/s), when the packet length is 256 symbols and with 2 or more channel decoders.

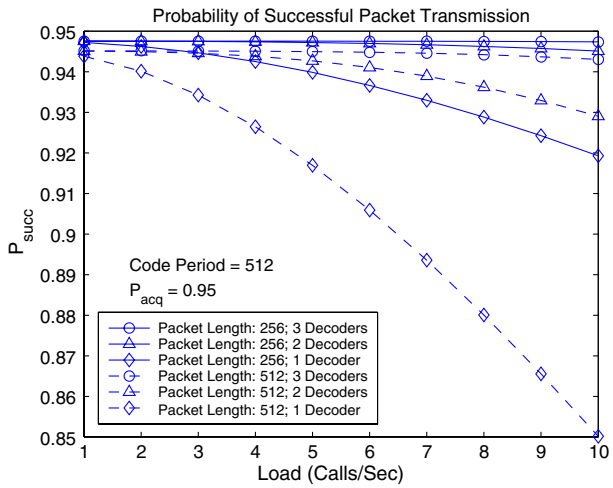


Figure 9. Probability of successful packet transmission.

3.2. Tracking Control Loop Performance

In this section we examine the tracking loop stability and the steady state error. The tracking loop performance is based on the analysis given in references [10] and [11] which is also outlined in Appendix B. The tracking loop circuitry is shown in Figure 10. The mean and the variance of the discriminator output has been derived for a discrete time model of the loop. Figure 11 shows the loop discriminator gain versus the timing error. The model of the above tracking circuit is shown in Figure 12(a). In this model the time unit is the duration of one channel symbol which is the period of accumulation. Assuming operation in the linear region of the curve, the loop has been approximated by a linear model shown in Figure 12(b).

There are four issues of importance in the practical system design: stability, convergence speed, steady state performance, and feedback bandwidth. In the following we discuss each one of them and their influence on each other.

The steady state timing error (derived in Appendix B) is be given by

$$\tau_s = \lim_{z\to 1}(1 - z^{-1})\frac{\tau(z)}{T_c} = \frac{c}{A\alpha F(z)}. \tag{6}$$

Where $F(z)$ is the loop filter, and c is the normalized doppler shift. The variance of the timing error $\sigma_s^2 = \mathrm{Var}(\tau/T_c)$ is given by (see equation (45) in Appendix B):

$$\sigma_s^2 = \frac{(V_0 + n_0)}{2\pi}\int_{-\pi}^{\pi}\left|\frac{\alpha F(e^{j\omega})e^{j\omega(-d-1)}}{1 - e^{-j\omega} + A\alpha F(e^{j\omega})e^{j\omega(-d-1)}}\right|^2 d\omega. \tag{7}$$

The value of $A\alpha$ is usually very small, and as we can see from the above expression the steady state variance increases as α increases. This implies that given a loop filter, there is an optimal value of α. We note however that the interference variance V_0 is itself a function of the steady state error.

So far, we have considered only one accumulator with length L. The length of the occumulation however cannot be larger than the proccessing gain because of the data symbol

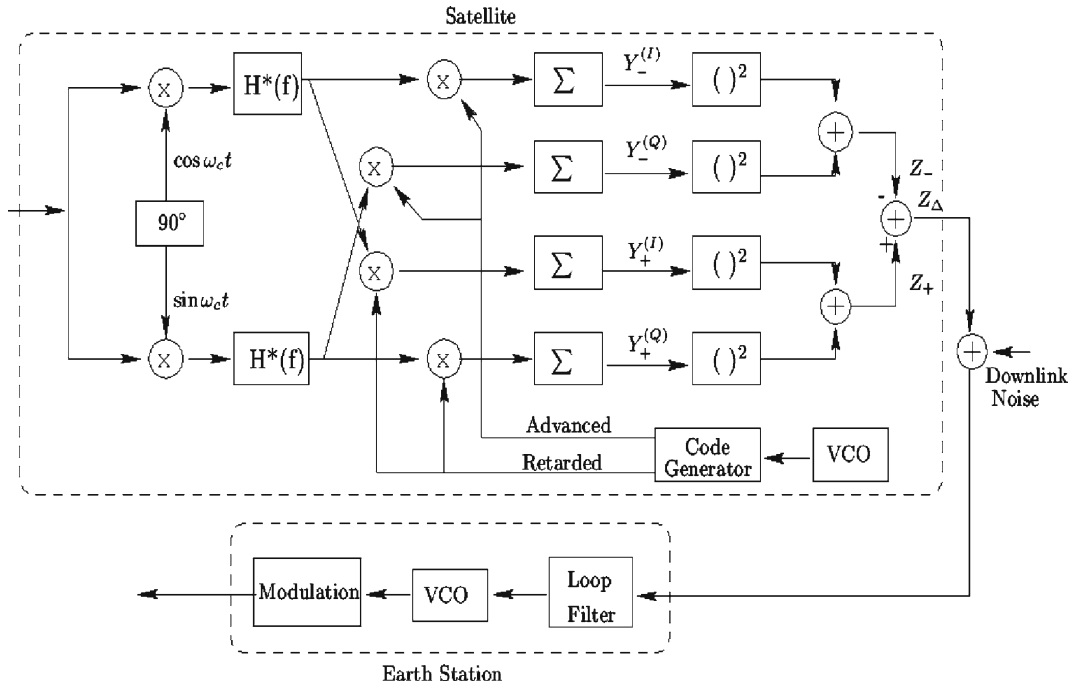


Figure 10. The noncoherent full-time code tracking loop.

length. This implies very large feedback bandwidth consumption (larger than the traffic channel), which is unreal. In attempting to solve this problem, we build a second accumulator on the satellite to accumulate and average Z_Δ. Assuming the length of the second accumulation is N, every component of the tracking loop now works N times slower. As we observe the previous equations we notice that only three parameters are affected by this down-sampling: the Doppler constant c, the delay step d, and the variance of the timing error σ_s^2. The Doppler constant is now replaced by $c' = cN$; the delay step is replaced by $d' = d/N$. The variance of V_0 is also divided by N because of the i.i.d. property of the interference from symbol to symbol. Equation (7) is thus replaced by

$$\sigma_{\mathrm{s}}'^2 = \frac{\sigma_{\mathrm{s}}^2}{N}. \tag{8}$$

From (6) we can see that if we want to maintain the same steady state timing error after the down-sampling, α needs to be N times larger. Using (7) and the new value of α in (8) we obtain higher steady state variance. Therefore we conclude that finer sampling (smaller N) achieves better steady state performance which however requires wider feedback bandwidth.

The final goal of this performance section is to establish the feasibility of the tracking feedback delay loop with given SS/CDMA system parameters and requirements. Hence, we consider the following system parameters: The chip rate $R_{\mathrm{c}} = 9.8304$ Mc/s ($T_{\mathrm{c}} = 1/R_{\mathrm{c}} = 1.0173 \times 10^{-7}$ s). The orthogonal (quadratic residue) code of length ($L = 60$), (one step in the discrete model is equal to 6.1035×10^{-6} s). The system is assumed to be fully loaded, which means that the number of users $K = 60$. The longest round trip delay is 0.26 s which makes the delay step d as large as 42598. The Doppler shift caused by the satellite drift is

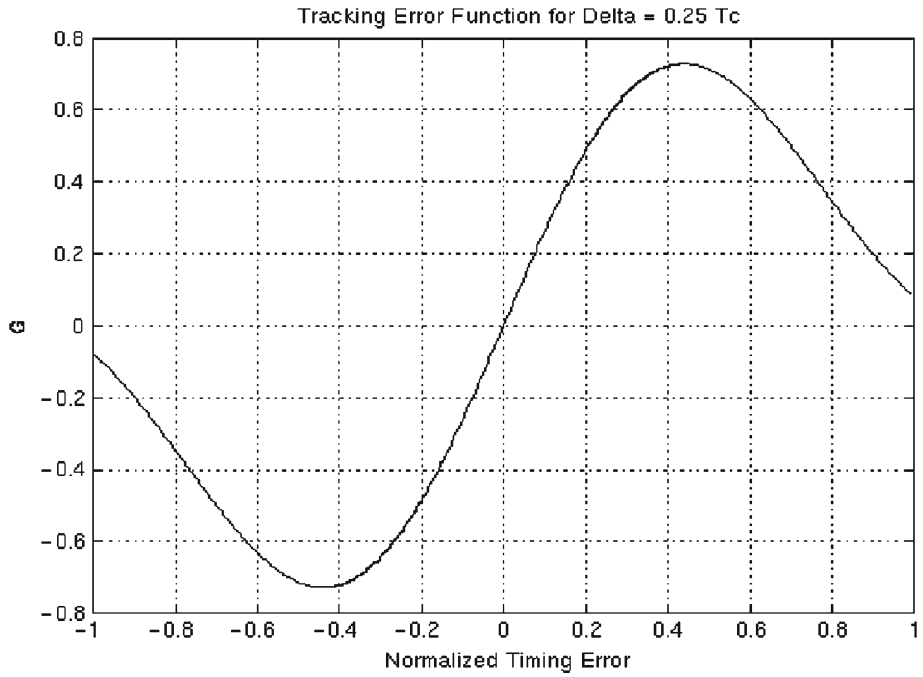


Figure 11. The tracking error function.

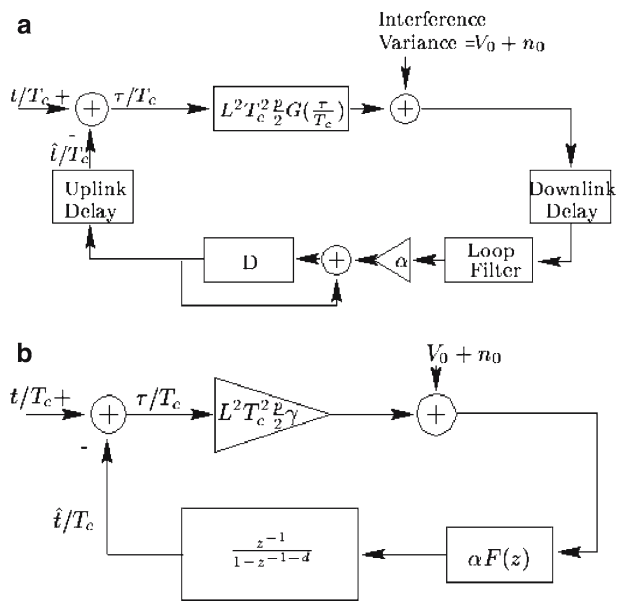


Figure 12a. (a) The tracking loop model. (b) The linear model of the code tracking loop.

40 ns/s. When normalized with T_c, the Doppler constant c is 2.4×10^{-6}. Raised cosine waveform with roll-off factor 0.1 is utilized as the chip waveform. As a result, the waveform factor $m_\psi = 9.8 \times 10^{-3}$ (see Appendix B). The received signal-to-noise ratio $E_s/N_0 = 6\,\text{dB}$. The maximum chip offset from the satellite oscillator is required to be within $\pm\frac{T_c}{10}$. For the

early-late correlators, we assume $\Delta T_c = \frac{T_c}{4}$, this puts a constraint of $\frac{T_c}{4}$ on the acquisition pull-in condition. The equivalent gain γ of the linear model can be obtained from (B.7) in Appendix B, is 2.6762.

In the following evaluation, we assume that the feedback information is well encoded so that the downlink noise can be ignored. Taking into consideration the accuracy of the feedback information, and the fact that the feedback bandwidth is limited, we reach the decision of setting the down-sampling factor $N = 1000$. Scaling of d, c, and σ_s^2 is done as described above. The assumption that the timing error does not change much in N symbols is justified since the new normalized Doppler shift is only 2.4×10^{-3} chip. Due to the large delay d, solving the characteristic functions (B.14) and (B.15) in Appendix B is not possible. Fortunately, we can use Jury Stability Test (see [12]) with computer aided search. The result shows that is not possible to have a loop filter of the form $F(z) = \frac{B(z)}{1-z^{-1}}$ (see equation (B.13) in Appendix B) without a steady state error. This means that we'll always have a steady state error $\tau_s = \frac{c}{A\alpha F(z)}$ (see equation (B.16) in Appendix B). Therefore, a scaling adjustment is required when the steady state is reached. This is possible since τ_s is approximately known.

A simple form of loop filter is taken for evaluation.

$$F(z) = \frac{1}{1 + \beta z^{-1}}. \tag{9}$$

Computer search shows that β can only be in the range of $(-1, 1)$ so the system is stable. The maximum allowable values of $A\alpha$ for different values of β's are shown in Figure 13. We define a cost function as $\tau_s + 2\sigma_s$, which means we have more than 95% of confidence that the timing error will be smaller than $\tau_s + 2\sigma_s$. A typical relationship between τ_s and σ_s is shown in Figure 14. With the timing error requirement being $T_c/10$, it is shown that the curve of $\tau_s + 2\sigma_s$ has two crossings with $T_c/10$. Considering the time needed for convergence after acquisition pull-in, we always want to maximize the loop gain. Therefore, it is better to choose the crossing point with larger α. In order to get the global optimization of α and β which minimize the convergence time with timing error requirement matched, we can use the linear model to simulate for each β and the corresponding α (the second crossing point). Hence, the optimal values of α and β for which the convergence time is the shortest can then be determined.

4. Conclusion

In this paper we have presented and evaluated the network synchronization for an orthogonal CDMA satellite system. The objective of providing sychronization of all uplink orthogonal code Traffic channels, as shown, can be achieved with a procedure which involves the uplink random access channel for coarse code acquisition and the use of an innovative feedback tracking control loop for fine synchronization. The Access channel code acquisition scheme is based on a parallel/serial design which is optimized in terms of minimizing the acquisition time and maximizing the acqisition confidence for a given signal-to-noise ratio. Performance analysis indicates that packets may be transmitted successfuly over the Access channel with probability near 0.95 when the traffic load is up to 10 packets/s and for a given set of system parameters. Performance analysis of the tracking loop has also been performed in order to

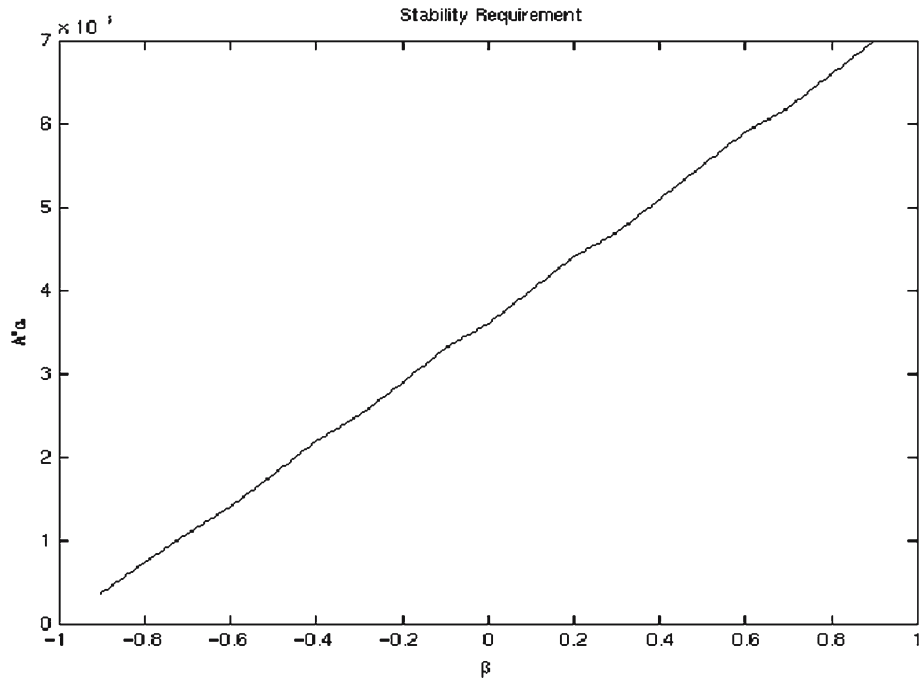


Figure 13. Stability requirement.

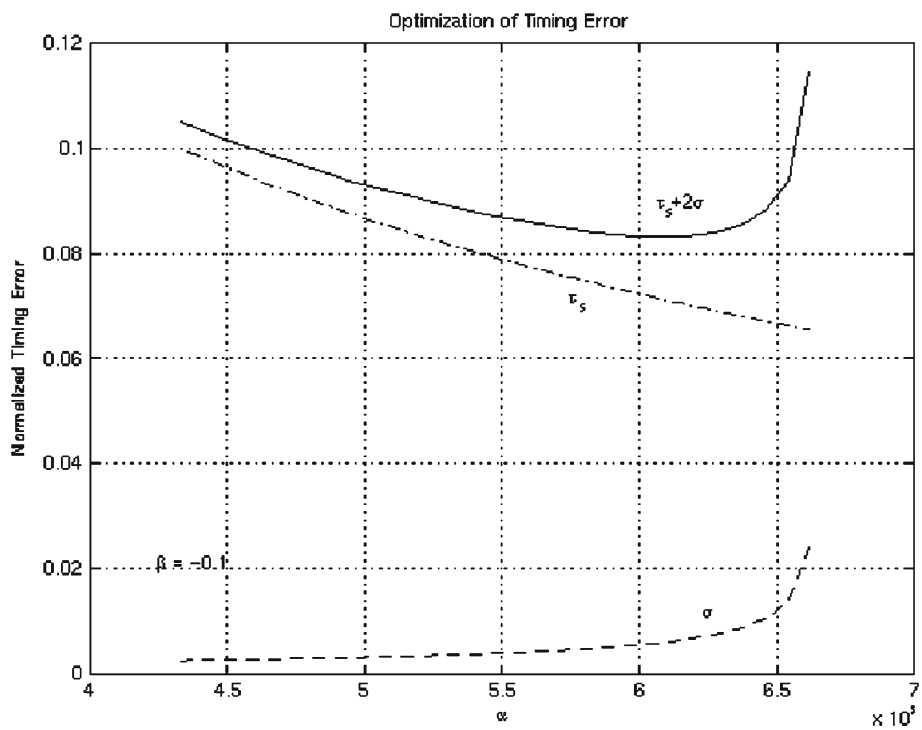


Figure 14. Optimization of the timing error.

determine the stability and the optimum loop design. Due to long round trip satellite propagation delay the loop responce has a steady state error which can be corrected by a scaling adjustment. Thus, the requirement of synchronizing each orthogonal code to the reference time within 10% of the chip length can be achieved.

Appendix A : The Packet Acquisition Performance

The PN code aquisition is based on the serial/parallel model shown in Figires 3 and 4. The PN sequence of length L is divided into K subsequences of ω chips each. There are K double dwell serial search circuits operating in parallel over each of these subsequences or windows. The PN phase offset of each arrived packet in a given window will be detected by the corresponding parallel searching circuit. In general the acquisition performance can be improved if the outputs of these parallel circuits are processed jointly, therefore the performance of any of the circuits assuming that they work independently can serve as an upper bound.

In order to determine the false alarm and detection probabilities, we first assume that each chip is further divided into l cells during the search. This will give a final pull-in uncertainty of $\frac{T_c}{2l}$ for the code tracking. For each searching window, a total of $\nu = l\omega$ cells will be tested, among which $\nu - 2l$ can lead to false alarms. The false alarm probabilities for noncoherent reception under unfaded AWGN channels can be written as (see [10]).

$$P_{Fi} = \int_{\Theta_i}^{\infty} p_{0i}(z)dz = e^{-\Theta_i/V_i}, \quad i = 1, 2, \tag{A.1}$$

where i is the dwell index and Θ_i is the corresponding threshold. $V_i = \gamma_i I_o$ is the equivalent noise spectral density with γ_i being the dwell (accumulation) time and

$$I_0 = N_0 + 2m_\psi \sum_{j=1}^{K_a} E_c(j). \tag{A.2}$$

Where $E_c(j)$ is the energy per chip for user j and K_a is the number of simultaneous packet reception; m_ψ is an interference constant depending on the chip waveform. For the $2l$ cells within one chip of the correct timing, we need to determine the detection probabilities. The worst case corresponds to sampling times that differ from the correct (peak) time by

$$\tau_j = \frac{j - (l + \frac{1}{2})}{l} T_c, \quad j = 1, 2, \ldots, 2l. \tag{A.3}$$

For each of these sampling times, the detection probabilities are given by

$$P_{Dij} = \int_{\Theta_i}^{\infty} p_{1ij}(z)dz = \int_{\Theta_i/V_i}^{\infty} e^{-(x+\mu_{ij})} J_0(2\sqrt{\mu_{ij}x})dx, \quad i = 1, 2; \quad j = 1, 2, \ldots, 2l, \tag{A.4}$$

with

$$\mu_{ij} = \gamma_i \frac{E_c(k)}{I_0} R^2(\tau_j), \tag{A.5}$$

where $R(\tau_j)$ is the correlation between the chip waveform and the receiver chip filter with time offset τ_j.

The reduced state diagram (in reference [10]), now has the branch transfer functions

$$H_0(z) = z^{\gamma_1}(1 - P_{\mathrm{F1}}) + z^{\gamma_1+\gamma_2} P_{\mathrm{F1}}(1 - P_{\mathrm{F2}}) + z^{\gamma_1+\gamma_2+\gamma_\mathrm{p}} P_{\mathrm{F1}} P_{\mathrm{F2}}, \tag{A.6}$$

$$H_\mathrm{D}(z) = \sum_{j=1}^{2l} P_{\mathrm{D1}\,j} P_{\mathrm{D2}\,j} z^{\gamma_1+\gamma_2} \prod_{i=1}^{j-1} \left[(1 - P_{\mathrm{D1}i}) z^{\gamma_1}\right], \tag{A.7}$$

$$H_\mathrm{M}(z) = z^{2l\gamma_1} \prod_{j=1}^{2l} (1 - P_{\mathrm{D1}\,j}) + \sum_{j=1}^{2l} P_{\mathrm{D1}\,j}(1 - P_{\mathrm{D2}\,j}) z^{\gamma_1+\gamma_2} \prod_{i=1}^{j-1} \left[(1 - P_{\mathrm{D1}i}) z^{\gamma_1}\right]. \tag{A.8}$$

Where $H_0(z)$ corresponds to the transfer function of the branches emerging from the $\nu - 2l$ nodes without the presence of the signal and $H_\mathrm{D}(z)$ and $H_\mathrm{M}(z)$ are the detection and miss transfer functions respectively emerging from the super-state representing the cells within one chip of the correct timing; γ_p is the penalty for false alarm at the second dwell. The total transfer function assuming that all cells in the searching window are equally likely to become the starting cell is given as follows

$$U(z) = \frac{H_0(z) H_\mathrm{D}(z) \left[1 - H_0^{\nu-2l}(z)\right]}{(\nu - 2l)\,[1 - H_0(z)] \left[1 - H_\mathrm{M}(z) H_0^{\nu-2l}(z)\right]}. \tag{A.9}$$

The mean and variance of the acquisition time can therefore be computed by

$$E[T_\mathrm{acq}] = \left.\frac{dU(z)}{dz}\right|_{z=1}, \tag{A.10}$$

and

$$\mathrm{Var}[T_\mathrm{acq}] = \left.\left\{\frac{d^2U(z)}{dz^2} + \frac{dU(z)}{dz}\left[1 - \frac{dU(z)}{dz}\right]\right\}\right|_{z=1}. \tag{A.11}$$

These two quantities, however, are not sufficient to evaluate the acquisition confidence for the given preamble length. Fortunately the operating situation we consider here meets the conditions given in [13], the approximation therein therefore can be applied to compute the cdf of the acquisition time. The single dwell equivalence of the case considered can be characterized by the following parameters:

$$\nu_e = \nu - 2l + 1, \tag{A.12}$$

$$\gamma_e = \left(\gamma_1 + P_{\mathrm{F1}} \frac{1 - P_{\mathrm{F2}}}{1 - P_{\mathrm{F1}} P_{\mathrm{F2}}} \gamma_2\right)\left(\frac{\nu_e - 1}{\nu_e}\right) + \left(\left.\frac{dH_\mathrm{D}(z)}{dz}\right|_{z=1} + \left.\frac{dH_\mathrm{M}(z)}{dz}\right|_{z=1}\right)\frac{1}{\nu_e}, \tag{A.13}$$

$$\gamma_{\mathrm{p}^e} = \gamma_\mathrm{p} + \frac{1 - P_{\mathrm{F1}}}{1 - P_{\mathrm{F1}} P_{\mathrm{F2}}} \gamma_2, \tag{A.14}$$

$$P_{\mathrm{D}e} = H_D(z)|_{z=1}\,, \tag{A.15}$$

$$P_{\mathrm{F}e} = P_{\mathrm{F1}} P_{\mathrm{F2}}, \tag{A.16}$$

where in (A.4) the second term is added to account for the additional dwell time introduced by the super-node containing the correct timing. When the search window size $\nu \gg 2l$, (A.4) becomes equivalent to (A.13) in [13]. The cdf of the acquisition time can then be approximated by [13].

$$F_{T_{\text{acq}}}(t) = 1 - (1 - P_{\text{D}e})^J \left[1 + J P_{\text{D}e} - \frac{P_{\text{D}e} t}{\nu_e(\gamma_e + P_{\text{F}e}\gamma_{\text{p}e})} \right] \tag{A.17}$$

where

$$J = \left\lfloor \frac{t}{\nu_e(\gamma_e + P_{\text{F}e}\gamma_{\text{p}e})} \right\rfloor. \tag{A.18}$$

Now, we assume that the false alarm probabilities $P_{\text{F}i}$, the penalty γ_{p}, the window size ν, the chip waveform and E_{c}/I_0 are given by the system requirements. If we further define an acquisition confidence α so that within the preamble length T_h, the probability of acquisition is P_{acq}, according to (A.8), we have

$$(1 - P_{\text{D}e})^J \left[1 + J P_{\text{D}e} - \frac{P_{\text{D}e} T_h}{\nu_e(\gamma_e + P_{\text{F}e}\gamma_{\text{p}e})} \right] = 1 - P_{\text{acq}}. \tag{A.19}$$

This relation can be used to obtain the optimal dwell times γ_1 and γ_2 which will minimize the required preamble length T_h. Due to the integration in (4), this optimization problem cannot be solved analytically. A discrete two dimensional search, however, can be performed to find the best dwell times. Given the simple form of (A.10), this search process does not need excessive computation.

Figure 8 shows an approximation of the cdf when $E_{\text{c}}/I_0 = -10\,dB$, $\gamma_1 = 54$ and $\gamma_2 = 137$ chips. In Tables 1 and 2 we presented the serial/parallel acquisition results performed with code lengths $L = 1024,\ 512$ and for $K = 32,\ 16$ parellel circuits. The parameters used are $P_{\text{F}1} = 0.01$, $P_{\text{F}2} = 0.1$, $P_{\text{acq}} = 0.95$, and the penalty γ_{p} equal to the PN code period L. The transmission chip waveform employed is a raised cosine with roll-off factor 0.1, and the receiver uses a matched filter with the same waveform.

During the search, local minima resulted from the discontinuity in (A.9) were observed. Moreover, smaller T_h does not guarantee smaller mean acquisition time due to the change of cdf. For example, longer dwell time can make T_h smaller by reducing the variance, but it also shifts the mean acquisition time towards larger value. As a result, we have to compromise between these two quantities. The results presented here have the minimal mean acquisition times among the local minima observed.

Appendix B: The Code Tracking Analysis

The mean and the variance of the discriminator output of the noncoherent code tracking circuit shown in Figure 11 given below, are derived in reference [10].

$$E[Z_\Delta] = L^2 T_{\text{c}}^2 \frac{p}{2}(R_+^2 - R_-^2), \tag{B.1}$$

$$\begin{aligned} \text{Var}[Z_\Delta] &\le \text{Var}(Z_-) + \text{Var}(Z_+) \\ &= 8(\sigma_N^2 + \sigma_I^2)^2 + 8L^2 T_{\text{c}}^2 p(R_+^2 + R_-^2)(\sigma_N^2 + \sigma_I^2), \end{aligned} \tag{B.2}$$

where p is the transmission power, L is the number of chips per accumulation and T_c is the chip duration. R_+ is the partial correlation between the (chip) matched filter of the late gate and the signal of interest, (see [14]). σ_N^2, σ_I^2 are the interferences due to thermal noise and other users, respectively.

$$\sigma_N^2 = LT_c\frac{N_0}{4}, \quad \sigma_I^2 = LK\frac{p}{2}T_c^2 m_\psi, \quad \text{and} \quad m_\psi = \frac{1}{2}\frac{1}{2\frac{T_c}{10}}\sum_{\substack{i=-\infty \\ i\neq 0}}^{\infty}\int_{iT_c-\frac{T_c}{10}}^{iT_c+\frac{T_c}{10}} R^2(t)dt, \tag{B.3}$$

where $R(t)$ is the convolution of the chip waveform and the matched filter (normalized, i.e., $R(0) = 1$).

The model of the above tracking circuit is shown in Figure 12(b). In this model the time unit is the duration of one channel symbol which is the period per accumulation. We define the gain of the early-late discriminator as $E[Z_\Delta(\tau)]$, which is a function of the normalized relative timing error τ/T_c. The relative timing error τ is the timing difference between the incoming signal and the local code generator.

$$E[Z_\Delta(\tau)] = L^2T_c^2\frac{p}{2}G(\tau/T_c), \tag{B.4}$$

where

$$G(\tau/T_c) = R^2\left(\frac{\tau-\Delta}{T_c}\right) - R^2\left(\frac{\tau+\Delta}{T_c}\right). \tag{B.5}$$

We also define the interference variance as

$$V_0 \leq \mathrm{Var}[Z_\Delta]. \tag{B.6}$$

The voltage controlled oscillator (VCO) in the terminal is modeled as an accumulator since the absolute timing of the local code generator is modified according to all previous (scaled) timing errors. When the pull-in condition from the acquisition stage is good, the relative timing error is very small. In this case, the tracking loop is operating in the linear region, see [15]. We can then model the loop by a linear model (shown in Figure 12(b)), in which γ is defined by

$$\gamma = \left.\frac{dG(\tau/T_c)}{d(\tau/T_c)}\right|_{\tau=0} \tag{B.7}$$

and $F(z)$ is the transfer function of the loop filter. Let the normalized pull-in timing error be τ_0/T_c, it can be represented by a step function whose generating function is $(\tau_0/T_c)/(1-z^{-1})$. In addition to this fixed timing error, we have the error caused by the satellite drift. During the tracking stage, this drift can be assumed to have fixed direction and fixed speed. Its z-transform can be written as $cz^{-1}\left(\frac{1}{1-z^{-1}}\right)^2$, where c is the normalized Doppler shift. The input to the linear model is then the sum of these two timing error terms. Finally, the generating function of the relative timing error is

$$\frac{\tau(z)}{T_c} = \left[\frac{\tau_0}{T_c}\left(\frac{1}{1-z^{-1}}\right) + cz^{-1}\left(\frac{1}{1-z^{-1}}\right)^2\right]\frac{1}{1+H(z)}, \tag{B.8}$$

$$H(z) = \frac{L^2T_c^2\frac{p}{2}\gamma\alpha F(z)z^{-1}}{1-z^{-d-1}}, \tag{B.9}$$

with d equal to the round trip propagation delay. If the loop filter is chosen such that its bandwidth is sufficiently narrow, V_0 can be assumed to be white Gaussian distributed. In steady state when the timing error is τ_s, V_0 is given by

$$V_0 = 8\left(\sigma_N^2 + \sigma_I^2\right)\left[\sigma_N^2 + \sigma_I^2 + L^2 T_c^2 \frac{p}{4}\left(G(\tau/T_c)\right)\right] \tag{B.10}$$

The variance of the timing error is obtained from the linear model as

$$\mathrm{Var}(\tau/T_c) = \frac{V_0 + n_0}{(L^2 T_c^2 \frac{p}{2}\gamma)^2}\frac{1}{2\pi}\int_{-\pi}^{\pi}\left|\frac{H(e^{j\omega})}{1 + H(e^{j\omega})}\right|^2 d\omega, \tag{B.11}$$

where n_0 is the downlink noise and $A = L^2 T_c^2 \frac{p}{2}\gamma$. Using equations (B.8) and (B.9) above we obtain the generating function of the relative timing error.

$$\frac{\tau(z)}{T_c} = \frac{1}{(1 - z^{-1})}\frac{\frac{\tau_0}{T_c} - \left(\frac{\tau_0}{T_c} - c\right)z^{-1}}{1 - z^{-1}\left(1 - A\alpha F(z)z^{-d}\right)}. \tag{B.12}$$

In order to have steady state timing error $\tau_s = 0$, we require that the loop filter in the form

$$F(z) = \frac{B(z)}{1 - z^{-1}} \tag{B.13}$$

where $B(z)$ can be any ratio of polynomials and d is feedback time delay. The characteristic function of $\frac{\tau(z)}{T_c}$ then is

$$(1 - z^{-1})^2 + A\alpha B(z)z^{-d-1}. \tag{B.14}$$

The loop filter $F(z)$, in general, will drive the system unstable when the feedback delay is large. For this reason we must include nonzero steady state timing error in our design consideration. If $F(z)$ does not have 1 as a pole, the characteristic function of $\frac{\tau(z)}{T_c}$ will be

$$(1 - z^{-1})(1 - z^{-1} + A\alpha F(z)z^{-d-1}). \tag{B.15}$$

By Final Value Theorem (see [12]), the steady state timing error will be given by

$$\tau_s = \lim_{z\to 1}(1 - z^{-1})\frac{\tau(z)}{T_c} = \frac{c}{A\alpha F(z)} \tag{B.16}$$

which decreases as α increases.
Using expression (B.11) the variance of the timing error $\sigma_s^2 = \mathrm{Var}(\tau/T_c)$ will be given by:

$$\sigma_s^2 = \frac{(V_0 + n_0)}{2\pi}\int_{-\pi}^{\pi}\left|\frac{\alpha F(e^{j\omega})e^{j\omega(-d-1)}}{1 - e^{-j\omega} + A\alpha F(e^{j\omega})e^{j\omega(-d-1)}}\right|^2 d\omega. \tag{B.17}$$

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