A HIGH-RESOLUTION AND FAST-CONVERSION TIME-TO-DIGITAL CONVERTER

Chorng-Sii Hwang, Poki Chen, Hen-Wai Tsao*

Department of Electrical Engineering and Graduate Institute of Electronics Engineering

National Taiwan University
Taipei, Taiwan, 10617, R.O.C.

* Department of Electronic Engineering, National Taiwan University of Science and Technology
Taipei, Taiwan 10650, R.O.C.

E-mail : tsaohw@cc.ee.ntu.edu.tw

ABSTRACT

This paper describes a design of time-to-digital converter (TDC), which has the features of high-resolution and fast conversion. With the aid of the gate delay difference technique, the TDC can achieve a sub-gate delay resolution. The flash-type operation enables the TDC to resolve the time difference for fine conversion in less than one reference clock cycle. The DNL can be less than ±0.03LSB and INL less than ±0.04LSB. We confirm the results based on 0.35um CMOS process technology.

1. INTRODUCTION

The time-to-digital converters (TDC's) have been widely used in many applications, e.g. particle life time detection in high energy physics, phase meter, frequency counter, automatic test equipment, laser range finder, on-chip jitter measurement etc. Most of the early TDC's were constructed with many discrete components on printed circuit boards such that they usually consumed large power. Due to the rapid development in VLSI technology, the design methodology of the TDC is moving toward highly integration so as to reduce the cost and power while maintaining the property of high resolution.

Traditionally, the TDC's utilize analog approaches like dual slope, and time-to-amplitude methods. The former often needs both charging and discharging current sources with the aid of a digital counter. The time-to-amplitude method converts the time difference into a voltage. Then the voltage is converted by an analog-to-digital converter (often the oversampling type) to achieve high resolution [1]. These methods are slow and vulnerable to the system noise. Averaging technique is frequently used to increase the accuracy.

Several digital methods were also introduced to obtain good property of high resolution and low power. The delay-locked loop (DLL) has been widely used to provide accurate timing reference in the digital type TDC's [2]. Due to the limitation of intrinsic delay (several hundreds of picosecends) of the delay buffer in DLL, the technique of applying the gate delay difference is adopted to improve the resolution up to sub-gate delay. The pulse-shrinking [3,4], vernier delay line (VDL) [5,6] and array [7] methods were presented. These approaches still suffer from long dead time or large area. Here we present a new method to construct the TDC that has the merits of high resolution and fast conversion with moderate chip area and power.

2. PRINCIPLE OF OPERATION

The proposed TDC accepts two asynchronous START and STOP input signals. The time interval between START and STOP is mainly digitized by DLL method. We use DLL's to provide precise timing to obtain the sub-gate delay resolution in fine time conversion. The principle of conversion is described in detail in the following sub-sections.

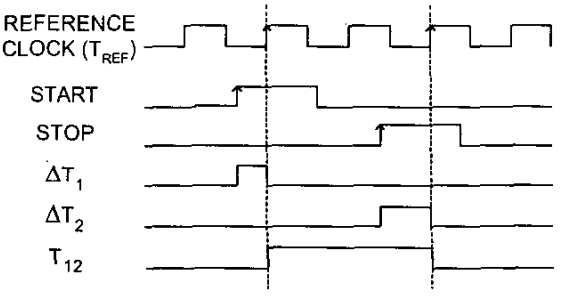

Figure 1. Timing diagram of conversion

A. Timing of Conversion

The timing diagram of the proposed TDC is shown in Fig.1. The timing acquisition process is divided into three phases : Firstly, the time interval (ΔT_1) between the rising edges of the START signal and the succeeding reference clock is measured. Secondly, a coarse counter is activated to measure the time (T_{12}) between the START and STOP signals aligned to the reference clock. Finally, the same procedure for the STOP signal versus reference clock rising edge is also performed. Then, the conversion result is equal to ($\Delta T_1 + T_{12} - \Delta T_2$). The dynamic range for fine conversion (ΔT_1, ΔT_2) is limited to only one reference clock cycle (T_{REF}). Since the coarse result is derived from the counter, the overall dynamic range of the time interval measurement can be extended by increasing the bit number of the counter.

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B. Time Sampler

The time sampler consists of a tapped delay line and a set of D-flip/flops. To acquire the timing relationship between data and clock, we may apply the data or clock signal to the tapped delay line [6]. We choose the delaying data technique as the main building block to construct the circuitry for fine conversion (see Fig.2). Assume the delay of the delay buffer is Δt_d. The Q output in the the i^{th} D-flip/flop represents the status of data signal of being ahead of the clock by an amount of $(i*\Delta t_d)$.

$$\text{If } Q_i = \text{High}, \quad t_x >= i*\Delta t_d$$
$$= \text{Low}, \quad t_x < i*\Delta t_d$$

If Q outputs of the 0^{th}~ i^{th} D-flip/flops are all high and the rest are low, it means that the data signal leads the clock signal by $(i*\Delta t_d)$. Assuming the data signal leads the clock signal by t_x, we can obtain the relationship :

$$i*\Delta t_d =< t_x < (i+1)*\Delta t_d$$

By utilizing a tapped delay line, the time sampler is equivalent to a timing vernier using the clock rising edge as the reference point with the limited resolution of the logic buffer delay Δt_d in Fig.3.

In practical application, the delay of the tapped delay buffer is stabilized via the control of delay from DLL with N delay elements running at a frequency equal to T_{REF}^{-1}. Then the data signal will propagate through the delay line to achieve a resolution of Δt_d which is equal to (T_{REF}/N).

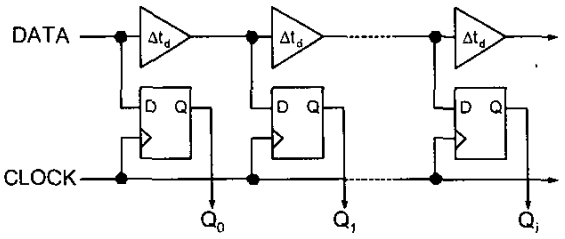

Figure 2. Time sampler using a tapped delay line

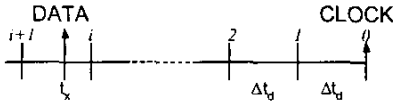

Figure 3. Timing vernier with a unit delay buffer resolution

C. Time Samplers with a sub-gate resolution

To achieve a finer resolution, the spacing of the vernier should be cut into several pieces equally (into a division of M). We assume that the finer resolution is Δt_r (= Δt_d/M). The timing information on the timing vernier can be derived from M time samplers with the phase-shifted sampling clocks described in the following.

At first, a time sampler is built as in Sec.2.B. Then a second time sampler with a phase-shifted sampling clock is also built as shown in Figure 4. The amount of phase-shift should be designed to fit the finer resolution Δt_r. By duplicating the time samplers with increased shifted amount by (M-1) times, the new TDC can achieve a sub-gate resolution of Δt_r (= $T_{REF}/[M*N]$).

In practical circuit implementation, the sub-gate resolution can be realized by employing the technique of gate delay difference. At first, we can add an extra delay buffer which has the same delay (Δt_d) as the tapped delay line. Then we must add a new delay buffer in front of the sampling clock. The delay of the new delay buffer should be equal to Δt_c (= $\Delta t_d \pm \Delta t_r = \Delta t_d*[M\pm1]/M = T_{REF}*[M\pm1]/[M*N]$). The new scheme for fine conversion is presented in Figure 5. For simplicity, we choose $\Delta t_c = \Delta t_d - \Delta t_r$ in discussion below.

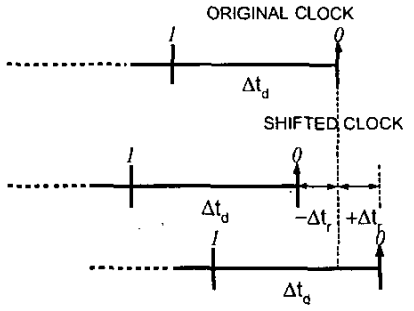

Figure 4. Timing vernier with a phase-shifted clock

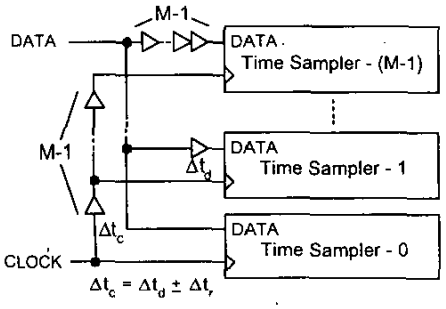

Figure 5. The new scheme for fine conversion

The Q output state of the i^{th} D-flip/flop in the j^{th} time sampler represents the timing of data signal indicated by the following formula :

If $Q_{i,j}$ = High, then

$$t_x >= i*\Delta t_d + j*\Delta t_r = i*M*\Delta t_r + j*\Delta t_r = (i*M + j)*\Delta t_r$$

If $Q_{i,j}$ = Low, then

$$t_x < (i*M + j)*\Delta t_r$$

If we re-define the data timing by leading the clock in this relationship ($t_x >= k * \Delta t_r$), then k should be equal to $(i*M + j)$. This result shows that the sequence of the new time vernier will be rotated row-wise in the parallel time samplers. Since the delay buffers for data path share the same bias control from a single DLL, all the delay lines inside the time samplers can be combined into only one delay line so as to minimize the area and power with proper arrangement.

The delay of the delay buffer in clock path should also be stabilized by a DLL. If we use the same reference clock for the new DLL in clock path, the delay line inside the DLL should contain ($T_{REF}/\Delta t_c$) (= [M*N]/[M±1]) tapped delay buffers.

D. Comparison

The proposed scheme for fine conversion can achieve the fastest conversion time with only the extra time of (M-1)* Δt_d. The increased time amount must be less than a reference cycle if the DLL is used to stabilized the delay of clock path.

The array method can sample the data in only one reference clock cycle. But it will need an array of DLL's and each DLL must have its own phase detector, charge pump, and loop filter. The area, power and routing complexity of the array method is more difficult to handle than the proposed scheme.

The VDL method described in [5] used a read-out pipeline to reduce the dead time. But the extra register files usually occupy more area than our proposed scheme if both methods have the same dynamic range. Our proposed scheme works essentially in a flash-type manner.

3. CIRCUIT DESCRIPTION

In order to evaluate the performance of the proposed TDC, we have designed a chip to be fabricated in TSMC 0.35um Silicide digital process. The architecture of the TDC chip is presented in Fig. 6. This chip accepts asynchronous START and STOP signals and then measures their time difference. The resolution is designed to be one fourth of the logic buffer delay. For multi-STOP application, we can simply replicate the delay lines, DFF arrays and counters.

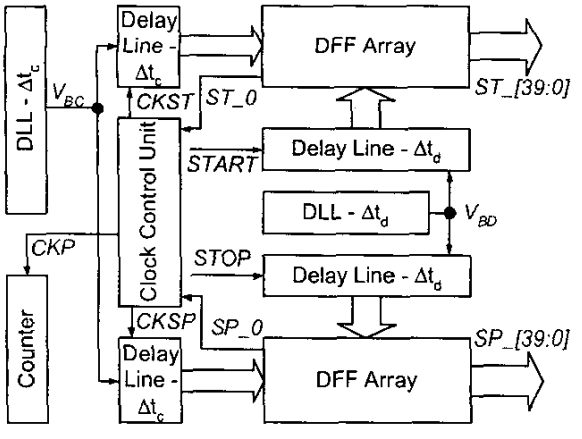

Figure 6. The architecture of the TDC chip

A. Delay-Locked Loop

Two DLL's are responsible for generating bias voltages to stabilize the delay of data and clock paths. For the data path, the DLL contain a 10-stage delay line, i.e. Δt_d is set to be $T_{REF}/10$. Since the sub-gate resolution is designed to be a quarter of Δt_d, the Δt_c is set to be $T_{REF}/8$ (=$T_{REF}/10$+$T_{REF}/40$). Thus the DLL for clock path utilizes an 8-stage delay line. Both DLL's utilize bang-bang configuration.

B. Delay Cell

The circuit diagram of the voltage-controlled delay cell is shown in Fig. 7(a). Its delay is determined by the current driving capability which is controlled by the gate bias of the starving NMOS transistors. In order to acquire better matching property in delay, the length of the transistors is chosen to be larger than the feature length. The two-inverter buffer is used for driving the clock and data paths to the D-flip/flop array. The delay characteristic of the delay cell is shown in Fig. 7(b). The bias voltages are set to V_{DD} before the lock-in process starts.

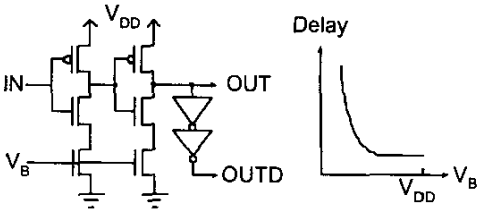

Figure 7. (a) Delay cell. (b)Delay vs. bias voltage

C. Phase Detector and Charge Pump

The linear type phase detector has dead-zone and phase offset problems. They are due to the finite rise/fall time of up/down pulses, charge sharing, charge injection and current mismatch [8]. Thus, the bang-bang type phase detector is chosen for its good phase response. An edge-triggered D-flip/flop with cross-coupled RS-latches [7] is used in the DLL's. From simulation, we find that the phase reference point is dependent on the initial state of the D-flip/flop output. Thus the phase detector is to be preset in the first cycle then to compare in the next cycle. The effective time for UP and DN pulse is also gated to be only a half cycle after phase comparison is complete.

The charge pump converts the phase difference derived from the phased detector into voltage so as to control the delay. Current-mode charge pump with power switches is used [9]. In a bang-bang type DLL, the charge in the loop filter must be added or removed after every comparing cycle. The loop jitter can be controlled via the charge pump current and switch turn-on time. The phase offset caused by charge injection, charge sharing and current mismatch in the charge pump can be ignored in the bang-bang operation.

The loop filter capacitor is a large NMOS transistor inside the N-well [10]. This transistor operates in accumulation mode to provide good frequency response comparing to the NMOS transistor located in the P-substrate. A guard ring around the loop filter is carefully added to prevent the substrate noise coupling.

E. D-Flip/Flop Array

The edge-triggered D-flip/flop is adopted again in the DFF-array due to its good timing characteristic. The size and current are optimized for both area and speed in operation. The outputs of DFF array are reordered to fit the sequence of conversion result.

E. Clock Control Unit and Counter

As shown in Fig. 6, before sending the reference clock to the clock delay path, the CKST and CKSP should be properly manipulated to avoid wrong sampling condition. After the START or STOP signals occur and propagate along the data delay path, CKST and CKSP should be disabled. Otherwise, the continuous sampling will lead to the output results of all zeros again. This function can be accomplished by using the first bit of conversion results (ST_0 and SP_0) because it will always become high after the START and STOP signals are enabled.

The clock pulse (CKP) for the counter can also be obtained via the ST_0 and SP_0 signals with proper timing alignment. The counter can be implemented in synchronous or ripple manners. The MSB of the counter can be used to extend the dynamic range by external counters if MSB is accessible from the chip directly.

4. CHIP LAYOUT AND SIMULATION

This TDC chip is designed by Cadence Virtuso environment provided by Chip Implementation Center (CIC) of National Science Council. The layout diagram is shown in Fig. 8. The core area occupies 1020 x 660 um^2. From post simulation results by using Hspice, the parasitic inductance from the bonding wire and leadframe of package is the main cause of the supply noise. Decoupling capacitance and double-bonding wires on power pads are added to reduce the unwanted parasitic effect.

The jitter caused by the supply noise will affect the differential non-linearity (DNL) and integral non-linearity (INL) in the fine conversion. The simulated results, performance and specification based on matched devices are illustrated in Fig. 9 and Table 1.

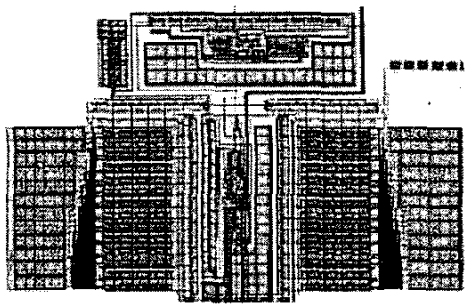

Figure 8. Layout diagram of the proposed TDC

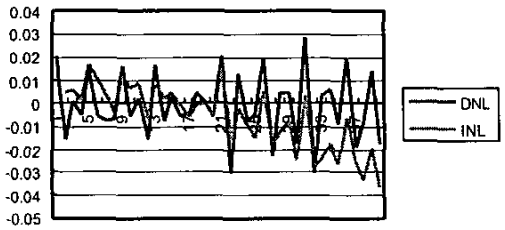

Figure 9. DNL and INL in fine conversion

Operating Voltage	3.0V~3.6V	
Temperature	-20°~+60°	
Reference Clock	Up to 400MHz	under typical condition
LSB	$T_{REF}/40$	62.5ps @ 400MHz
Conversion Time	$< T_{REF}^{-1}$	<2.5ns @ 400MHz
Current Consumption	< 30mA	

Table 1. Performance Summary

5. CONCLUSION

In this paper, a high-resolution and fast-conversion TDC has been proposed and simulated. With the aid of the technique of gate delay difference, the TDC can achieve a sub-gate resolution. The flash-type operation enables the TDC to resolve the time difference for fine conversion in less than one reference clock cycle. Post-simulation shows the DNL can be less than ±0.03LSB and INL less than ±0.04LSB. The chip of the proposed TDC is implemented with 0.35um CMOS process technology. The layout area of TDC core is 1020 x 660 um^2.

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