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A 6.25 mm^2 2.4 GHz CMOS 802.11b Transceiver

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SUMMARY This CMOS transceiver IC exploits the superheterodyne architecture to implement a low-cost RF front-end with only 6.25 mm^2 die area for IEEE 802.11b standard. The transceiver is implemented in 0.25 μm CMOS process with 2.7 V supply voltage, and achieves a −86 dBm 11 Mb/s receive sensitivity and a 2 dBm transmit output power.

key words: *802.11b, CMOS RF transceiver, image-reject mixer, 2.4 GHz transceiver, filter reuse, IF circuits reuse*

1. Introduction

Wireless local-area network (WLAN) is a fast growing market driven by the insatiable demand for high-speed wireless connectivity and increasing availability of cost-effective standards-based interoperable products. WLAN applications include: (1) the seamless connectivity of network inside the home for broadband internet sharing; (2) the extension of the wired Ethernet to wireless mobile devices in the enterprise; and (3) the increasing deployment of wireless accesses in the public areas such as airports and hotels. Furthermore, the core technology has applications in the fixed wireless space enabling cost-effective wireless broadband network between buildings and into the homes.

In the 2.4 GHz ISM band, two prominent wireless LAN RF data link standards are 802.11b and 802.11g. They differ distinctly from one another and demand different levels of RF specification. The 802.11b WLAN is a direct sequence spread-spectrum system with CCK modulation, but the 802.11g is a QAM-based OFMD system, which requires high linearity in RF front/rear-ends and a low phase-noise synthesizer. From the system cost point of view, 802.11b has an advantage over 802.11g. Comparing the RF transceiver on 802.11b [1] with the 802.11g design [5], the 802.11g transceiver requests good modulator (demodulator) I/Q matching, thus extra I/Q gain and phase tuning circuits have to be added in the transceiver design. The penalties of these circuits are the hardware overhead and current consumption. On the baseband processor design, both 802.11g and 802.11b require CCK modem, but OFDM modem is only required in 802.11g for high data rate transmission. Due to these hardware overheads, the 802.11g standard is not as cost effective as the 802.11b when the applications only request a data rate less than 11 Mb/s.

This paper extends the work in [1] by giving a more detailed description on a CMOS transceiver designed for IEEE 802.11b standard. The single-chip transceiver IC is fabricated in a 0.25 μm CMOS technology with a power supply of 2.7 V, and the fully integrated design occupies a very small die area of 6.25 mm^2.

2. Transceiver Architecture

The most common approaches for the WLAN 802.11b transceiver architecture design are zero-IF [4] and superheterodyne [1]–[3]. The trade-off between these two architectures has been discussed in the literature. This paper demonstrates a lowest cost RF radio for 802.11b. When comparing a zero-IF architecture with a superheterodyne, without an off-chip channel-select filter is one of the big advantages in the zero-IF architecture, but the cost of off-chip filter can be compensated by the lower silicon cost obtained from a design using smaller die area and thus having higher yield. Table 1 shows the architecture and performance comparison on different 802.11b RF transceiver designs.

To minimize the transceiver die size, several methods have been integrated. First, stack inductors [6] are used to replace the one-layer inductors in Low Noise Amplifier (LNA) and transmit preamplifier design; also symmetric inductors are used in VCO and VCO buffer design. Second, dc coupling instead of ac coupling is used in the inter-stage of the circuits. Third, since IEEE 802.11b is a TDD system where receiver (RX) and transmitter (TX) are active on different time slots, well-designed IF and baseband circuits can

Table 1 The architecture comparison on 802.11b RF transceivers.

Ref	Architecture	Sensitivity	Output Power	Die size (mm^2)
[2]	heterodyne	-86dBm	0dBm	7.5
[3]	heterodyne	-87dBm	20dBm	16
[4]	zero-IF	-87dBm	0dBm	9.61
This work	heterodyne	-86dBm	2dBm	6.25

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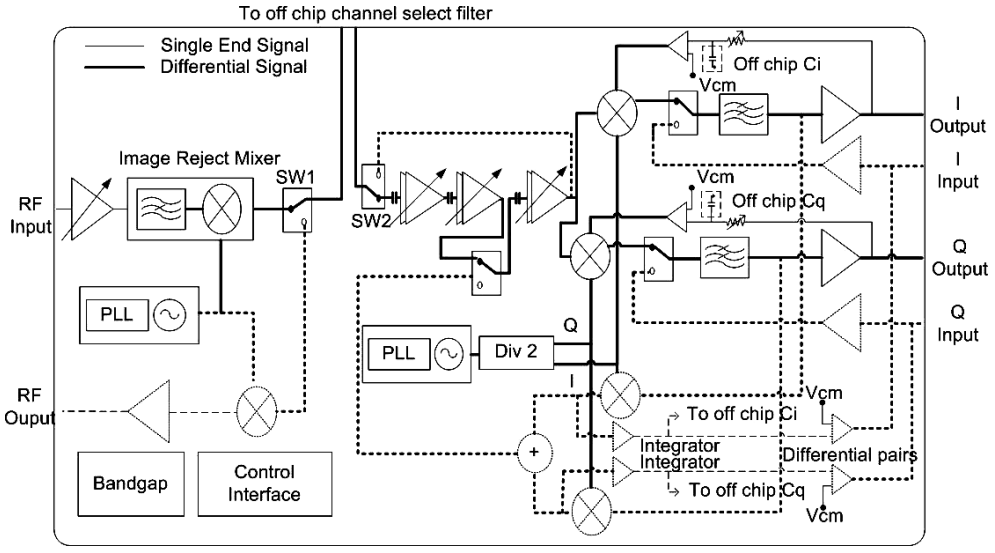

Fig. 1 Transceiver architecture.

be re-used in both the receiving and transmitting paths, thus reducing half of the IF and base-band circuit components. Fourth, a small size image reject architecture is proposed here to reduce the die area.

Figure 1 shows the overall transceiver architecture. Dashed lines are used to represent the transmitter signal path, and solid lines to represent the receiver signal path. The receiver font-end, a single-end input two-stage LNA is followed by an image-reject mixer. An active combiner, which is labeled as SW1 in the figure, is used to drive the off-chip SAW filter. From IF to baseband, the IF signal runs through an active combiner SW2 to a two-mode RX/TX voltage-controlled gain amplifier (VGA). Succeeding the VGA are the in-phase and quadrature down-conversion mixer and two third-order Bessel filters. The VGA and filter are reused in both the receiving and transmitting paths through SW3 and SW4 to reduce the total transceiver die area. A continuous feedback dc offset cancellation loop is designed to remove the output dc offset voltage.

As shown in Fig. 1, the transmitting path starts from an input buffer followed by a RX/TX two-mode Bessel low-pass filter. A traditional Gilbert-cell double-balance mixer is used to up-convert the baseband signal to IF frequency. The TX output power range, which is determined by the dual-mode VGA gain, varies from −23 dBm to 2 dBm. The transmitter shares the same SAW filter with the receiver through the on-chip active combiners SW1 and SW2. The active combiners are designed to have a differential 200 Ω output impedance.

In the transmitter Front-End (FE), a differential-to-single circuit succeeds the Gilbert-cell RF up-conversion mixer to drive the single-ended preamplifier. A two-stage preamplifier is designed to have 15 dB gain and 6 dBm output 1 dB-compression point (P1 dB).

The integer-N RF PLL operates with a 1 MHz reference frequency, which is derived from the system reference frequency provided by an external 44 MHz crystal oscillator. Three additional capacitor arrays parallel to the LC tank are used to extend the RF VCO frequency range up to 280 MHz. The central frequency calibration is performed whenever channel changes. The IF PLL is implemented with an integer-N structure, the reference frequency is the same as the RF PLL. The IF VCO oscillates in 748 MHz frequency and uses a divide-by-two circuit to create the 374 MHz quadrature IF local signal.

3. Circuit Designs

3.1 Receiver

In the receiver chain, a single-end two-stage LNA is shown in Fig. 2. The first LNA stage provides a fixed gain and the second LNA stage provides a gain control function. The first LNA stage uses a common-source amplifier with cascade transistors to maximize the reverse isolation and a degenerated down-bond inductor to achieve the real-part impedance matching. The second LNA stage combines a common-source amplifier with a resistor-based voltage divider. One control bit is used to control the LNA gain through a switch in the second stage, such that the signal will go through a gain or a loss-stage according to this control bit. This method has two benefits for fixing the gain in the first LNA stage. (1) Attenuation network is added in the output of the first LNA stage instead of the input, and a better noise performance can be targeted because the device noise from attenuation network is suppressed by the gain of the first LNA stage. (2) For different gain modes, the bias condition and circuits of the first LNA stage are the same, thus the input impedances of LNA are almost the same in two different gain modes. In general, a worse linearity performance and higher current consumption in low-gain mode are the penalty of the proposed structure. The first LNA stage is turned on when in low-gain mode and the cascade linearity

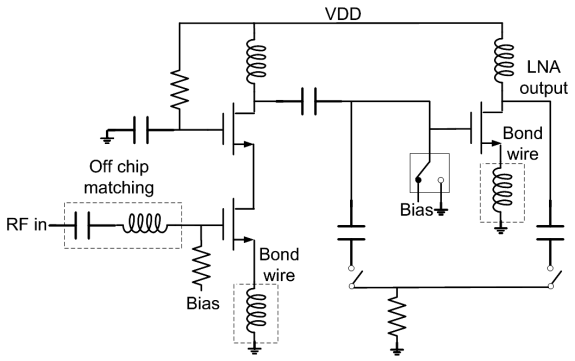

Fig. 2 Two-gain mode LNA circuit.

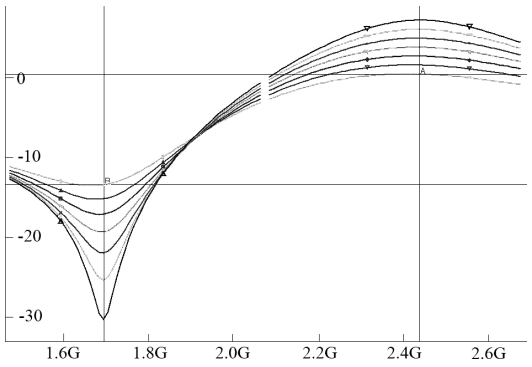

Fig. 4 Simulated frequency response of image-reject mixer.

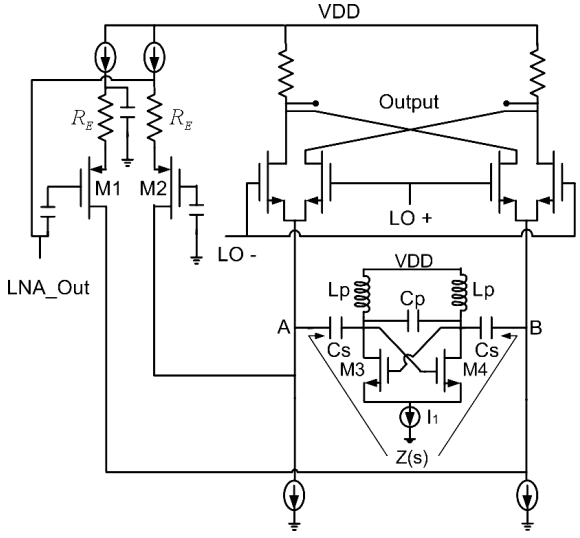

Fig. 3 A proposed single to differential image-reject mixer.

performance is limited by the LNA input device. As well as the degradation of linearity performance, the current consumption of the first LNA stage in low-gain mode is also a disadvantage.

Figure 3 shows the schematic of the RF image-reject down-conversion mixer, where the CS (M1) input is connected with a degeneration resistor R_E and CG (M2) input with a voltage divider R_E and $1/g_{M2}$. Thus, the drain current I_{DM1} of M1 is:

$$I_{DM1} = -\frac{g_{M1}}{1 + g_{M1}R_E} \times V_i \tag{1}$$

And the drain current I_{DM2} of M2 is:

$$I_{DM2} = \frac{r_{M2}}{R_E + r_{M2}} \times g_{M2} \times V_i \tag{2}$$

where

$$r_{M2} = \frac{1}{g_{M2}},$$

g_{M1} and g_{M2} are the transconductances of M1 and M2 respectively. Comparing Eq. (1) with Eq. (2), when $g_{M1} = g_{M2}$, the attitudes of current output I_{DM1} and I_{DM2} are the same but with a phase difference of 180°. This input pair architecture converts a single-ended LNA output to a differential mixer, and thus improves the performance of linearity and gain of the mixer. A 35 dB on-chip image rejection is obtained through the notch mixer design and band-pass characteristic of LNA. The impedance between nodes A and B in Fig. 3 is:

$$Z(s) = \frac{L_p(C_s + 2 \cdot C_p) \cdot s^2 + 1}{L_p \cdot C_s \cdot 2 \cdot C_p \cdot s^3 + C_s \cdot s} \tag{3}$$

The filter has imaginary zeros at

$$w_z = \pm\frac{1}{\sqrt{L_p \cdot (C_s + 2 \cdot C_p)}} \tag{4}$$

and imaginary poles at

$$w_p = \pm\frac{1}{\sqrt{L_p \cdot 2 \cdot C_p}} \tag{5}$$

This circuit was first published by Samavati et al. [7] and used in a differential image-reject LNA design. Given an adequate value on inductor and capacitor, the proposed mixer behaves as a high impedance in desired frequency and a very low impedance in image frequency. Thus the mixer can achieve a maximum gain in desired frequency and a minimum gain in image frequency. The simulated result is shown in Fig. 4. As mentioned in [7], the depth of the notch in Fig. 4 depends on the negative impedance which is generated by the cross-connected differential pair, M3 and M4. The different curves in the figure correspond to different g_{M3} (g_{M4}) conditions. Circuit stability is one of the problems of this notch filter, the image-reject mixer becomes unstable when the net negative admittance of the filter becomes comparable to g_{M3}. Thus the design needs to include the adequate g_{M3} with a trade-off between image rejection performances on the one hand and circuit stability on the other. The notch filter zeros and poles auto-tuning circuits and tank Q tuning circuits are removed here when compared with [7] and [8], respectively. It is the trade-off between circuit performance and die area.

The notch image rejection filter can be placed in the LNA [7]–[9] or the first down-converted mixer [10] of a

high-IF receiver architecture. The proposed receiver architecture here places the notch image rejection filter in the mixer. There are two advantages over the reference designs in [7] and [9] when the notch filter is placed in a mixer instead of an LNA. (1) A single-end LNA uses less current and input matching components when compared with the differential one. Instead of using a differential image-reject LNA [7], we proposed a single-end LNA with a differential image-reject mixer. (2) The notch filter with extra device noise is placed in the mixer instead of the LNA, and thus a better cascade noise performance can be targeted. Comparing our design with the image-reject mixer [10], a cross-connected differential pair is added to the LC tank for tank Q enhancement; given a higher Q, the proposed mixer will deliver a better image rejection performance.

The proposed image-reject architecture can eliminate one mixer and one polyphase filter without considering the in-phase and quadrature local signals; in comparison with the traditional image-reject architecture which uses I/Q mixers followed with a RC polyphase filter, our design has better image rejection performance. The proposed mixer architecture can reduce a lot of die area with an acceptable image rejection performance. An active combiner SW1 is used to drive the off-chip SAW with internal 200 Ω matching.

In the receiver IF chain, signal filtered by the off-chip channel-select filter SAW goes into the chip. An active combiner SW2 is followed with a dual-mode VGA circuit as shown in Fig. 1. The last two stages of VGA are reused in both the receiving and transmitting paths. The VGA has a 60 dB (0–60 dB) control range in RX and a 26 dB range in TX. An ac-coupling RC is added between the two VGA cells to remove the dc offset. Figure 5 shows the proposed VGA cell. Compared with the VGA cell in [11], a source-follow pair is added after the VGA cell and common feedback circuits are used at the source-follow output. These approaches can reduce the parasitic capacitors on the dominant pole of the VGA cell [11]. Thus a higher 3 dB bandwidth and output driving capability can be obtained with the extra bias current on the source-follow pair in our proposed VGA circuit. Succeeding the VGA is a traditional Gilbert-cell double-balance mixer and a third-order Bessel low-pass filter. The filter is implemented in a g_m-C structure; the OTA [12] is designed with an adaptive feedback loop to enhance the filter linearity and performance.

The continuous time dc offset cancellation loop circuitry, as shown in Fig. 6, is designed in the demodulator to remove the dc offset. The proposed dc offset cancellation architecture can eliminate one loop filter compared with the negative feedback structure [13] which senses the forward path differential output for dc offset cancellation. The equivalent mixer input dc offset Δdc_{w_neg} in the negative feedback structure:

$$\Delta dc_{w\_neg} = \frac{A}{1 + A(g_{m\beta}R_{Load\_Mixer})}\Delta dc_{wo} \approx \frac{1}{g_{m\beta}R_{Load\_Mixer}}\Delta dc_{wo} \quad (6)$$

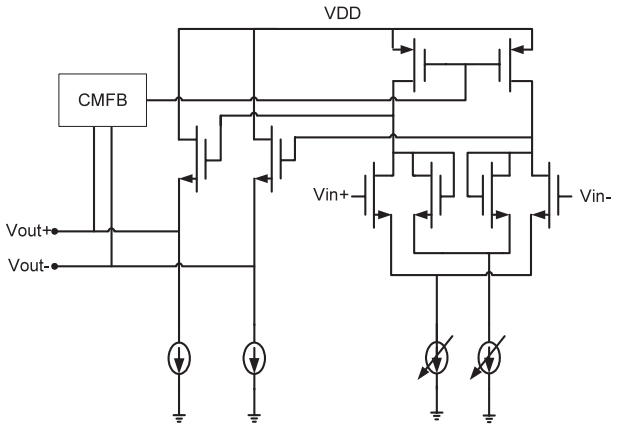

Fig. 5 Variable gain control amplifier cell.

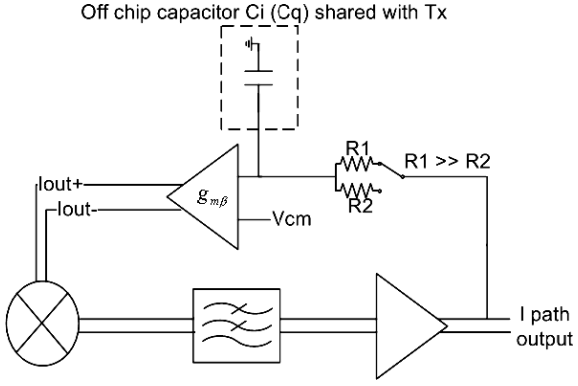

Fig. 6 A simplified receiver dc offset cancellation loop.

Without the dc offset cancellation loop, the equivalent mixer input dc offset voltage is Δdc_{wo}.

In our proposed structure, only one of the differential output dc is extracted, this dc will compare with the common mode dc voltage of differential output, and thus the equivalent mixer input dc offset is:

$$\Delta dc_{w\_our} \approx \frac{1}{\frac{1}{2}g_{m\beta}R_{Load\_Mixer}}\Delta dc_{wo} \quad (7)$$

The dc offset double with the same feedback loop gain $g_{m\beta}R_{Load\_Mixer}$ is the penalty of this structure, but dc offset cancellation performance can be improved by increasing $g_{m\beta}$. An optional close-loop high-pass corner frequency is performed by switching resisters R1 and R2. It is the trade-off between non-significant signal power loss and the dc offset settling time. Whenever the transceiver changes the mode from TX to RX, a switch will connect to a small resistor R1 for fast settling (the dc is always settling within 2 μs), then a switch will change the connection back to a large resistor R2. The final high-pass corner of the loop is about 10 kHz.

3.2 Transmitter

As shown in Fig. 1, the transmitting path starts from the in-

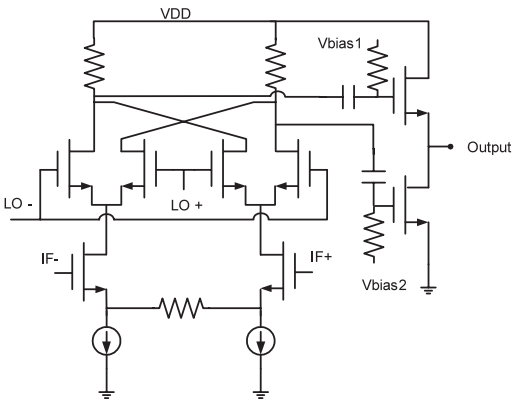

Fig. 7 TX RF up-conversion mixer.

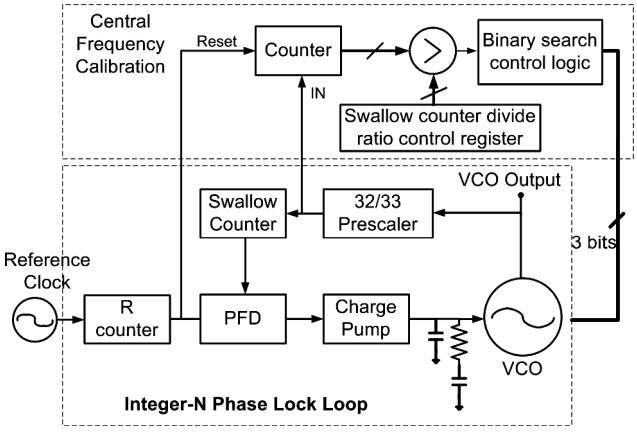

Fig. 8 RF PLL block diagram.

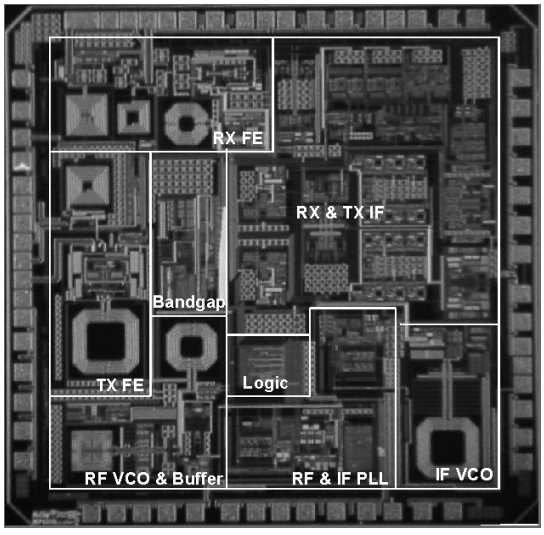

Fig. 9 Die micrograph (2.5 mm × 2.5 mm).

put buffers followed by two Bessel low-pass filters through the switch SW4, and the low-pass filters are reused in the receiver. Two traditional Gilbert-cell double-balance mixers with the same resistor load are used to combine the I and Q signals and to up-convert the baseband signal to IF frequency. The up-converted IF signal goes into VGA through the switch SW3, and the two cascaded VGA cells are used in the transmitting path for gain tuning. The low-pass filter and VGA cell design have already been described in the receiver section.

To eliminate the dc offset in the modulator, a continuous dc offset cancellation loop is used as shown in Fig. 1. The loop behavior as a high-pass filter and the dc gain of the integrator is designed to have a two-gain mode. At the high-gain mode, a higher 3 dB cut-off frequency is designed to target a fast dc offset settling time. At the low-gain mode, a lower 3 dB cut-off frequency is achieved to avoid the data that has been filtered out by the loop. The large off-chip capacitor is shared in the receiver dc offset cancellation loop to reduce one off-chip component and the number of pins.

Figure 7 shows the RF up-conversion mixer design; a differential-to-single circuit succeeds the Gilbert-cell mixer to drive the single-ended preamplifier. Source degeneration resistor is added to improve the circuit linearity. A two-stage preamplifier is designed to have 15 dB gain and 5 dBm output P1 dB.

3.3 Synthesizer

Figure 8 shows the integrate-N PLL architecture. In order to have a large VCO frequency tuning range to cover the process variation and small *Kvco* for good VCO phase noise performance, a 3-bit switch capacitor array is added into the VCO tank. Central frequency calibration circuit is used to determine which VCO curve shall be used. Whenever a channel change occurs, the central frequency calibration circuit will obtain the input from the 32/33 prescaler output. This high-frequency input serves as a clock to count the other low-frequency 1 MHz reference clock input. The counter output will be compared with the swallow counter number which is saved in the register. VCO shall go to a lower oscillation frequency by setting the 3-bit control switch capacitors in the VCO tank when the count number is higher than the swallow counter number, otherwise it shall go to a higher frequency. A binary search is used here, only 3 cycles are needed for a 3-bit control switch capacitor array, and the VCO central frequency calibration time is less than 10 μs. Two cross- coupling pair VCO architectures are respectively used as the RF VCO and IF VCO.

4. Measurement Results

The die microphotograph is shown in Fig. 9 and typical measurement results are summarized in Table 2. The receiver features a noise figure NF=5 dB, the RX front-end (FE) NF and gain performance are shown in Fig. 10. The receiver IIP3 at minimum gain is 0 dBm. The image rejection from our proposed image-reject mixer is higher than 35 dBc. Without an external power amplifier, the transmitter signal error vector magnitude (EVM) is 6.5% at 1 dBm power output. The output mask is shown in Fig. 11. The RF and IF PLLs feature a 1.7degree integrated phase noise

Table 2 Performance summary.

Technology	0.25 um CMOS1P5M
Chip area	6.25mm^2
RX Chain Noise Figure at High Gain Mode	5dB
RX Chain Maximum Gain	103dB
RF&IF VCO Phase Noise at 1MHz	116dBc/Hz & -120dBc/Hz
RX IP3 at High/Low Gain Mode	-30dBm / 0dBm
AGC Gain Range	60dB
TX Output Power	2dBm
LO Leakage	<-30dBc
Side Lobes	<-35dBc
Power Supply	2.7V
RX/TX Current	110mA / 104mA

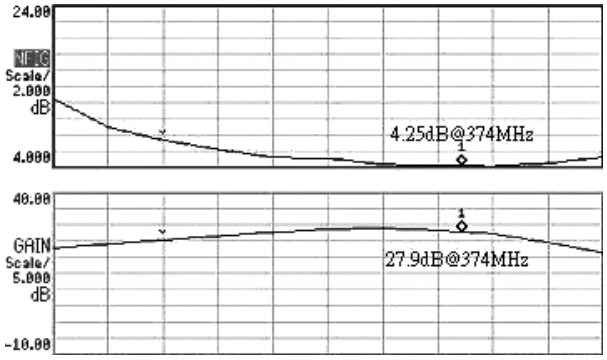

Fig. 10 RX front-end noise figure and gain.

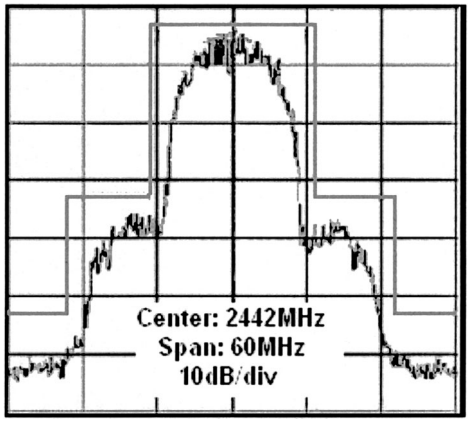

Fig. 11 Transmitter output spectrum for 11 Mb/s data rate.

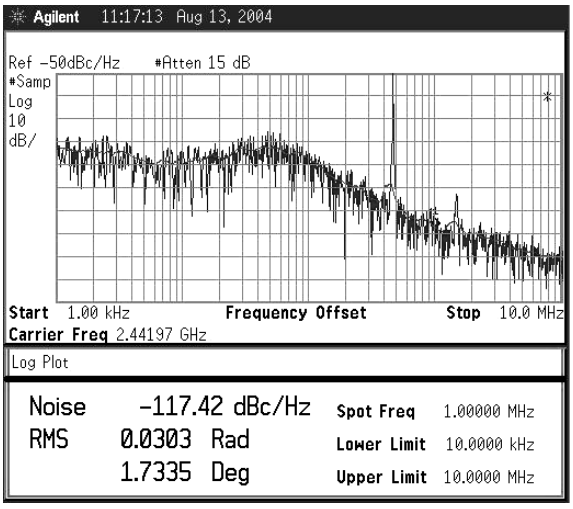

Fig. 12 Integrated phase noise.

from 10 kHz to 10 MHz as shown in Fig. 12. The transceiver exceeds standard specifications by a wide margin.

5. Conclusion

A fully integrated 802.11b transceiver has been implemented in a 0.25 μm CMOS technology. By proposing an innovative architecture and sophisticated circuit designs, we obtained the following advantages: (1) The IF circuits are reused in both the RX and TX chains; (2) A small die size image-reject mixer is achieved; and (3) The use of symmetric and stack inductors reduces the chip area. Therefore, our fully integrated transceiver die size is only 6.25 mm^2, which currently is the smallest 802.11b transceiver compared with other existing designs, as published in [2]–[4].

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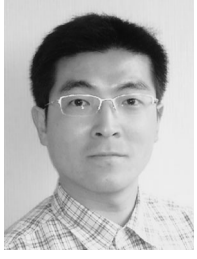

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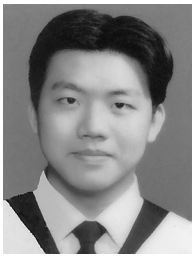

Shin-Ming Lin received the M.S. degrees in Electrical Engineering from the National Taiwan University, Taipei, Taiwan, ROC in 2002. In 2002, he joined the MuChip Co., Ltd., Hsin-Chu, Taiwan to engage in RF circuit including voltage control oscillator, phase lock loop using CMOS technology, and CMOS analog circuit.

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Sao-Jie Chen received the B.S. and M.S. degrees in Electrical Engineering from the National Taiwan University, Taipei, Taiwan, ROC, in 1977 and 1982 respectively, and the Ph.D. degree in electrical engineering from the Southern Methodist University, Dallas, USA, in 1988. Since 1982, he has been a member of the faculty in the Department of Electrical Engineering, National Taiwan University, where he is currently a professor. From 1985 to 1988, he was on leave from National Taiwan University and working toward his Ph.D. at Southern Methodist University. During the fall of 1987, he held a visiting appointment at the Department of Electrical and Computer Engineering, University of Wisconsin, Madison. His current research interests include: VLSI physical design automation, fault-tolerant computing, object-oriented software engineering, and supercomputer architecture design and simulation. Dr. Chen is a member of the Chinese Institute of Engineers, the Association for Computing Machinery, the IEEE, and the IEEE Computer Society.