An Optimization Technique for RF Buffers with Active Inductors

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***Abstract*—A technique of sizing RF buffers is presented to optimize with minimum power dissipation. By using the proposed current-reusing technique, the operating frequency of the RF buffer can be further increased with the same power consumption. The same technique can be also applied to reduce power by a factor of two while keeping the same operating frequency. The analysis is also verified by the circuit simulation.**

I. INTRODUCTION

RF frequency synthesizers usually need to drive many circuits at the same time, such as up/down conversion mixers in both RF transmitters and receivers, shown in Fig. 1.

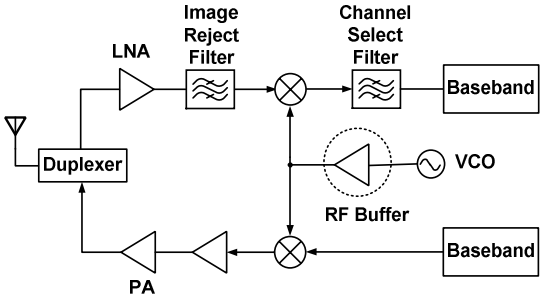

Fig. 1. A simplified RF transceiver architecture shows the necessity of inserting a RF buffer between the frequency synthesizer and mixers.

The voltage controlled oscillator (VCO) in the frequency synthesizer is sensitive to loading effect. If the VCO is an *LC* resonator, large load capacitance reduces the resonant frequency. Thus, the tuning range becomes narrower and the carrier frequency shifts from the desired band. If the VCO is ring-oscillator type, large load capacitance may cause the ring oscillator fail to oscillate and the frequency synthesizer cannot work properly. Thus, inserting a buffer between the VCO and the up/down conversion mixers is necessary.

Adding a buffer can avoid the loading effect described above and can get an additional benefit from the isolation between the synthesizer and other noisy signals that may couple through the mixers. However, the buffer consumes large power to transfer the high-frequency signal to loads because the power consumption is proportional to fCV^2, where f and C are quite significant in GHz operation. Therefore, minimizing the power dissipation of the buffer is a major issue.

An analog filter can be combined in a buffer design to achieve the frequency selectivity. Analog filters can be constructed in many ways using resistors, capacitors and inductors. A parallel *LC* circuit is the bandpass filter prototype. However, passive inductors have the drawback of large size. Therefore, instead of using passive inductors, CMOS filters can incorporate active inductors to save the chip area.

The remains of this paper describe the active filter design strategy using active inductors. Section II is the analysis of the proposed active inductor structure including the method of minimizing the power consumption. Section III is the simulation results, and section IV summarizes with conclusions.

II. ACTIVE FILTER DESIGN

A gyrator with a capacitor C can emulate an inductor in a parallel *LC* filter [1]. Shown in Fig. 2, a gyrator is a G_m cell with a negative G_m cell on the feedback path.

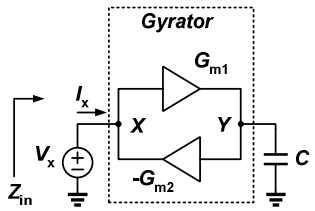

Fig. 2. A gyrator is composed by two transconductance cells.

The effective impedance Z_{in} in Fig. 1 can be derived as Eq. (1)

$$-I_X = -G_{m2}\left(G_{m1}V_X \times \frac{1}{sC}\right)$$
$$\frac{V_X}{I_X} = \frac{sC}{G_{m1}G_{m2}} = sL, \quad (1)$$

where $L = \dfrac{C}{G_{m1}G_{m2}}$.

Equation (1) shows that the effective inductance of a gyrator is inverse proportional to the product of transconductance of the two G_m cells and proportional to the capacitor capacitance C. In RF buffer application, no extra capacitor but only the parasitic capacitance of G_m is at node Y. Therefore, to drive a large capacitive load in an RF buffer application, the inductance should be small enough to tune the center frequency to the desired value, i.e. the transconductance of the G_m cell should be large.

In CMOS technology, the tranconductance can be increased either by using large aspect ratio devices or increasing the bias current but at the cost of more power consumption. Thus, for a limited power consumption constraint, the transconductance can be increased only by using large devices, but large devices induce more parasitic capacitance and lower the resonant frequency however. This contradiction complicates the active inductor design.

The quality factor (Q) of an active inductor is directly proportional to output impedance of the G_m cell [1]. Very high-Q active inductors achieved by cascode devices [2] or Q-enhancement topology [3], [4] are not suitable for RF buffer application because the buffer operates in large signals and large-Q active inductors may cause instability. Also, noise power is Q times worse in a resonant circuit employing an emulated inductor [1]. Thus very high-Q active inductor design is not used. But, if the positive G_m cell in the gyrator is replaced by a simple common-gate amplifier, as shown in Fig. 3, the input admittance Y_{in} is

$$Y_{in} \approx sC_p + \frac{1}{R_s + sL} + \frac{1}{R_p},$$

where

$$C_p = C_{db1} + C_{sb2} + C_{gs2} + \frac{C_Y C_{gd1}}{C_Y + C_{gd1}},$$

$$R_s = \frac{1}{g_{m1} g_{m2} (r_{o2} // R_{oc})},$$

$$L = \frac{C_{gd1} + C_Y}{g_{m1} g_{m2}},$$

$$R_p = r_{o1} // \left(\frac{C_{gd1} + C_Y}{g_{m1} C_{gd1} + g_{m2} C_Y} \right) \approx \frac{1}{g_{m2}}.$$

Thus, the quality factor is poor due to the small equivalent impedance R_p in parallel with the active inductor and the filter provides poor frequency selectivity. Thus, an active inductor with reasonable Q is suitable for RF buffer application.

A. Proposed Active Inductor Design and Analysis

Figure 4 shows the proposed the active inductor design. The differential-to-single-ended amplifier represents the positive G_m cell and the PMOS common-source amplifier forms the negative G_m cell in the gyrator structure. Both G_m cells have large output impedance. Therefore, without using other Q-enhancement circuit, the overall Q factor is still larger than simply employing a common-gate amplifier.

If $M_{2,3}$ and $M_{4,5}$ are perfect symmetric, from Eq. (1), we obtain

$$L_{ind} = \frac{C_p}{g_{m1} g_{m2}}, \tag{2}$$

where C_p denotes the total parasitic capacitance at the drain of transistor M_3.

In order to make the resonant frequency higher, we can increase g_{m1} and g_{m2} by increasing the sizing of the transistors M_1~M_3, but C_p is increased simultaneously. Thus, increasing the transconductance of the two amplifiers by increasing the width of the transistors arbitrarily can not ensure higher resonant frequency

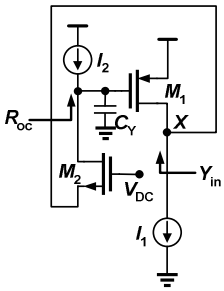

Fig. 3. A gyrator is composed by common-source and common-gate amplifiers.

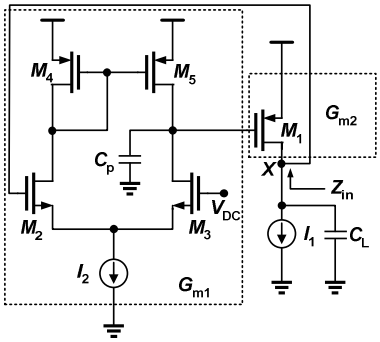

Fig. 4. Proposed active inductor design (only half circuit is shown).

eventually.

The parasitic capacitance C_p consists of the parasitic capacitance of the transistors M_1, M_3 and M_5, and can be written as follows.

$$C_p = C_{gs1} + C_{db3} + C_{db5} + C_{gd1} + C_{gd3} + C_{gd5} \tag{3}$$

Assuming all the transistors operate in the saturation region, the gate-to-drain overlap capacitors are much smaller than the other parasitic capacitors and can be neglected. Thus, expression (3) becomes

$$\begin{aligned} C_p &\approx C_{gs1} + C_{db3} + C_{db5} \\ &\approx \frac{2}{3} W_1 L_1 C_{ox} + \gamma_3 W_3 + \gamma_5 W_5 \\ &= \frac{2}{3} W_1 L_1 C_{ox} + \gamma_2 W_2 + \gamma_5 W_5 . \end{aligned} \tag{4}$$

Equation (4) also uses average capacitance for C_{db3} and C_{db5}. Thus, the junction capacitance is simply proportional to the width of the transistor with a constant coefficient γ, determined by the process parameters.

From Eqs. (2) and (4), the effective inductance becomes

$$\begin{aligned} L_{ind} = \frac{C_p}{g_{m1} g_{m2}} &= \frac{\frac{2}{3} W_1 L_1 C_{ox} + \gamma_2 W_2 + \gamma_5 W_5}{\sqrt{2\mu_p C_{ox} \frac{W_1}{L_1} I_1} \sqrt{2\mu_n C_{ox} \frac{W_2}{L_2} \frac{I_2}{2}}} \\ &= \frac{\frac{2}{3} W_1 L_1 C_{ox} + \gamma_2 W_2 + \gamma_5 W_5}{\sqrt{2\mu_p \mu_n} C_{ox} \times \sqrt{\frac{W_1}{L_1}} \sqrt{\frac{W_2}{L_2}} \sqrt{I_1 I_2}} . \end{aligned} \tag{5}$$

The total capacitance C_x at node X can be estimated as

$$\begin{aligned} C_x &\approx C_L + C_{gs2} + C_{db1} \\ &\approx C_L + \frac{2}{3} W_2 L_2 C_{ox} + \gamma_1 W_1 , \end{aligned} \tag{6}$$

where C_L represents the total load capacitance including

the current source parasitic capacitance. Equation (6) neglects gate-to-drain overlap capacitance also.

If all the transistors have minimum channel length, $L_{\min}$, multiply (5) by (6) we get

$$L_{ind}C_x = \frac{\left(\frac{2}{3}L_{\min}C_{ox}W_1 + \gamma_2 W_2 + \gamma_5 W_5\right)\left(\gamma_1 W_1 + \frac{2}{3}L_{\min}C_{ox}W_2 + C_L\right)}{\left(\frac{C_{ox}}{L_{\min}}\sqrt{2\mu_p\mu_n}\sqrt{I_1 I_2}\right)\sqrt{W_1 W_2}}. \quad (7)$$

The resonant frequency of a parallel LC filter is equal to the reciprocal of the square root of Eq. (7). Because transistor M_5 takes no effect on the transconductance of either G_m cell, minimum width of M_5 should be chosen to minimize the contribution of C_p as long as it can operate in the saturation region. Thus, if power consumption is limited (i.e. I_1 and I_2 both are fixed), only two parameters W_1 and W_2, the width of the transistors M_1 and M_2, are variable. Take partial derivatives on Eq. (7) with respect to W_1 and W_2, respectively, and set both expressions equal to zero.

$$\frac{\partial}{\partial W_1}\left(L_{ind}C_x\right) = 0 \quad (8)$$

$$\frac{\partial}{\partial W_2}\left(L_{ind}C_x\right) = 0 \quad (9)$$

Divide one resulting equation by another and through algebraic simplification, we get

$$W_1\left(\frac{4}{3}L_{\min}C_{ox}\gamma_1 W_1 + \frac{2}{3}L_{\min}C_{ox}C_L + \gamma_1\gamma_5 W_5\right) = W_2\left(\frac{4}{3}L_{\min}C_{ox}\gamma_2 W_2 + \gamma_2 C_L + \frac{2}{3}L_{\min}C_{ox}\gamma_5 W_5\right). \quad (10)$$

Equation (10) indicates that the parameters W_1 and W_2 must meet this constraint equation to minimize $L_{\text{ind}}C_{\text{x}}$ in Eq. (7). Typically, if W_1, W_2 and W_5 are not too large, the term containing load capacitance C_{L} dominates in the parenthesis of Eq. (10), therefore Eq. (10) can be simplified to

$$\frac{2}{3}L_{\min}C_{ox}C_L W_1 \approx \gamma_2 C_L W_2,$$

$$\frac{W_1}{W_2} = \frac{\gamma_2}{\frac{2}{3}L_{\min}C_{ox}}. \quad (11)$$

Equation (11) shows that the width ratio between transistors M_1 and M_2 has a proportional relation with a constant proportional coefficient. This constant can be calculated from the process parameters and approximately equals to unity. Using the above approximation and go back to solve the Eq. (8), we obtain the following solution.

$$W_1 \approx \sqrt{\frac{3}{8}\frac{W_5 C_L \gamma_5}{L_{\min}C_{ox}\gamma_2}} \quad (12)$$

Combine with the Eqs. (11) and (12), the approximation of the optimal sizes that maximizing the resonant frequency can be found.

From another point of view, Eq. (7) can be modified to

$$\sqrt{I_1 I_2} = \frac{\left(\frac{2}{3}L_{\min}C_{ox}W_1 + \gamma_2 W_2 + \gamma_5 W_5\right)\left(\gamma_1 W_1 + \frac{2}{3}L_{\min}C_{ox}W_2 + C_L\right)}{\left(\frac{C_{ox}}{L_{\min}}\sqrt{2\mu_p\mu_n L_{ind}C_x}\right)\sqrt{W_1 W_2}}. \quad (13)$$

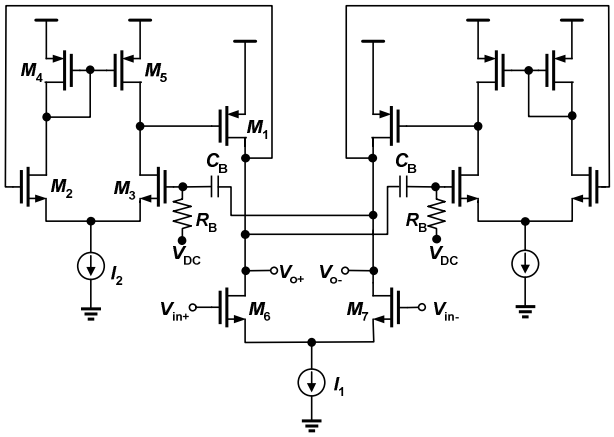

Fig. 5. An RF buffer uses active inductors as loads and the active inductors employ current reusing technique.

$L_{\min}$	0.35 μ m
C_{ox}	4.6e-3 F/m^2
γ_2	1.2363 nF/m
γ_5	1.7442 nF/m
W_5	20 μ m
C_{L}	0.3 pF

Table 1. Parameters used in MATLAB simulation.

For a desired resonant frequency (i.e. LC product value is a given constant) similar to the previous analysis, the optimal width of W_1 and W_2 can be found to minimize (13). Throughout the calculation, the solution still follows (11) and (12). This indicates that while sizing the transistors based on Eqs. (11) and (12), minimum power can be used to produce the desired resonant frequency. This can be a minimum-power-consuming estimation for generating a specific resonant frequency.

B. Current Reusing Technique

If differential signal operation is available or necessary, the resonant frequency can be further increased without consuming additional power by changing the circuit in Fig. 4 as Fig. 5 shows.

In Fig. 5, both input ports of the differential-to-single-ended amplifier connect to small signal inputs $V_{\text{o+}}$ and $V_{\text{o-}}$ which are different from that in Fig. 4, where one input port shorts to AC ground. R_{B} and V_{DC} set the operating points of the G_{m} cells and C_{B} is used to form AC coupling.

The active inductor property remains the same as before, but the effective inductance seen at node $V_{\text{o+}}$ is reduced because the transconductance of the positive G_{m} cell increases by a factor of two due to the out-of-phase signal input now. Thus, change g_{m2} in the Eq. (5) into $2g_{\text{m2}}$, and apply the analysis as section A does, the same results (11) and (12) can be obtained. This means the sizing rules remain the same, but for a prescribed resonant frequency requirement, the power dissipation can be reduced by a factor of two in comparison to the conventional structure by using this technique.

III. SIMULATION RESULTS

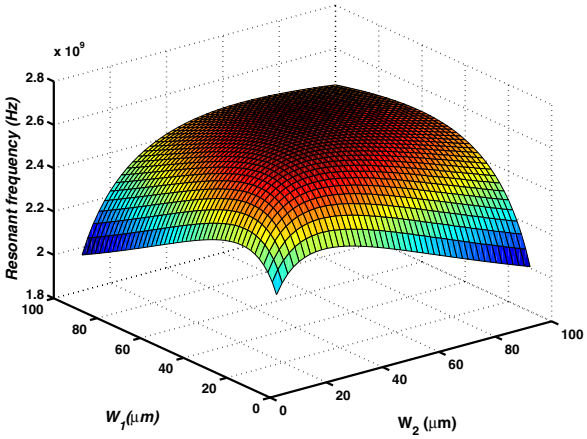

Fig. 6. Numerical plot of the resonant frequency with different transistor sizes.

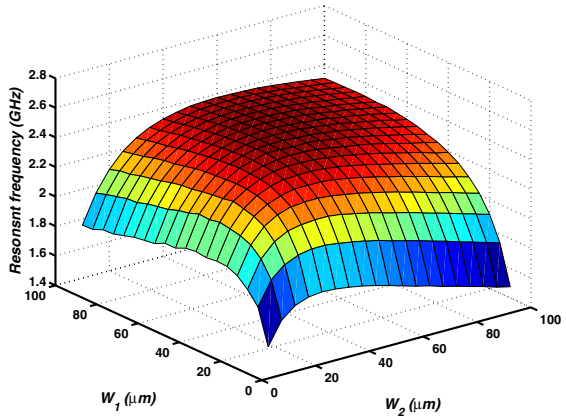

Fig. 7. Resonant frequency from SPICE simulation.

The solutions to the Eq. (7) are the optimal sizes for minimizing the power dissipation. MATLAB is used to predict the actual solutions. Fig. 6 is the plot of resonant frequency based on Eq. (7) with different W_1 and W_2 values, where the process parameters are calculated from the TSMC 0.35-μm CMOS process and summarized in Table 1. From Fig. 6, we find the optimal sizes in this case which are 39.6 μm and 40.7 μm for W_1 and W_2, respectively. The values of W_1 and W_2 calculated from Eqs. (11) and (12) are 44.4 μm and 38.6 μm which are a little different from the actual solutions. But, Fig. 6 shows that the resonant frequency changes little at the points adjacent to the optimal solution. Thus, Eqs. (11) and (12) can predict the solutions of Eq. (7) very well.

Use SPICE to simulate the circuit shown in Fig. 5 but without employing current-reusing technique. Fig. 7 shows the frequency where the buffer has maximum gain with different transistor width. Compared with Fig. 6, in Fig. 7 the resonant frequency varies more slowly with large W_1 and W_2 values. This is because we estimate the gate-to-source capacitance as $2WLC_{ox}/3$. However, this estimation becomes invalid for low V_{GS} as shown in Fig. 8. If the current flowing through the transistor M_1 is fixed, the overdrive voltage of M_1 will decrease by increasing W_1. Thus, for large W_1 values, C_{gs1} makes less

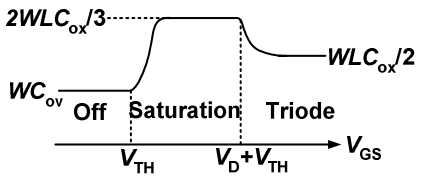

Fig. 8. Variation of gate-source capacitance versus V_{GS}.

contribution to parasitic capacitance as Eq. (4) predicts. As a result, the resonant frequency is less sensitive to the transistor width variation. Although Eq. (7) can not precisely predict the resonant-frequency-variation characteristic with large W_1 and W_2 values, Eqs. (11) and (12) still give good approximation to the optimal sizes.

IV. Conclusions

An RF buffer is used between the frequency synthesizer and its loads. The buffer consumes large power because high operating frequency and large load capacitance. The proposed buffer uses active inductors as a filter in order to provide frequency selectivity. A method for minimizing the power consumption of this buffer design is presented and verified by the circuit simulation. Finally, a current–reusing technique can be applied to save the power up to a factor of two.

Acknowledgement

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