行政院國家科學委員會專題研究計畫　成果報告

毫米波單晶電路之研製(3/3)

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計畫參與人員：王暉、林坤佑、連俊憲、張鴻埜、魏淑芬、涂文化、曾柏森、陳柏佑、陳炳佑、蔡作敏、林晉申、范綱維、王毓駒、雷明峰、張家祺、吳佩&#24985；、林義翔、趙世鋒、林宗良

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行政院國家科學委員會補助專題研究計畫成果報告

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※ **毫米波單晶電路之研製(1/3) (2/3) (3/3)** ※

※Research and Development of millimeter-wave monolithic circuits (1/3) (2/3) (3/3) ※

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計畫類別：☑個別型計畫 □整合型計畫
計畫編號：NSC89-2213-E-002-178
NSC90-2213-E-002-049
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計畫主持人：王 暉
共同主持人：

本成果報告包括以下應繳交之附件：
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☑出席國際學術會議心得報告及發表之論文各一份
□國際合作研究計畫國外研究報告書一份

執行單位：國立台灣大學電信所

中 華 民 國 92 年 12 月 30 日

毫米波單晶電路之研製 (1/3), (2/3), (3/3) 完整報告

Research and Development of millimeter-wave monolithic circuits (1/3), (2/3), (3/3)

計畫編號：NSC89-2213-E-002-178
NSC90-2213-E-002-049
NSC91-2219-E-002-042

執行期限：89 年 8 月 1 日至 92 年 10 月 31 日

主 持 人：王暉　　國立台灣大學電信所教授

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一. 中文摘要(關鍵詞：毫米波，Q-頻段，V-頻段，W-頻段，高速場效電晶體，異質接面雙極性電晶體，單晶微波積體電路。)

本三年期之計畫目標為使用砷化鎵單晶微波積體電路製程技術(0.15 或 0.1 微米之高電子移動率電晶體與 2 微米之異質接面雙極性電晶體)來研製毫米波頻段(Q-band，33-50GH_Z)以上之單晶體電路。所計劃研製之單晶積體之電路，包括放大器、混頻器、震盪器及被動和研製電路，如毫米波切換器、相移器及平衡-不平衡轉換器等。

我們在計畫的第一年中成功地研製出 Q-頻段(33-50GH_Z)之各項積體電路。其中包括 40 GHz 共面波導低雜訊放大器、35-45 GHz 次諧波混頻器、35 GHz 振盪器、Q 頻段單刀雙擲開關

在第二年之計劃中，我們完成了 57-60 GHz 低雜訊放大器、54~64 GHz 次諧波混頻器、55-60 GHz 功率放大器與 15-80 GHz 利用行波(traveling wave)概念所設計之單刀雙擲切換器。

在第三年的計畫中，已完成 W-頻段(75-110 GHz)之積體電路之研製，其中包括 77 GHz 功率放大器、84 GHz 倍頻器、94 GHz 三倍頻器、97 GHz 振盪器與 W 頻段之次協波混頻器。以上單晶積體電路皆已完成量測。

本計畫之積體電路係為應用 CIC 所洽商之美國 TRW 公司之 0.15 微米與 0.1 微米 HEMT，與 GCS 公司之 2 微米 HBT MMIC 製程。

Abstract (Keywords : Millimeter-wave, Q-band, V-band, W-band, HEMT, HBT, MMIC)

This three-year project is proposing the development of monolithic millimeter-wave (MMW) components at Q-band (33-50 GHz) and above using GaAs MMIC process technologies (e.g. 0.15 or 0.1-μm gate-length HEMT, 2-μm HBT), which are available through a certain foreign commercial foundries, coordinated by Chip Implementation Center, National Applied Research Laboratories. The MMIC components will include low noise amplifiers, power amplifiers, mixers and oscillators, as well as some passive and control components, such as MMW switches, phase shifters, and baluns, etc.

The MMIC components development for frequency up to Q-band (33-50 GHz) has been demonstrated in the first year. These circuits include 40-GHz GCPW low noise amplifier, 35-45 GHz subharmonic mixer, 35-GHz oscillator and Q-band SPDT (single-pole-double-throw) switch.

In the second year, we have completed the development of a 57-60 GHz low noise amplifier, a 54-64 GHz sub-harmonic mixer, a 54.5-59.5 GHz power amplifier, and a 15-80 GHz SPDT switch using traveling-wave concept.

In the third year, the W-band MMICs include 77-GHz power amplifier, 84-GHz frequency doubler, 94-GHz frequency tripler, 85-GHz voltage control oscillator and W-band

subharmonic mixer were developed. All the MMICs have been measured.

This research utilized 0.1- and 0.15-μm gate-length HEMT MMIC processes provided by TRW, USA and 2-μm HBT MMIC process provided by GCS, USA through CIC.

二. 研究計畫之背景及目的

Millimeter-wave (MMW) frequency (30-300 GHz) transceiver will play a very import role in the next generation's wireless communication systems. There are many MMW MMIC components, including low noise amplifiers, power amplifiers, mixers and oscillators reported in US, Japan, and European countries [1]-[5] for MMW radar, communication and radiometer applications. In MMW frequency range, In the first year of this project, Q-band MMIC components was demonstrated. This research utilized 0.15-μm and 0.1-μm gate-length pHEMT MMIC process of TRW, and 2-μm HBT MMIC process of GCS also through CIC. The objective of this project is to establish the design and modeling techniques for MMW MMIC up to W-band frequency using accessible MMIC processes and to train qualified personnel's (student and/or engineer).

三. 研究方法與結果

In this research, the procedures of MMW MMIC development is presented as follows.

1) **Establish design goal of each component.** The design goal of each component need to be determined by certain system requirements. Before the design starts, the system application and the detail design goal will be identified.

2) **Device model investigation.** For each solid-state device, the device figure of merit (FOM) need to be calculated in order to decide the circuit topology, e.g., f_T, f_{max}, maximum available gain of the transistor and cut-off frequency of the diode. For those devices that the models are not available, we need to perform the device dc and RF characterization and generate the models.

3) **Passive model library establishment.** Mainly for some special structures, e.g. power dividers/combiners, 90^o and 180^o couplers, baluns and etc. The goal will be targeted for miniature size.

4) **Circuit topology trade study and initial circuit design.** After the device FOM is obtained, the gain stage number of amplifiers can be determined. Regarding the mixer topology, sub-harmonic mixer is preferred in this project since it can use low frequency low phase noise source without frequency multiplication. The design approach of other components will be also determined via certain FOM and trade-off considerations.

5) **Circuit simulation, detailed design and layout.** In MMW frequency, the EM analysis of entire matching structure may be needed.

6) **Circuit fabrication and evaluation.** We share the R&D mask with CIC of National Science Council and get the chip fabricated using the 0.15- and 0.1-贡m PHEMT MMIC processes (provided by TRW). For circuit testing, on-wafer probing is planned to avoid the complicated fixture test.

The results of this project are described as follow.

Q-band MMICs

LNA Fig. 1 shows the chip photo of the monolithic 40GHz CPW LNA, with a chip size of 3 mm × 2 mm. The three-stage LNA was designed using CPW transmission lines. The 4-finger 120 μm PHEMT was used for each stage. Drain short stubs use as feedback inductors to improve the stability. Fig. 2 shows the measurement result of small-signal gain and input return loss. In 37 to 43 GHz over 21 dB gain and 10 dB input return loss was achieved. The output return loss is better than 10 dB. The result is shown in Fig. 3.

Mixer Fig. 4 shows the chip photo of the sub-harmonic mixer, with a chip size of 1.5 mm × 1 mm. Using anti-parallel diode to produce the LO second harmonic power. Quasi-lumped stubs replace the quarter wave open stubs and short stubs and good isolation between RF and LO. Fig. 5 illustrates the conversion loss measurement result of the mixer. The conversion loss is less than 15 dB in 35 GHz ~ 45 GHz.

VCO Fig. 6 shows the chip photo of the 35 GHz VCO, with a chip size of 3 mm × 1 mm. The total gate width of transistor is 200 μm. MIM capacitor is RF bypass and DC block. Short stubs are used in gate and source as the feedback circuit. The match circuit contains open stubs, short stubs and coupled lines Fig. 7 presents the measurement result of the output power and output frequency, 10 dBm output power and 0.8 GHz tuning range are achieved. Fig. 8 shows the spectrum of the VCO output.

Switch Fig. 9 shows the chip photo of the Q-band SPDT switch with a chip size of 1 mm × 2 mm. Fig. 10 is the measurement insertion loss and isolation. Over 30-dB isolation is achieved and it has about 2 dB insertion loss at 40 GHz. The results of this switch were published in [9].

V-band MMICs

LNA Fig. 10 shows the chip photo of the monolithic V-band LNA, with a chip size of 1.5 mm × 1 mm. The two-stage single-ended LNA was designed using microstrip line. The 4-finger 40 μm PHEMT was used for each stage. Source inductors were added for the stability concern. MIM capacitors are used for RF bypassing and DC blocking. Fig. 11 shows the measurement results of small-signal gain and input/output return losses. From 57 to 60 GHz over 12-dB gain was achieved.

Mixer The anti-parallel diode pair was used to design the sub-harmonic mixer. Quasi-lumped stubs replace the quarter wave open stubs and short stubs to provide good isolation between RF and LO [6]. The coupled line filter is used to isolate the IF signal to RF port. The low-pass filter composes of high-impedance transmission line and capacitor improves the RF-to-IF isolation. Fig. 12 shows the chip photo of the V-band sub-harmonic mixer, with a chip size of 1 mm × 1 mm. Fig. 13 illustrates the conversion loss measurement results of the mixer. The conversion loss is about 15±5 dB in 54 GHz ~ 64 GHz.

PA This power amplifier is a two-stage, single-ended design. The total output gate periphery is 320 μm combined of four transistors, and the gate width of the drive stage is 80 μm. MIM capacitors are used for RF bypassing and DC blocking. The low impedance lines are used in the matching circuits of the output stage. Fig. 14 shows the chip photo of the V-band power amplifier, and the chip size is 3 mm × 1 mm. Fig. 15 presents the measurement results of the small-signal performances. From 54.5 GHz to 59.5 GHz, the measured small-signal gain is better than 12 dB, and the input/output return losses are better than 3.6 dB/4.5 dB.

Switch Some broadband SPDT switches were report previously [7], [8]. The SPDT switch was designed using traveling-wave concept. When the passive HEMTs shunt to a transmission line, the whole circuit can be treated as lossless and lossy transmission lines corresponding to the OFF and ON states of the transistors, respectively. Since ON-state resistance is very small, lossy transmission line is nearly equivalent to short circuit. On the other hand, the lossless transmission line is equivalent to a 50-Ω transmission line after suitably choosing dimension of the transmission line. Quarter-wavelength transformer series to artificial transmission line is a transition of lossy line from nearly short to nearly open. The four-finger 80-μm transistor is used in this SPDT MMIC switch design. Fig. 16 shows the chip photo of the 15-80 GHz SPDT switch with a chip size of 1.5 mm × 1.5 mm. Fig. 17 shows the measurement results. The insertion loss and isolation are better than 3.6 dB and 25 dB, respectively from 15 GHz to 80 GHz. This circuit was reported in [10].

W-band MMICs

PA This power amplifier was designed using 0.1-μm GaAs HEMT process. The gate peripheries of the first and output stages are 320 and 640 μm, respectively. Fig. 18 shows the chip photo with a chip size of 3 X 2 mm^2. The output stage is in balanced structure by using the Lange couplers, and the first stage is single end. Fig. 19 shows the on-wafer measured small-signal characteristics. The small-signal gain is above 10 dB and input/output return losses are better than 5 dB from 75 to 80 GHz. The power performance was tested in a packaged module, at 77 GHz, the P_{1dB} (1-dB compression power point) and P_{sat} (saturation power) are 18.5 and 21.5 dBm, respectively.

Doubler The doubler is a microstrip line design,

and the device is 4-finger, 120-μm HEMT. The output matching is for maximum second harmonic power transferring, and a radial stub is used to provide a short circuit for second harmonic frequency at the output. Fig. 20 shows the chip photo of the W-band doubler with a chip size of 1 x 1 mm^2. The measured conversion gain is between -2.3 and -7 dB while the input power is 3 dBm, and the measured conversion gains with 0- and 3-dBm input power are shown in Fig. 21.

Tripler This frequency tripler was implemented by anti-parallel diode pair (APDP) using GaAs HEMT process. The diode size of this circuit is 4-finger, 28 μm. Fig. 22 shows the chip photo of the tripler with a chip size of 1.5 x 1 mm^2. A quarter-wavelength open stub is used to provide a short circuit at third harmonic frequency, and a band-pass filter at output is used to reject the fundamental frequency signal. Fig. 23 shows the measured conversion loss of this frequency tripler with 10-, 12- and 14-dBm input power level. The conversion loss is better than 20 dB from 87 to 102 GHz while the driving power is 14 dBm. The results of this frequency tripler were reported in [11].

VCO This W-band GCPW (grounded coplanar waveguide) VCO was designed using 0.1-μm GaAs HEMT process, and the device size in this VCO is 4-finger 80 μm. Fig. 24 shows the chip photo with a chip size of 1.5 x 1 mm^2. The measured output spectrum of the VCO is shown in Fig. 25, and the output power is -0.5 dBm while the frequency is 97.12 GHz. The phase noises at 1-MHz offset is -88 dBc/Hz. The output signal frequency of this VCO is controlled by the gate voltage, and the tuning range is about 2 GHz centered at 97 GHz while the gate voltage is from -0.4 to 0.3 V. This W-band VCO will be present in the 2003 European Microwave Conference (EuMC) [12].

Mixer The W-band mixer was fabricated using GCS 2-μm HBT MMIC process. In this design, quarter-wavelength open-stub and short-stub at each end of the diodes pair are also utilized to achieve good isolation between LO and RF ports. LO port matching is obtained by reactive matching techniques using microstrip-lines while RF port matching is obtained with a coupled line filter. The short stub in the matching network also acts as a dc return of the circuit. Fig. 26 shows the chip photo of this mixer with a chip size of 1 x 1 mm^2. The measured conversion loss while the LO frequency is 42.5 GHz with 10-dBm power level. The conversion loss is better than 18.5 dB from 86 to 104 GHz.

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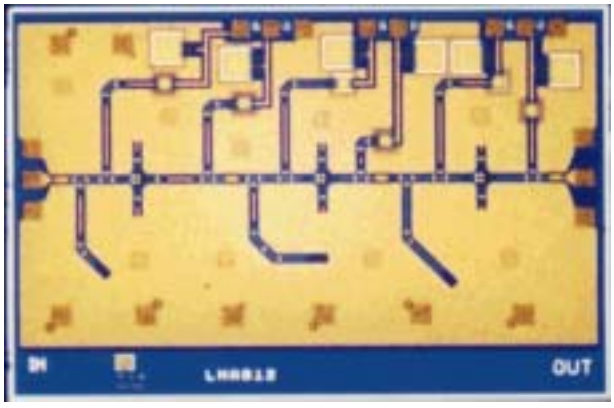

Fig. 1. Chip photo of the 40 GHz CPW LNA.

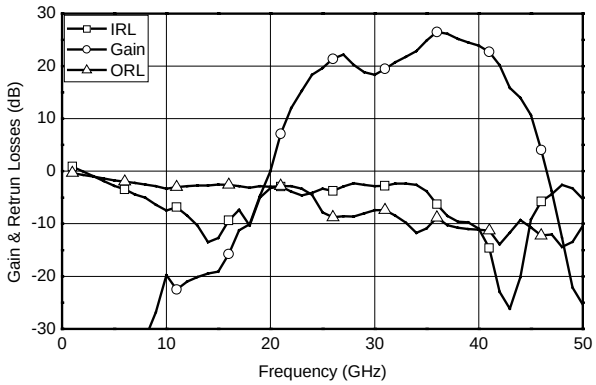

Fig. 2. Measured small-signal of gain and input return loss.

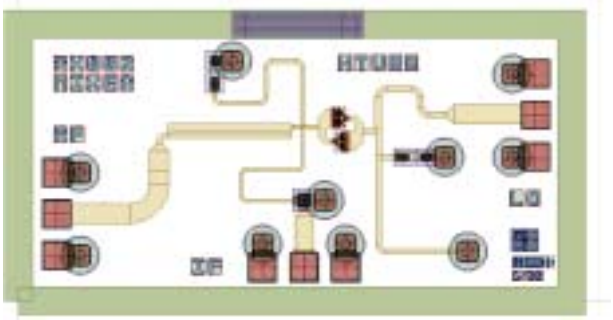

Fig. 3. Chip layout of the 35-45 GHz sub-harmonic mixer.

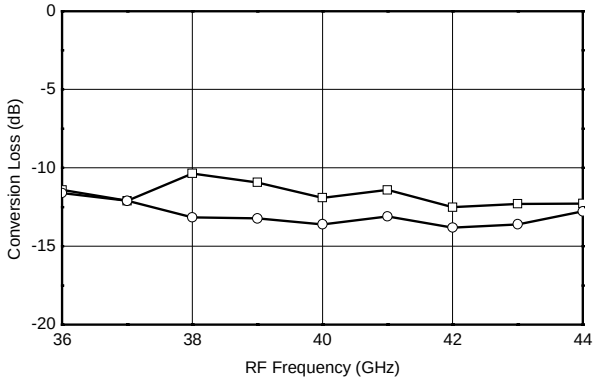

Fig. 4. Measured conversion losses of the 35-45 GHz sub-harmonic mixer.

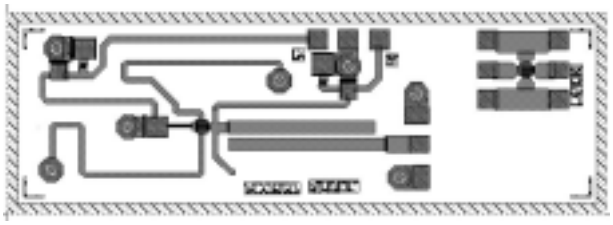

Fig. 5. Chip layout of the 35 GHz VCO.

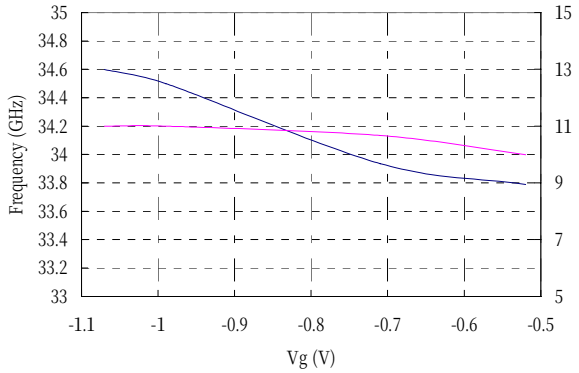

Fig. 6. Measurement result of output power and output frequency to tuning voltage

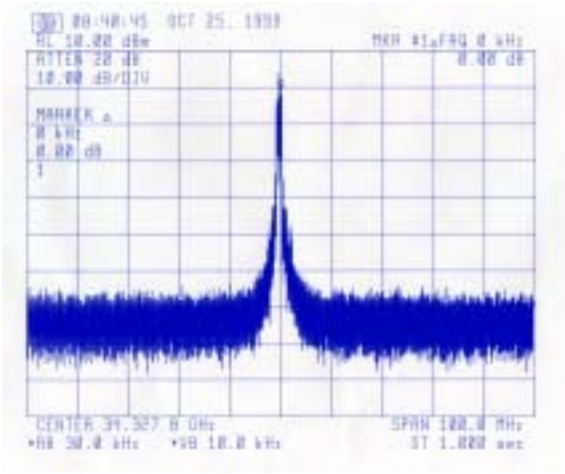

Fig. 7. Spectrum of the VCO output.

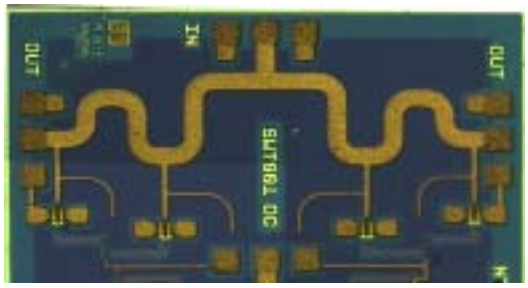

Fig. 8. Chip photo of the Q-band Switch.

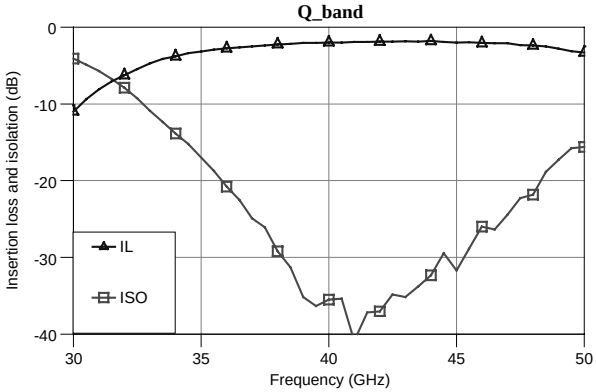

Fig. 9. Measurement insertion loss and isolation of the Q-band Switch.

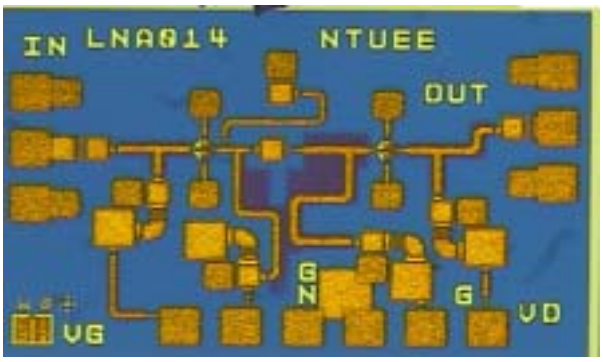

Fig. 10. Chip photo of the V-band low noise amplifier.

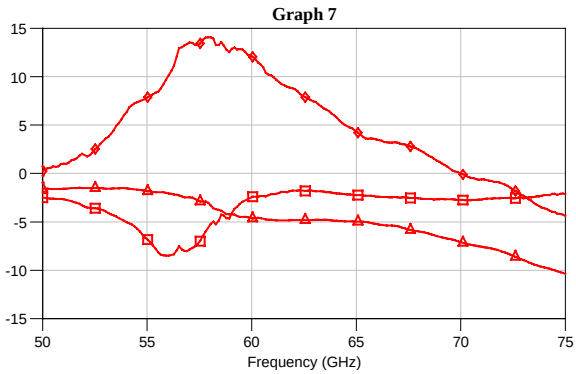

Fig. 11. Measured small-signal performances of the V-band low noise amplifier.

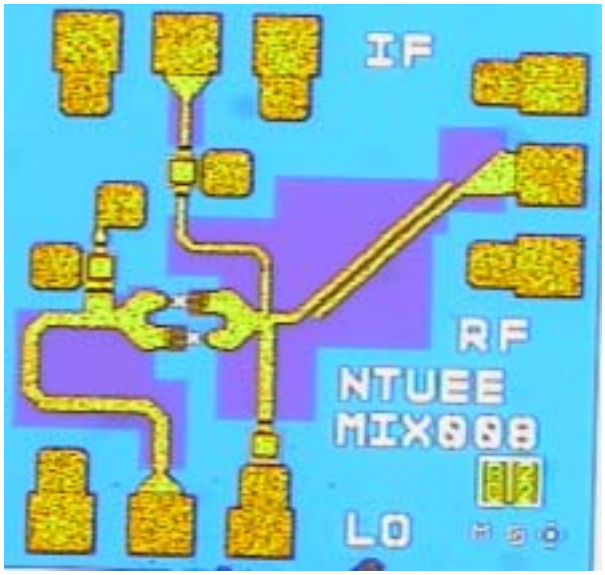

Fig. 12. Chip photo of the V-band sub-harmonic mixer.

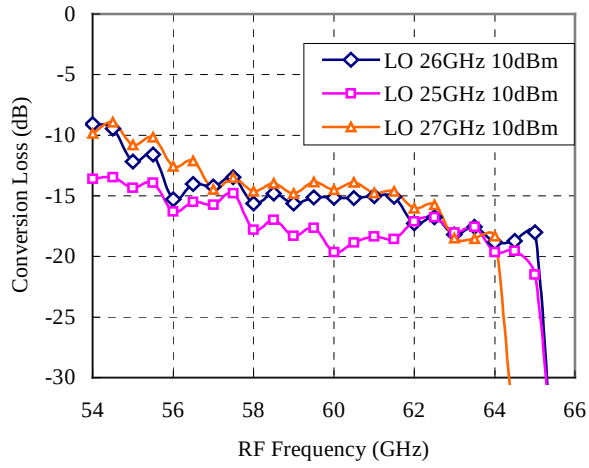

Fig. 13. Measured conversion loss versus RF frequency of the V-band sub-harmonic mixer.

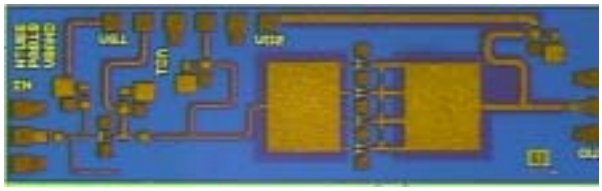

Fig. 14. Chip photo of the V-band power amplifier.

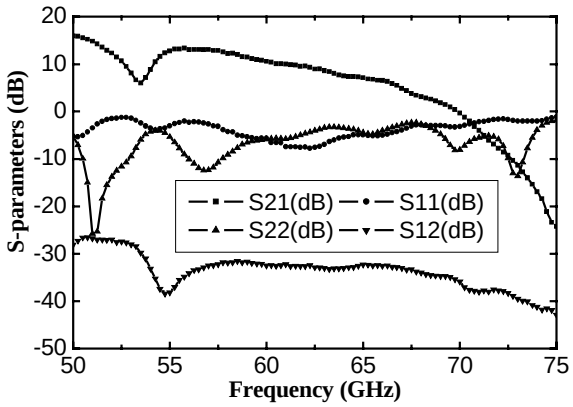

Fig. 15. Measured small-signal performances of the V-band power amplifier.

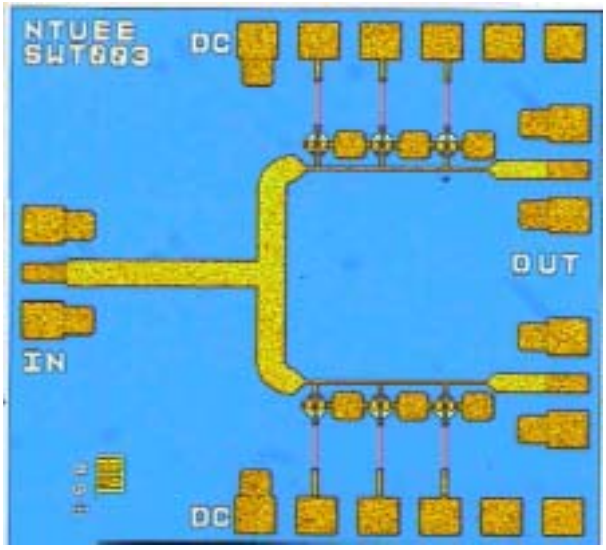

Fig. 16. Chip photo of the SPDT switch using travelling-wave concept.

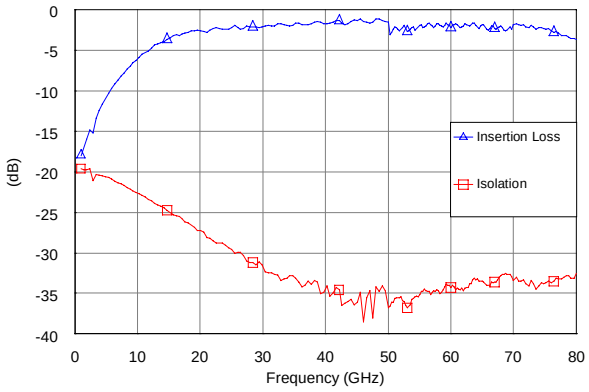

Fig. 17. Measured insertion loss and isolation of the 15-80 GHz switch.

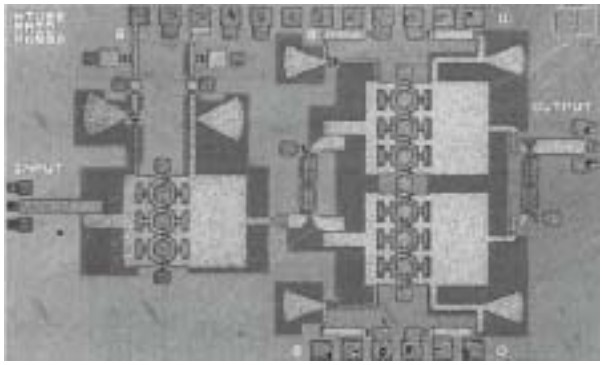

Fig. 18. Chip photo of the 77-GHz power amplifier.

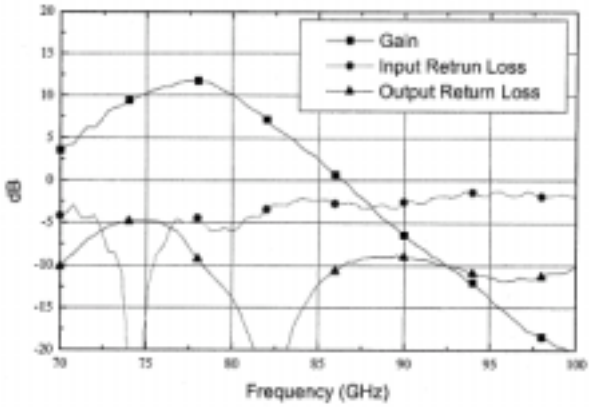

Fig. 19. Measured small-signal gain and return losses of the 77-GHz power amplifier.

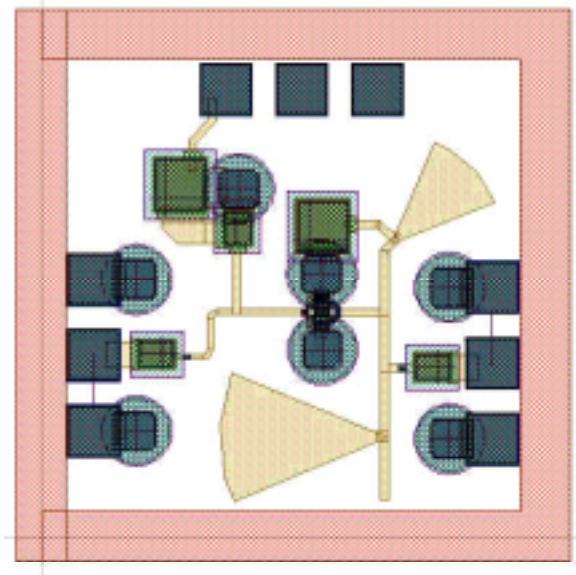

Fig. 20. Chip layout of the W-band doubler with a chip size of 1 x 1 mm^2.

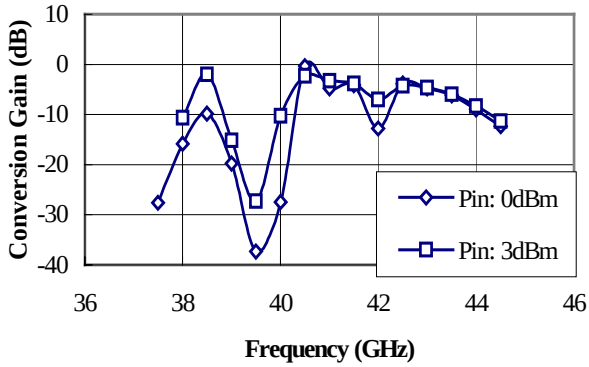

Fig. 21. Measured conversion gain versus input frequency of the W-band doubler.

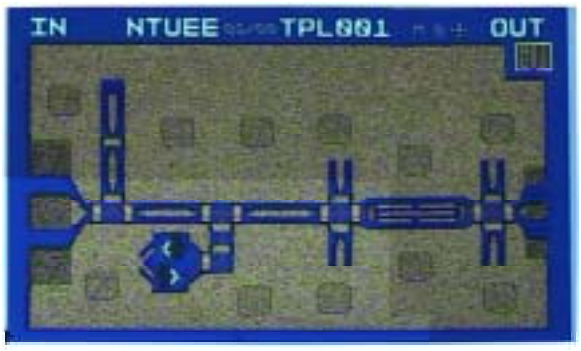

Fig. 22. Chip photo of the W-band tripler with a chip size of 1.5 x 1 mm^2.

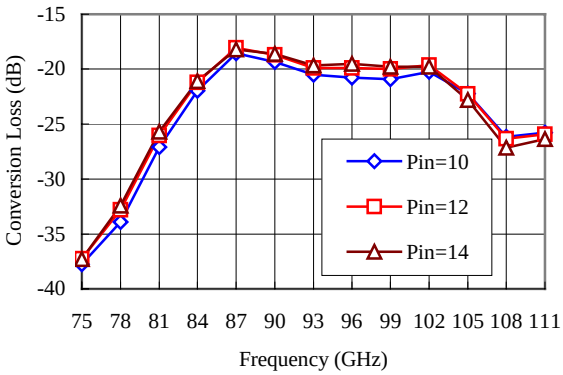

Fig. 23. Measured conversion loss versus output frequency of the W-band tripler.

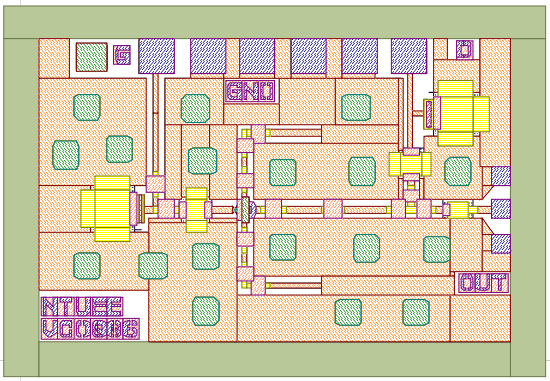

Fig. 24. Chip layout of the W-band VCO.

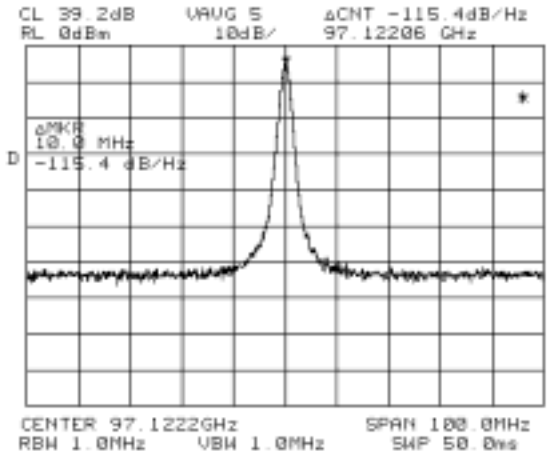

Fig. 25. Measured output spectrum of the W-band VCO.

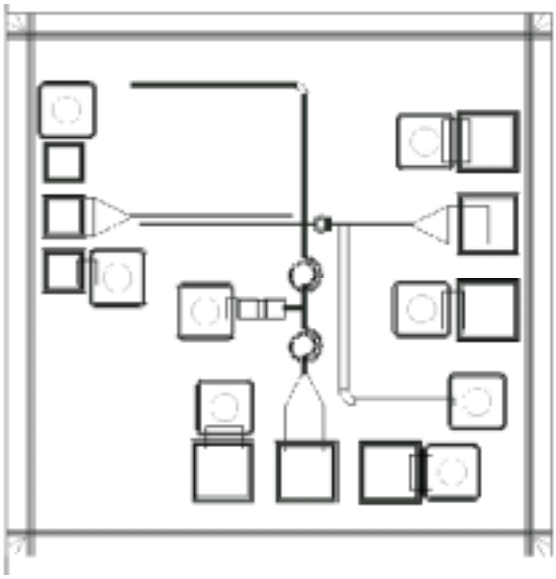

Fig. 26. Chip layout of the W-band subharmonic mixer.

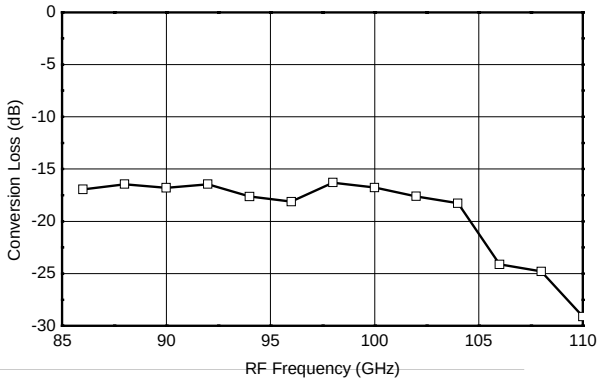

Fig. 27. Measured conversion loss of the W-band subharmonic mixer.