A Double-Sampling Pseudo-Two-Path Bandpass $\Delta\Sigma$ Modulator

Shen-Iuan Liu, Chien-Hung Kuo, Ruey-Yuan Tsai, and Jingshown Wu

***Abstract*—A double-sampling pseudo-two-path bandpass $\Delta\Sigma$ modulator is proposed. This modulator has an output rate equal to twice the clock rate, uses $n/2$ operational amplifiers (op-amps) for an nth-order noise transfer function, and has reduced clock feedthrough in the signal path band. The required clocks can be simpler to implement than the conventional pseudo-two-path techniques. The measured signal-to-noise ratio and dynamic range of the fourth-order double-sampling pseudo-two-path bandpass $\Delta\Sigma$ modulator in a 30-kHz bandwidth at a center frequency of 2.5 MHz (at a clock frequency of 5 MHz) are 62 and 68 dB, respectively.**

***Index Terms*—Bandpass $\Delta\Sigma$ modulator, double sampling, pseudo-two-path.**

I. Introduction

In modern wireless communication systems, the increasing progress in CMOS technology has made it possible for applications not only for digital signal processing in the baseband but also for analog signal processing in the intermediate-frequency (IF) and radio-frequency bands. Bandpass $\Delta\Sigma$ modulators [1] provide a method for performing analog-to-digital conversion of IF signals. There exist many methods to realize switched-capacitor bandpass such as the LDI and FE types [2], the two-delay type [3], the low-pass filter synthesis type [4], the high-pass filter synthesis type [5] and the pseudo-two-path type [1], [6]. The two-delay type [3] uses two delay cells in a negative feedback loop to realize $z^{-2}/(1+z^{-2})$. Since half the period is idle, it can be used for double sampling. However, the LDI and FE types as well as the two-delay type require four op-amps to realize a fourth-order bandpass $\Delta\Sigma$ modulator. The low-pass filter synthesis method [4] uses a low-pass filter $z^{-2}/(1-z^{-2})$. It appropriately changes the input and output polarities to synthesize a bandpass filter $-z^{-2}/(1+z^{-2})$. The required number of op-amps is reduced by half, since the same op-amp is shared. The high-pass filter synthesis [5] uses a pair of high-pass filters with $z^{-1}/(1+z^{-1})$ and utilizes the time-multiplexed technique to realize $z^{-2}/(1+z^{-2})$. A new double-sampling, pseudo-two-path bandpass $\Delta\Sigma$ modulator requiring a reduced number of op-amps is presented in Section II. Circuit implementations are given in Section III, and the measured results are discussed in Section IV.

II. Circuit Description

Since the pseudo-N-path (PNP) filter has only one physical path, it can overcome the sensitivity due to path mismatch. Ghaderi *et al.* [7] proposed a circulating-delay-type filter and a RAM-type PNP filter, which are suitable for narrow-band bandpass filters. Since there is a noise peak in the center of the passband, several improved versions were presented [8]–[10].

The double-sampling technique [11]–[13] is an efficient way to increase the oversampling ratio (OSR) by a factor of two in a $\Delta\Sigma$ modulator without increasing the clock rate, the settling time and dc gain of op-amps, etc. The proposed double-sampling bandpass $\Delta\Sigma$ modulator is described as follows:

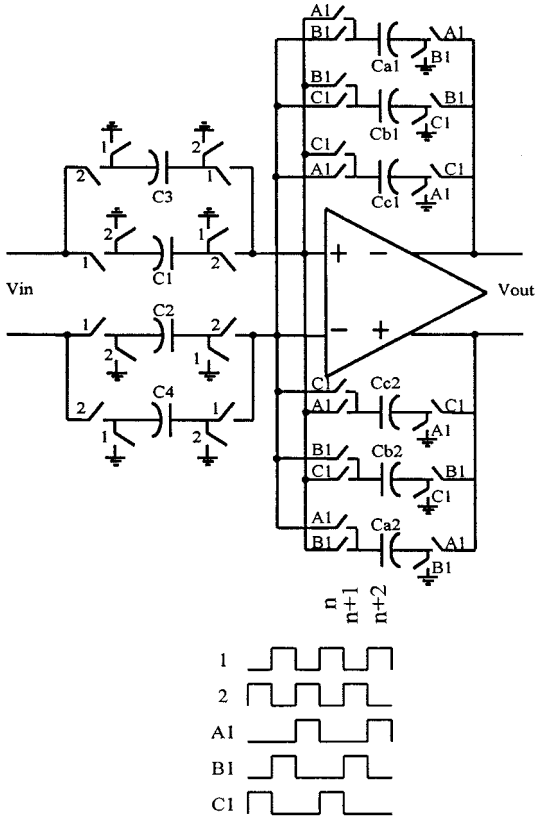

Fig. 1. The proposed double-sampling pseudo-two-path bandpass filter.

A. Double-Sampling Pseudo-Two-Path Bandpass Filter

Fig. 1 shows the proposed double-sampling pseudo-two-path bandpass filter and its clock phases: clk1, clk2, clkA1, clkB1, and clkC1. Capacitor pairs $(C1, C2)$ and $(C3, C4)$ are the sampling capacitors, which are sampled at clk1 and clk2, respectively. Capacitor pairs $(Ca1, Ca2), (Cb1, Cb2)$ and $(Cc1, Cc2)$ are the storage capacitors. To analyze the proposed circuit, Fig. 1 has been divided into three equivalent circuits according to the clock phases, clkA1, clkB1, and clkC1, as shown in Fig. 2(a)–(c).

Assume that all the values of the capacitors are identical. For the circuit in Fig. 2(a), at time n, clk1 is high,

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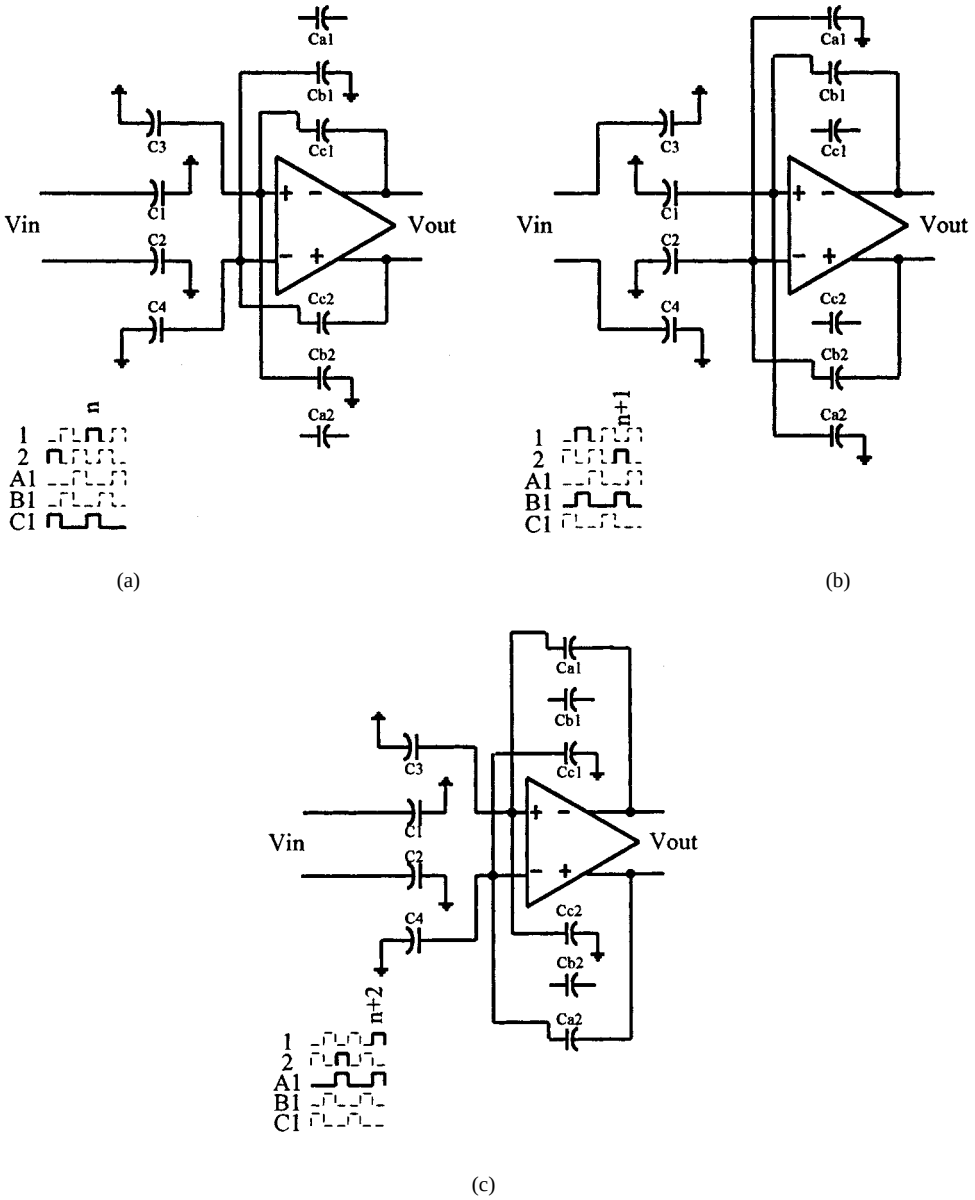


Fig. 2. (a) Clock phase clkC1. (b) Clock phase clkB1. (c) Clock phase clkA1 of Fig. 1.

clk2 is low, and clkC1 is high. The input voltage $v_{\text{in}}(n)$ is sampled to the capacitor pair $(C1, C2)$. The capacitor pairs $(C3, C4)$ and $(Cb1, Cb2)$ perform charge transfer to the capacitor pair $(Cc1, Cc2)$. The output voltage $v_{\text{out}}(n) = v_{\text{in}}(n-1) - v_{\text{out}}(n-2)$ appears at the capacitor pair $(Cc1, Cc2)$, where $v_{\text{in}}(n-1)$ was sampled to $(C3, C4)$ at time $n-1$ and $v_{\text{out}}(n-2)$ was the voltage of $(Cb1, Cb2)$ at time $n-2$. At the same time, the charge in the capacitor pair $(Cb1, Cb2)$ is set to zero, which can be used for storing charge at time $n+1$. At time $n+1$ (shown in Fig. 2(b)), the voltage $v_{\text{out}}(n+1) = v_{\text{in}}(n) - v_{\text{out}}(n-1)$ is stored to $(Cb1, Cb2)$. At time $n+2$ (shown in Fig. 2(c)), $v_{\text{out}}(n+2) = v_{\text{in}}(n+1) - v_{\text{out}}(n)$ is stored to $(Ca1, Ca2)$. If the procedure is repeated, one can get the following expressions:

$$v_{\text{out}}(n+3) = v_{\text{in}}(n+2) - v_{\text{out}}(n+1), \quad \text{at time } n+3 \quad (1)$$

$$v_{\text{out}}(n+4) = v_{\text{in}}(n+3) - v_{\text{out}}(n+2), \quad \text{at time } n+4 \quad (2)$$

$$v_{\text{out}}(n+5) = v_{\text{in}}(n+4) - v_{\text{out}}(n+3), \quad \text{at time } n+5. \quad (3)$$

It is a complete circle from time n to time $n+5$ for performing

$$v_{\text{out}}(n+k) = v_{\text{in}}(n+k-1) - v_{\text{out}}(n+k-2) \quad (4)$$

where k is an integer and greater than two. Therefore, the z-domain transfer function of (4) is $z^{-1}/(1+z^{-2})$. This circuit performs the double-sampling function and it needs only one op-amp for a second-order system. Since the frequency of clkA1, clkB1, and clkC1 is two-thirds that of clk1 and clk2, the clock feedthrough noise will lie at $fs/3$, $2fs/3$, and fs, where fs is the sampling rate. Fortunately, noise peaks lie out of the modulator's band.

B. Fourth-Order Double-Sampling Pseudo-Two-Path Bandpass $\Delta\Sigma$ Modulator

In Fig. 3, the capacitor pairs $(Cs1, Cs2)$ and $(Cs3, Cs4)$ are used for storing the output of the bandpass modulator at clk1 and

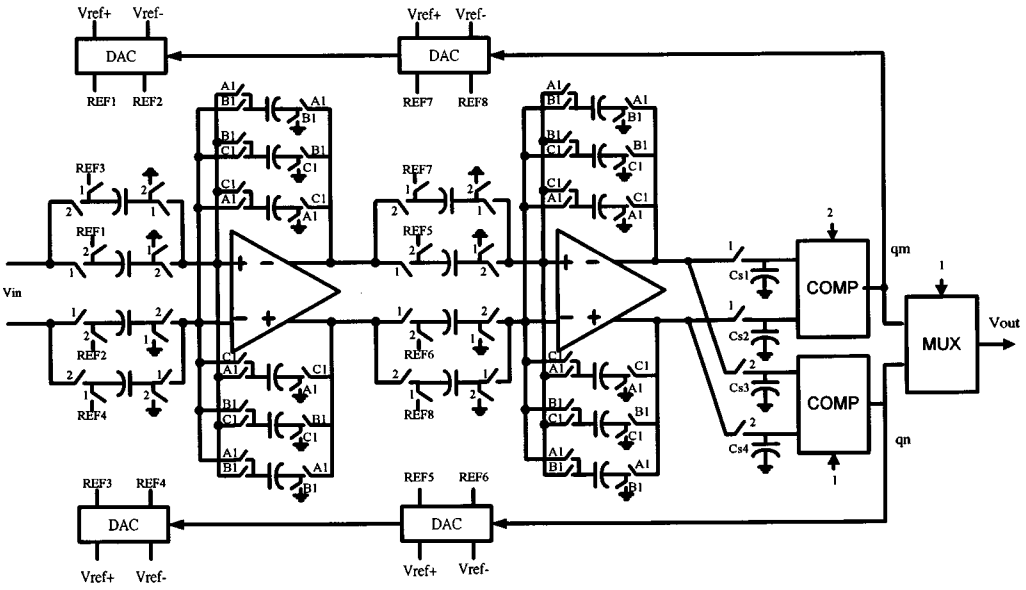


Fig. 3. The proposed fourth-order double-sampling pseudo-two-path bandpass $\Delta\Sigma$ modulator.

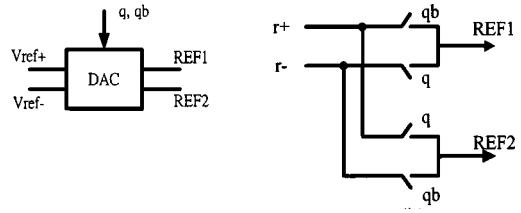


Fig. 4. The feedback DAC of Fig. 3.

clk2, respectively. Because of the double-sampling property, the outputs of the bandpass modulator are sampled both at clk1 and clk2; otherwise, the value will miss at the next clock phase. The practical implementation of the feedback digital-to-analog converter (DAC) is shown in Fig. 4. The feedback DAC signal is directly connected to the input capacitor and performs addition. Connecting $V\mathrm{ref}+$ or $V\mathrm{ref}-$ to the feedback DAC depends on whether the digital output qn (or qm) is high or low. If qn is high, $V\mathrm{ref}-$ is connected to REF1 in Fig. 4(b) at the phase of clk2. Since $V\mathrm{ref}-$ is lower than $V\mathrm{cm}$, there would be more charge stored in the sampling capacitors and the addition is accomplished. The operation is similar when qn is low.

III. Circuit Implementation

The proposed fourth-order double-sampling pseudo-two-path bandpass $\Delta\Sigma$ modulator is implemented in a 0.35-μm double-poly, double-metal CMOS process. With a 3.3-V supply voltage, the reference voltages are set at 1.3 and 2.0 V, centered at a common-mode level of 1.65 V. The folded cascode amplifier with the switched-capacitor common-mode feedback (CMFB) circuit [14], as shown in Fig. 5, is adapted in the modulator. Its simulation results are shown in Table I. A folded cascode amplifier with a class AB output stage and two on-chip resistors are used to generate the analog common voltage, 1.65 V, from the supply voltage. Regenerative feedback comparators [15] with latches are used in this design. The nonoverlapping

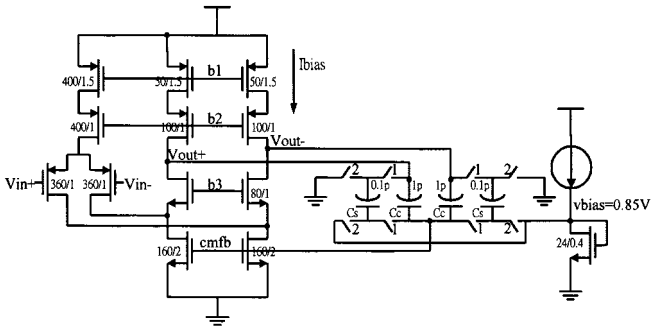


Fig. 5. The folded-cascode op-amp and the CMFB circuit.

TABLE I
Simulation Results of the Op-Amp

DC gain	56 dB
Phase margin	60
Unity-gain freq.	107 MHz@CL=1pF
Slew rate	35V/us @CL=1pF
Settling time	15 ns @error<1%
Output swing	0.2V-3.1V
VDD	3.3V
Ibias	75uA
Power	2.5mW

clock generator is used to generate the clocks, clk1 and clk2. The extra clocks, clkA1, clkB1, and clkC1 are generated by shift registers, some logic gates, and the clocks, clk1 and clk2.

IV. Experimental Results

The die photograph of the proposed bandpass $\Sigma\Delta$ modulator is shown in Fig. 6. In order to avoid noise coupling between analog and digital blocks, separated analog and digital power and ground lines are used. Off-chip bead inductors and decoupling capacitors are also used to reduce noise coupling. The

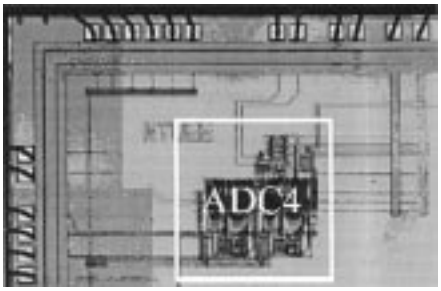
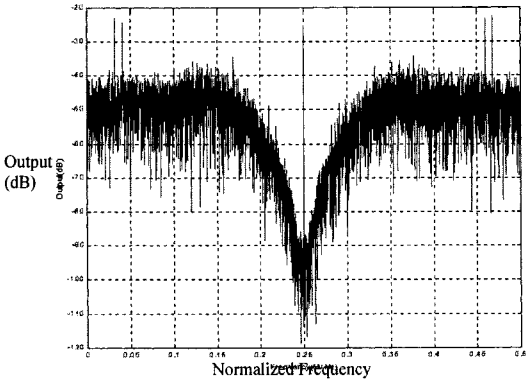
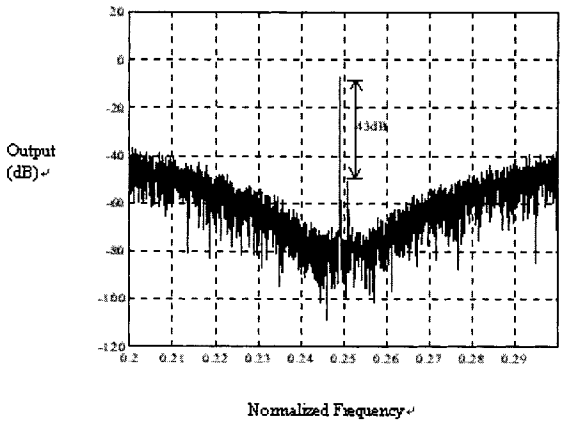


Fig. 6. Die photograph of Fig. 3.



(a)



(b)

Fig. 7 (a) The output spectrum of the proposed fourth-order bandpass modulator for $f\text{in} = 2.5$ MHz. (b) The output spectrum of the proposed fourth-order bandpass modulator for $f\text{in} = 2.49$ MHz.

sampling frequency is set to be 5 MHz. Its power consumption is 5.5 mW. The absolute capacitance of all capacitors is set to 1 pF except for the capacitor pairs $(Cs1, Cs2)$ and $(Cs3, Cs4)$, which are 0.2 pF. Fig. 7(a) shows a typical output spectrum of the proposed modulator with $f_{\text{in}} = 2.5$ MHz, and Fig. 7(b) shows the output spectrum with $f_{\text{in}} = 2.49$ MHz. Fig.7(b) indicates the suppression of the mirror signal is 43 dB. Fig. 8 shows the measured signal-to-noise ratio (SNR) versus input amplitude in 30-, 100-, and 200-kHz bandwidth at 5-MHz sampling rate. Because of double sampling, the effective sampling frequency equals 10 MHz. The peak SNR's are 62, 56, and 52 dB, and the dynamic ranges are 68, 60, and 54 dB, respectively.

The nonidealities that degrade the modulator performance may be contributed by the nonidealities of the integrator, the

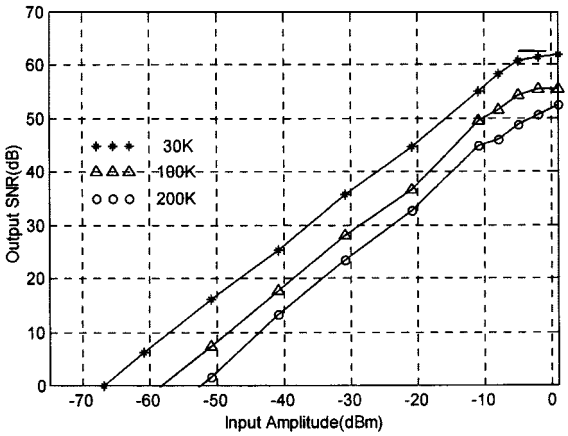


Fig. 8. The measured output SNR versus input amplitude of the proposed fourth-order bandpass modulator.

TABLE II
PEAK SNR WITH DIFFERENT INPUT FREQUENCIES IN A 30-kHz BANDWIDTH

MHz		dB
fs	fin	SNR
8	4.0	33
7	3.5	45
6	3.0	53
5	2.5	62
4	2.0	62
3	1.5	63
2.5	1.25	65

hysteresis and delay of the comparator, and clock timing jitter. The major SNR loss from the theoretical 90 dB calculated from $fs = 10$ MHz ($2\times$ 5 MHz), bandwidth $= 30$ kHz, and OSR $= 167$ is discussed as follows.

The nonidealities of the integrator are due to the large nonconstant resistance of the switches, the finite slew rate and nonlinear settling characteristics of op-amps, and the sample-and-hold noises caused by switches and op-amps [16]. Based on HSPICE simulations, by using the switches with the constant turn-on resistance (100 Ω) and the practical op-amps in Fig. 5, the peak 75-dB SNR for the proposed modulator can be achieved. To keep the turn-on resistance of the switches constant, the clock boosting techniques and the CMOS switches can be applied. The nonidealities of the integrators must also be improved to achieve the theoretical SNR. Moreover, the offset, finite gain, and bandwidth of op-amps and capacitor mismatches will also degrade the performance of the proposed modulator [16]. Table II lists the peak SNR with respect to the different input frequencies in a 30-kHz bandwidth. Moreover, the 2% variation of the duty cycle (from 50% to 48%) will degrade the peak SNR to 57 dB in a 30-kHz bandwidth at 5-MHz sampling rate for our modulator.

V. CONCLUSION

A fourth-order double-sampling pseudo-two-path bandpass $\Delta\Sigma$ modulator has been proposed and shown. The experimental results are given to demonstrate the feasibility of the proposed circuits.

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