Voltage-peak synchronous closing control for shunt capacitors

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Indexing terms: Shunt capacitor banks, Switch-closing speed, Switch-timing deviation, Voltage-zero synchronous closing, Voltage-peak synchronous closing

Abstract: The paper presents a new synchronous closing control, the voltage-peak closing method, to reduce shunt capacitor inrush currents and overvoltages. Switch timing and precharged voltages for energising a single capacitor bank, a back-to-back capacitor bank and a three-phase capacitor bank are presented. The effects of switch-closing speed and timing deviation are discussed. Two examples are illustrated to show the excellent performance.

1 Introduction

The switching of any capacitor bank produces overvoltages. Transient overvoltage will always occur during energisation, and will only occur during de-energisation if restrikes occur in the switching device [1]. The switching of shunt capacitor banks has become the most common source of transient voltage on many power systems. Certain switching operations can also present some potentially hazardous overvoltage conditions [2], not only to the capacitor bank, but to other nearby equipment such as circuit breakers and transformers.

Customer loads are becoming increasingly sensitive owing to a move to power electronics equipment for increased energy efficiency and flexibility. Utility customers are also adding power-factor correction capacitors to avoid rate penalties and further reduce energy costs. The combination of these trends is now resulting in increased customer power quality problems owing to capacitor switching events on the utility system [3]. Several methods are available for reducing energising transients [4], however, not all are practical or economical.

Both preinsertion resistors and inductors have been used by circuit-breaker manufacturers to reduce voltage and current transients during the energisation of high-voltage shunt capacitor banks. The difficulty with these devices, however, is in providing sufficient energy absorption capability without greatly increasing the complexity and cost of the circuit breaker.

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Synchronous closing is another means of reducing energising transients [5]. However, the reliability requirement of the sensing device coupled with mechanical variations in the switching device under a wide range of operating conditions have delayed developments.

This paper proposes a voltage-peak synchronous closing (VPSC) method to reduce capacitor energising transients. Since the current zero appears at the instant of voltage peak for a shunt capacitor in the steady state and the voltage changing rate is minimum at the same time, a shunt capacitor can be energised at the instant of voltage peak with a predicted capacitor voltage level to reduce or even eliminate transients. This method brings a better performance than the traditional voltage-zero synchronous closing (VZSC) in capacitor energisation [5].

2 The proposed synchronous closing method

Assume a capacitor bank is energised by a sinusoidal alternating supply voltage $v(t) = V_m \sin(\omega t + \alpha)$ where V_m is the peak value of the AC voltage. The supply frequency is varying at the radial supply frequency, ω. The inclusion of the arbitrary phase angle α permits closing of the switch at any instant in the voltage cycle. When the switch is closed, the equation expressed in terms of the current is

$$L\frac{di(t)}{dt} + \frac{1}{c}\int i(t)dt = v(t)$$

where C is the capacitance of the capacitor bank and L is the effective inductance between source and this capacitor bank. Resistance is assumed to be negligible.

The instantaneous current and voltage equation of the capacitor bank can be evaluated as follows:

$$\begin{aligned} i(t) = {} & \hat{I}_m \cos(\omega t + \alpha) \\ & + \left[I(0) - \hat{I}_m \cos\alpha\right] \cos\omega_n t \\ & + n\left[\hat{I}_m \sin\alpha - \frac{V_c(0)}{X_c}\right] \sin\omega_n t \end{aligned} \quad (1)$$

$$\begin{aligned} v_c(t) = {} & \hat{V}_m \sin(\omega t + \alpha) \\ & + \left[V_c(0) - \hat{V}_m \sin\alpha\right] \cos\omega_n t \\ & + \frac{1}{n}\left[X_c I(0) - \hat{V}_m \cos\alpha\right] \sin\omega_n t \end{aligned} \quad (2)$$

where $I(0)$ and $V_c(0)$ are the initial values of inductor current and capacitor voltage, respectively, ω_n is the

natural frequency of the switching circuit and n is the per unit natural frequency.

$$\omega_n = \frac{1}{\sqrt{LC}} \quad \text{and} \quad n = \frac{\omega_n}{\omega}$$

X_c is the impedance of the capacitor in the fundamental frequency, $\hat{I}_m$ and $\hat{V}_m$ are the peak values of the fundamental frequency components of the capacitor current and voltage, respectively.

$$\hat{I}_m = \left(\frac{n^2}{n^2-1}\right)\frac{V_m}{X_c} = \frac{\hat{V}_m}{X_c}$$

Eqns. 1 and 2 represent the time-domain response of the capacitor current and voltage in the capacitor switching circuit. The first term is the fundamental frequency component. The second and third terms represent the oscillatory components with a circuit natural frequency ω_n. The magnitude of the oscillatory components is a function of the system voltage, capacitor trapped voltage, inductor current and the switch closing time.

In general, capacitors are discharged, $V_c(0) = 0$. The worst case occurs at the time when a discharged capacitor is energised at the instant of voltage peak, which results in a transient overvoltage nearly twice the normal peak voltage.

For ideal switching, the oscillatory components of current in eqn. 1 (voltage in eqn. 2) must be zero. This can happen only when the following two conditions are simultaneously satisfied.

$$I(0) = \hat{I}_m \cos\alpha$$

$$V_c(0) = \hat{V}_m \sin\alpha$$

In the switching circuit, the initial current is zero, $I(0) = 0$. The first condition of ideal switching means that the switch must be closed at a positive or negative crest of the supply voltage sinewave (i.e. $\alpha = \pm 90°$). The second condition means that the capacitor must be charged to a specific voltage level

$$V_c(0) = \pm\hat{V}_m = \pm\left(\frac{n^2}{n^2-1}\right)V_m \qquad (3)$$

Both ideal switching conditions must be satisfied so that the oscillatory components will disappear. Then, both the capacitor current and voltage consist of only the fundamental frequency component.

The procedure to energise a shunt capacitor bank by the proposed VPSC method is:

Step 1: Calculate the prerequisite initial voltage level of the capacitor bank via eqn. 3.

Step 2: Precharge the capacitor bank to that voltage level by a DC charging circuit.

Step 3: Close the switch at the instant of voltage peak by a synchronous closing control circuit.

A practical approximation of the ideal switching is implemented by modifying the precharging voltage level. The predicted voltage level in step 1 is replaced by the level of the system peak voltage so that the voltage precharge device can be simplified. In other words, the capacitor bank is precharged to the level of the system peak voltage. Then, its switch is closed at the instant of voltage peak with the same polarity. The instantaneous capacitor current and voltage are

$$i(t) = \hat{I}_m \cos(\omega t + 90°) + n\left(\frac{\hat{V}_m - V_m}{X_c}\right)\sin\omega_n t$$

$$v_c(t) = \hat{V}_m \sin(\omega t + 90°) + (V_m - \hat{V}_m)\cos\omega_n t$$

The second term on the right-hand side represents the oscillatory component brought by the capacitor precharged voltage being not exactly equal to the predicted level from eqn. 3. The magnitude of this component is not large enough to distort its bus voltage. Although this method is not an ideal switching it is better than the VZSC method.

3 Switch timing and precharged voltages

The switch timing and precharged voltages to implement the VPSC for single-phase and three-phase capacitor energisation are presented as follows.

3.1 Single-phase capacitor energisation

Quite often the capacitor bank is divided into a number of parallel sections which can be switched independently [1]. In Fig. 1 there are two sections with their switches S_1 and S_2. The source inductance is represented by L_s, while L_b represents the inductance of the local circuit comprising the two capacitors and their bus and ground connections. Resistance is assumed to be negligible.

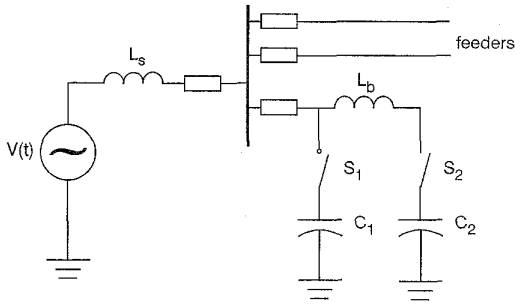

Fig. 1 *Switching capacitors on a substation bus*

3.1.1 Single bank capacitor energisation: Consider first the closing of switch S_1. This is a single-bank capacitor switching. For ideal switching, the switch must be closed at a positive or negative crest of the supply voltage sinewave (i.e. $\alpha = \pm 90°$) and the capacitor must be precharged to a predicted voltage level.

Fig. 2 shows the switch timing for the proposed closing method. The positive going zero crossing of the voltage is used as the synchronous reference. T_m is the mechanical operation time which may vary due to the operation frequency, ambient temperature and manufacturing technique. T_e is the electrical time which is adjusted to make the switch close at the expected instant of voltage peak. A capacitor can be precharged to the positive or negative voltage peak. The capacitor switch must be closed at the instant of voltage peak with the same polarity of precharged voltage.

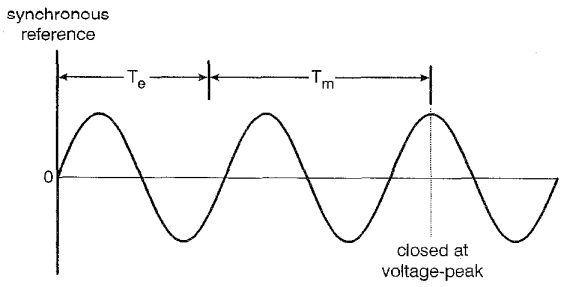

Fig. 2 *Switch timing for the proposed switching method*

3.1.2 Back-to-back capacitor energisation: Consider next the closing of switch S_2. This is a back-to-back switching operation. We suggest that the polarity of the precharged voltage of capacitor C_2 be the same as that of capacitor C_1. Thus, both switches S_1 and S_2 are closed at the same side of the positive voltage peak or negative voltage peak so that they will not be confused. The precharged voltage level of capacitor C_2 is equal to the system peak voltage, $V_{C_2}(0) = \pm V_m$.

3.2 Three-phase capacitor bank energisation

The VPSC can be applied to the energisation of a capacitor bank in a three-phase circuit. When a capacitor bank is connected between one phase and another, the capacitor bank must be precharged to a line-to-line peak voltage prior to its switch being closed at the instant of the line-to-line voltage peak with the same polarity of precharged voltage.

3.2.1 Grounded Y connection: In a grounded three-phase circuit, the energisation of capacitor banks connected in a grounded Y connection can be considered with three single-phase circuits independently.

Fig. 3 shows the switch timing and precharged voltages for a grounded Y connected capacitor bank. The next positive going zero crossing of the phase A voltage is used as the synchronous reference. In order to close the three switches as soon as possible, the time differences $t_3 - t_2$ and $t_2 - t_1$ should be equal to $\pi/(3\ \omega)$. The closing time t_1 of switch (SW-1) is chosen at the instant of phase A-to-ground voltage peak. Therefore the precharged voltage level of the capacitor C_1 is decided as $V_{C_1}(0) = V_m$. Similarly, the precharged voltage levels of C_2 and C_3 are decided by the relative closing time t_2 and t_3 as $V_{C_2}(0) = -V_m$ and $V_{C_3}(0) = V_m$

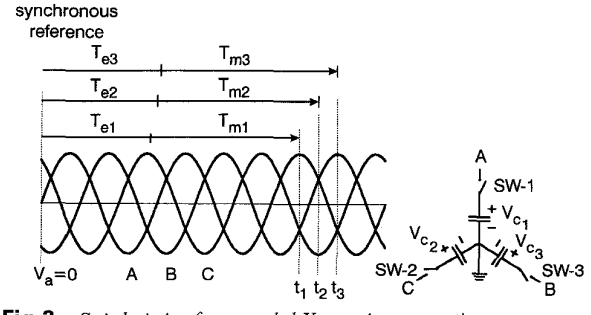

Fig. 3 *Switch timing for grounded Y capacitor connection*
$V_{C_1}(0) = V_m$; $V_{C_2}(0) = -V_m$; $V_{C_3}(0) = V_m$

3.2.2 Ungrounded Y connection: The proposed closing method for energising the three capacitors connected in an ungrounded Y connection in a three-phase circuit is shown in Fig. 4. The method comprises two steps:

Step 1: Choose any two capacitors and energise by the VPSC method with the line-to-line voltage peak across these capacitors.

Step 2: The other capacitor is energised by the VPSC method with a phase-to-neutral voltage.

The switch timing and precharged voltage of the capacitor bank connected in an ungrounded Y connection is shown in Fig. 4. The next positive going zero crossing of the line-to-line voltage between phase A and B is used as the synchronous reference. In order to close the three switches as soon as possible, a time interval of $\pi/(2\ \omega)$ between t_1 and t_2 is necessary. SW-3 can be closed first since it cannot become a closed-loop circuit, then SW-1 is closed at t_1, the instant of voltage peak of phase A-to-B. Therefore the precharged voltage levels of the two capacitors C_1 and C_3 are $V_{C_1}(0) = \sqrt{3}V_m/2$, $V_{C_3}(0) = -\sqrt{3}V_m/2$. The other closing time t_2 for SW-2 is chosen at the instant of voltage peak of phase C-to-neutral and the precharged voltage level of capacitor C_2 is $V_{C_2}(0) = -1.5V_m$.

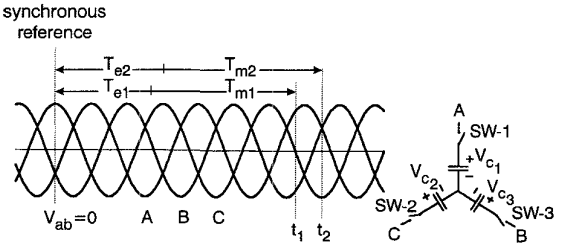

Fig. 4 *Switch timing for ungrounded Y capacitor connection*
$V_{C_1}(0) = 0.866V_m$; $V_{C_2}(0) = -1.500V_m$; $V_{C_3}(0) = -0.866V_m$

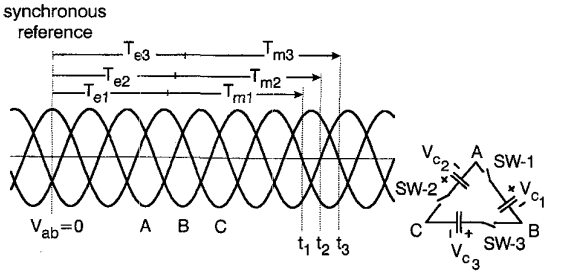

Fig. 5 *Switch timing for delta capacitor connection*
$V_{C_1}(0) = 1.732V_m$; $V_{C_2}(0) = -1.732V_m$; $V_{C_3}(0) = 1.732V_m$

3.2.3 Delta connection: Fig. 5 shows three capacitors connected in a delta connection in a three-phase circuit which can be energised, respectively, by the VPSC method with line-to-line voltages.

The switch timing of capacitor banks connected in a delta connection is shown in Fig. 5. The next positive going zero crossing of phase A-to-B voltage is used as the synchronous reference. In order to close the three switches as soon as possible, the time differences $t_2 - t_1$ and $t_3 - t_2$ should be equal to $\pi/(3\ \omega)$. The closing time t_1 of SW-1 is chosen at the instant of phase A-to-B voltage peak. Therefore the precharged voltage level of the capacitor C_1 is decided as $V_{C_1}(0) = \sqrt{3}V_m$. Similarly, the precharged voltage levels of the capacitors C_2 and C_3 are decided as $V_{C_2}(0) = -\sqrt{3}V_m$ and $V_{C_3}(0) = \sqrt{3}V_m$.

4 Advantages

The advantages of VPSC can be illustrated in the switch closing speed and timing deviation by the comparison of VPSC with VZSC.

4.1 Closing speed

A switch's contact velocity and dielectric characteristics are combined to form dV/dt, a rate of change of the gap dielectric withstand voltage. It must always be greater in magnitude than the rate of voltage change for VZSC [5]. However, this constraint is not so strict for VPSC.

The principle requirement of the gap dielectric characteristics at closing is shown in Fig. 6, where the absolute value of a sinusoidal voltage is plotted for VZSC and VPSC. Lines (i) and (ii) illustrate the critical

rate of change of the gap dielectric withstand voltage for making a VZSC and a VPSC occur, respectively. As the contact closing speed increases, the rate of change of the gap dielectric withstand voltage also increases. Below a critical value, the line always crosses the AC voltage envelope, but it does not cross the expected voltage point. Above this critical value, a condition for making the synchronous closing occurs.

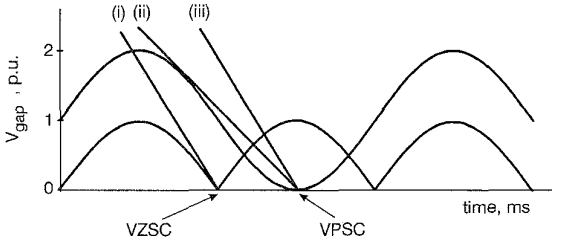

Fig.6 *Condition with contact making for VZSC and VPSC*

The switch used in the VZSC method can be applied to the VPSC method, shown as line (iii). It is apparent that the slope of line (ii) is less steep than that of line (iii) so that the switch contact at voltage peak is easier than voltage zero. A vacuum switch is an excellent switch for synchronous voltage-zero closing [5]. Therefore it is certain that the vacuum switch can be applied to the proposed VPSC method.

4.2 Timing deviation

Since switches and circuit breakers are mechanical devices with complex mechanisms, the speed of operation is not completely consistent. A typical deviation of ±0.2ms is measured [5]. This deviation is due to the small change with temperature and the inherent mechanical inconsistency of the switch.

In order to analyse the effect of the deviation time on the voltage-zero closing and voltage-peak closing, the phase angle α in the switching capacitor current eqn. 1 is replaced by the phase angle of the expected closing point with a voltage-phase shift. The voltage-phase shift ($\Delta\alpha$) is proportional to the deviation time. Thus, the phase angle $\alpha = 0° + \Delta\alpha$ represents when the switch is closed at voltage zero with deviation time and the phase angle $\alpha = 90° + \Delta\alpha$ represents when the switch is closed at voltage peak with deviation time.

Therefore for VZSC, the current equation will be

$$i(t) = \hat{I}_m \cos(\omega t + \Delta\alpha) - \hat{I}_m \cos\Delta\alpha \cos\omega_n t + n\hat{I}_m \sin\Delta\alpha \sin\omega_n t \quad (4)$$

and for VPSC, the current equation will be

$$i(t) = \hat{I}_m \cos(\omega t + 90° + \Delta\alpha) - \hat{I}_m \cos(90° + \Delta\alpha)\cos\omega_n t + n\hat{I}_m[\sin(90° + \Delta\alpha) - 1]\sin\omega_n t \quad (5)$$

The last terms of eqns. 4 and 5 are dominantly the major quantities of the oscillatory component of the inrush current. Thus, we can obtain

$$|\sin\Delta\alpha| > |\cos\Delta\alpha - 1| \quad \text{for } 0 < \Delta\alpha < 90° \quad (6)$$

The inequality indicates that the maximum peak value of the current in eqn. 4 is higher than that in eqn. 5. This results in the maximum peak value of the current of the capacitor bank energised by VPSC being less than that by VZSC when the switch is closed with deviation time.

The magnitudes of the high frequency oscillatory current and voltage are amplified owing to the deviation of closing time. It is more significant when the switch is closed by a VZSC method than by a VPSC method for $\Delta\alpha < 90°$.

The transient magnitude of the oscillatory current versus closing time accuracy is shown for a VZSC method and a VPSC method in Fig. 7. The VPSC method has the longest allowable time deviation for a given inrush current limit. For 3p.u. oscillatory current-limit performance, the maximum time deviation for a VPSC method is 2.3ms while for a VZSC method it is 0.9ms. Even although the switch is closed exactly at voltage zero, it still brings a 1.0p.u. high frequency oscillatory component. With the limitation of a 1.0p.u. oscillatory component, the maximum time deviation for the VPSC method is 1.2ms.

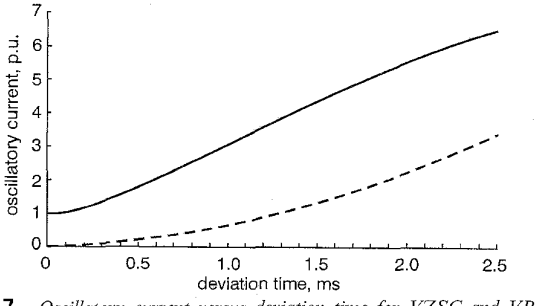

Fig.7 *Oscillatory current versus deviation time for VZSC and VPSC methods*
n = 8.0p.u.
——— voltage-zero closing
– – – – voltage-peak closing

It is more desirable for the switch to be closed late rather than early. In practice, the energisation time of 0.3ms late is adapted by the synchronous voltage-zero closing method [5].

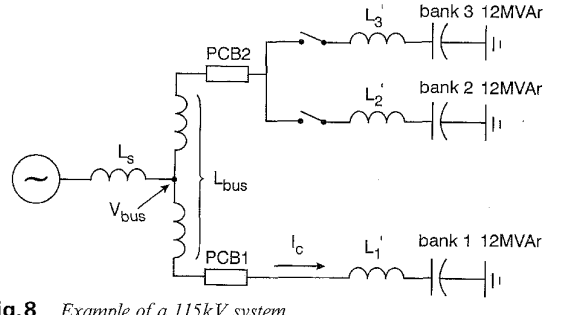

Fig.8 *Example of a 115kV system*
L_s = 10mH; L_{bus} = 37.6μH; L_1^1 = 20.0μH; L_2^1 = 27.1μH; L_3^1 = 27.1μH

Table 1: Capacitor energising transients in three cases

Condition	Case 1		Case 2		Case 3	
Closing method	I_c (pu)	V_{bus} (pu)	I_c (pu)	V_{bus} (pu)	I_c (pu)	V_{bus} (pu)
Worst situation	17.03	1.98	132.04	1.55	166.70	1.45
Series inductor	17.62	1.94	51.75	1.91	56.53	1.62
VZSC method	1.99	1.05	2.18	1.04	2.21	1.04
VPSC method	1.00	1.00	1.05	1.01	1.04	1.04

5 Examples

5.1 Example 1: IEEE example of a 115kV system

Fig. 8 shows an IEEE example of a 115kV system [6]. The capacitor banks shown have a nominal rating of

12MVAr and the nominal current per bank is 60A. This system is simulated by the Electromagnetic Transients Program (EMTP) [7]. Three control strategies are adapted to reduce the capacitor energising transients shown in Table 1. The bus voltage in per unit is based on its system peak voltage and the maximum current in per unit is based on the peak value of the fundamental frequency current of the capacitor bank 1. For illustration, the following three cases are assumed:

Case 1: Energisation of capacitor bank 1 with bank 2 and 3 not energised (isolated switching). The worst situation means that capacitor bank 1 is discharged and is energised at an instant of voltage peak. This involves up to a 2p.u. overvoltage and moderate inrush current. Addition of an inductance (0.6mH) [6] is supposed to limit the inrush current but the result does not seem obvious. A large series inductor will obviously limit the inrush, but it will also reduce the capacity of the capacitor bank and may induce a serious resonance. A synchronous voltage-zero closing method can reduce the energising transients efficiently, but it still brings a 2p.u. inrush current and some overvoltage. The proposed closing method in this paper can make a single capacitor bank energised in a transient-free switching.

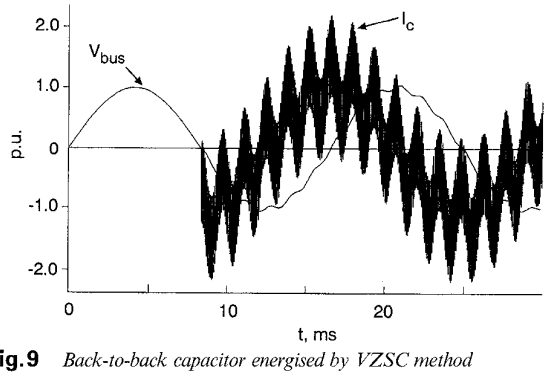

Fig. 9 *Back-to-back capacitor energised by VZSC method*

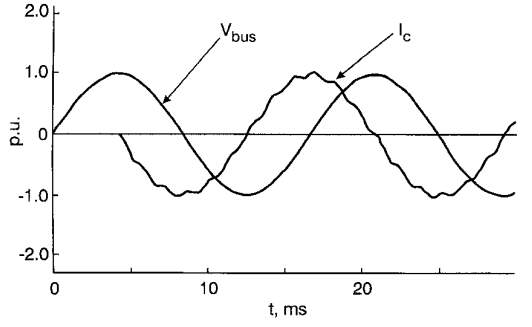

Fig. 10 *Back-to-back capacitor energised by VPSC method*

Case 2: Energisation of capacitor bank 1 with bank 2 energised on the bus (back-to-back switching against an equal-size bank). Since the inductance between capacitor bank 1 and bank 2 is very small, in the worst situation, the back-to-back case involves moderate overvoltage and severe inrush current. Addition of an inductance (0.6mH) will limit the back-to-back inrush current to 52p.u., but it cannot reduce the transient overvoltage which swings between the capacitor bank and source inductance. A synchronous voltage zero closing can reduce the inrush current to 2p.u., but it brings some transient overvoltage, as shown in Fig. 9. However, the proposed closing method can energise the capacitor bank within minimum transients and operate as soon as possible to reach a steady state, as shown in Fig. 10.

Case 3: Energisation of capacitor bank 1 with bank 2 and 3 energised on the bus. This is also a back-to-back capacitor bank energisation. The simulation results are similar to case 2. The proposed closing method shows the best result for capacitor energisation, which has a much better performance than the traditional voltage-zero synchronous closing method.

In order to analyse the effect of switch timing deviation on capacitor energisation, two deviation times (0.3ms late and 1.0ms late) are assumed to be applied to the voltage-zero closing method and the proposed closing method, respectively.

Table 2 shows the maximum inrush current and bus voltage when capacitor bank 1 is energised. With the same deviation time, the VZSC method will bring a larger inrush current and overvoltage than the proposed closing method.

Table 2: Synchronous closing with timing deviations

Condition	Case 1		Case 2		Case 3	
Closing method	I_c (pu)	V_{bus} (pu)	I_c (pu)	V_{bus} (pu)	I_c (pu)	V_{bus} (pu)
VZSC with 0.3ms late	3.20	1.13	15.66	1.08	19.13	1.07
VPSC with 0.3ms late	1.12	1.00	1.50	1.01	1.14	1.02
VZSC with 1.0ms late	7.33	1.37	46.85	1.20	58.10	1.16
VPSC with 1.0ms late	2.25	1.08	9.55	1.04	11.14	1.03

The proposed VPSC method can effectively reduce the inrush current and overvoltage for the energisation of a single capacitor bank and a back-to-back capacitor bank. Note that the VPSC with 1.0ms deviation time is even better than the VZSC with 0.3ms deviation time.

5.2 Example 2: voltage magnification

Capacitor switching transients can be magnified in certain installations. One that appears to be most commonly associated with this phenomenon occurs when capacitors are switched on from a bus switch supplying a step-down transformer that has shunt capacitors installed on the secondary side [3]. An example of an installation that may produce voltage-magnification effects is shown in Fig. 11. Energising the primary loop will excite the natural modes of oscillation in both the primary and secondary loops.

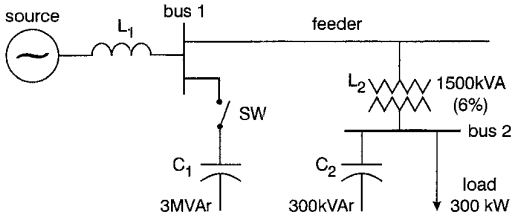

Fig. 11 *Voltage-magnification example*

Whenever capacitors are installed at multiple voltage levels, the equipment at the lower voltage level may be subjected to severe overvoltages even when the tuning is not exact ($L_1C_1 \cong L_2C_2$).

The circuit in Fig. 11 was developed to analyse different energising strategies that can affect this magnifi-

cation [3]. The system source at bus 1 is equal to 200MVA. A 3MVAr shunt capacitor bank is on the substation bus 1. A 1500kVA transformer (6% impedance) is connected to the customer at bus 2 and a 300kVAr power factor correction capacitor and a 300kW resistive load are on the customer bus 2.

Table 3 shows the maximum voltage in per unit at bus 1 and bus 2 when capacitor C_1 is energised by 7 different closing methods. In the worst situation, the discharged capacitor C_1 was energised at an instant of voltage peak. It brings a 1.89p.u. overvoltage at bus 1 and a 2.54p.u. overvoltage at bus 2. The VZSC method can reduce the transient overvoltage to 1.03p.u. at bus 1 but it still brings a 1.27p.u. overvoltage at bus 2. With a deviation time, the voltage magnification at bus 2 cannot be reduced effectively by the VZSC method. With a 1.0ms deviation time, the VZSC method brings a 1.81p.u. overvoltage at bus 2. However, the proposed VPSC method has a very good performance for reducing the capacitor energising transients. Even with a 1.0 ms deviation time, the VPSC method still can limit the transient overvoltage at bus 2 below 1.1p.u.

Table 3: Voltage magnification produced by closing methods

Closing method	V_{bus1} (pu)	V_{bus2} (pu)
Worst situation	1.89	2.54
VZSC method	1.03	1.27
VZSC with 0.3ms late	1.05	1.37
VZSC with 1.0ms late	1.21	1.81
VPSC method	1.02	1.03
VPSC with 0.3ms late	1.02	1.04
VPSC with 1.0ms late	1.04	1.09

6 Conclusions

The voltage-peak synchronous closing method can effectively reduce the energising transients for a single capacitor bank and a back-to-back capacitor bank. This method is superior to the voltage zero synchronous closing method in switch-closing speed and timing deviations.

The proposed method is also applied to the energisation of various loads, such as the reduction of transformer inrush current. The reduction of energising transients reduces the stresses on the switching device, extends the equipment life and improves the network power quality.

A patent on this synchronous closing control is pending.

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