Dual Hysteresis Loops for a High-Performance Four-Switch Boost Rectifier

*** Yu-Kang Lo, Member, IEEE, ** Huang-Jen Chiu and * Sheng-Yuan Ou**

* Dept. of Electronic Engineering
National Taiwan Univ. of Science and Technology
No. 43, Sec. 4, Keelung Rd.
Dept. of Electronic Engineering, NTUST
10607, Taipei, Taiwan, R.O.C.
yklo@et.ntust.edu.tw

** Dept. of Electronic Engineering
I-Shou University
No. 1, Sec.1, Hsueh-Cheng Rd.
Dept. of Electronic Engineering, ISU
Ta-Hsu, Kaohsiung, Taiwan, R.O.C.
D8602017@mail.ntust.edu.tw

Abstract

A new current controller adopting dual hysteresis loops for a high-performance four-switch boost rectifier is proposed in this paper. The four-switch boost rectifier is operated under the so-called phase-adjusted unipolar PWM strategy. The inner loop confines the current ripple within a preset band. The outer loop determines the instants to change the switching patterns. Experimental results are satisfactory.

1. Introduction

Pulse-width modulated (PWM) ac/dc boost rectifiers have been presented to replace the diode rectifiers in the recent years for their high input power factor values. Many topologies of the PWM boost rectifiers have been studied in the literature [1, 2]. Among these, a four-switch boost rectifier as shown in Fig. 1 claims to produce the input current of a better quality under the phase-adjusted unipolar PWM scheme [1]. Such scheme chooses between two sets of switching patterns according to the sign of the time-averaged values of v_μ. However, it is difficult and impractical to extract the fundamental component $v_{\mu 1}$ from the real-time pulse-like waveform of v_μ. In this paper, a new current controller with dual hysteresis loops is proposed to check the sign of $v_{\mu 1}$. The inner loop with a smaller hysteresis band forces the input current to follow a sinusoidal command. The outer loop with a larger band detects the instants at which the sign of $v_{\mu 1}$ changes. In the following sections, the circuit descriptions and design of the controller will be discussed in detail. Experimental results on a prototype system are given to show the feasibility of the proposed scheme.

2. Circuit Descriptions

Consider the four-switch boost rectifier shown in Fig. 1. It is known that applying the phase-adjusted PWM scheme will result in an undistorted input current with lower switching frequencies or, equivalently, with smaller harmonic contents [1, 2]. Table I lists the possible switching states of the discussed rectifier. The phase-adjusted PWM requires that two sets of switching patterns are alternatively utilized in one complete cycle. The input current i_s will go beyond the hysteresis band after some instants if the switching pattern is not changed. These instants are called the transition angles [3]. For example, in the positive half cycle, v_μ is controlled to fluctuate between −E and 0 at first. When v_μ equals −E, i_s tends to approach to the upper band, and vice versa. After the transition angle θ_T, however, i_s continues to grow beyond the upper band even when v_μ equals 0. For i_s to remain in the hysteresis band, the switching patterns must be changed so that v_μ fluctuates between 0 and +E. Then when v_μ equals +E, i_s tends to approach to the lower band, and vice versa. The same situation occurs in the negative cycle, where the switching patterns are changed at $(\theta_T + \pi)$. θ_T can be determined by equating the changing rate of i_s when v_μ is 0 to the changing rate of the current command i_{com}.

$$\left.\frac{di_s}{dt}\right|_{v_\mu = 0} = \frac{v_s}{L} = \frac{V_s \sin\theta_T}{L} = \left.\frac{di_{com}}{dt}\right|_{\theta = \theta_T} = \omega I_{com}\cdot\cos\theta_T, \tag{1}$$

where L is the input inductance, ω is the fundamental radian frequency, I_{com} is the amplitude of the current command, and V_s is the amplitude of v_s. Thus,

$$\theta_T = \tan^{-1}\left(\frac{\omega L I_{com}}{V_s}\right). \tag{2}$$

To determine θ_T correctly is crucial for the discussed rectifier to exhibit a better performance. However, there are practical difficulties to calculate θ_T directly from (2). Nevertheless, we may take advantage of the

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characteristics of the phase-adjusted PWM scheme to detect θ_T.

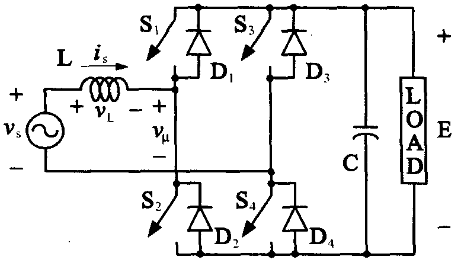


Fig. 1 The four-switch boost rectifier.

3. The Proposed Hysteresis Contoller

From the discussions above, we can conclude that the transition angles can be detected by a second hysteresis loop with a larger band. The proposed hysteresis controller and its transfer characteristic is depicted in Fig. 2, with R_2' larger than R_2 . Δi_s is the difference between i_s and i_{com}. A and B are the TTL-compatible outputs of the two comparators. The inner loop forces i_s to follow i_{com}. When Δi_s exceeds the inner hysteresis loop, the outer loop will be touched and A will change its state. Then the suitable switching patterns are chosen to pull Δi_s back into the inner hysteresis loop. The detection of θ_T will be more accurate if the hysteresis bands of these two loops are closer. However, the effects of the signal noises should be taken into account when designing the widths of the hysteresis bands. According to Table I and the transfer characteristics of the proposed controller, the gating signals for the active switches can be arranged. Let C represent the binary variable for the sign of v_s . For instance, in the positive half cycle (C is high), S_2 is turned on before θ_T (A is high) or after θ_T (A is low) and when the lower bound of the inner hysteresis loop is touched (B is high), and S3 is turned on only before θ_T (A is high) and when lower bound of the inner hysteresis loop is touched (B is high). Thus,

$$S_2 = (A + \bar{A}B)\cdot C = (A + B)\cdot C, \qquad (3)$$

$$S_3 = A\cdot B\cdot C, \qquad (4)$$

The gating signals for S_1 and S_4 can be produced in the same way.

$$S_1 = \bar{A}\cdot\bar{B}\cdot\bar{C}, \qquad (5)$$

$$S_4 = (\bar{A} + \bar{B})\cdot\bar{C}. \qquad (6)$$

These signals can be produced by simple TTL-based circuits. It should be noted that the switching numbers of S_1 and S_3 are fewer. Also, S_1 and S_4 are always turned off in the positive cycle, and S_2 and S_3 are always turned off in the negative cycle. Thus the dead times are needed to be inserted only in signals C and $\bar{C}$, which change their states twice in a complete period.

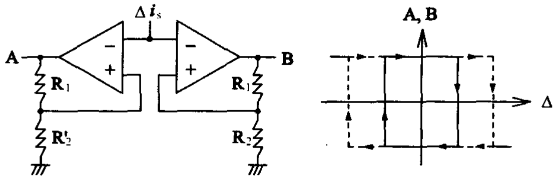


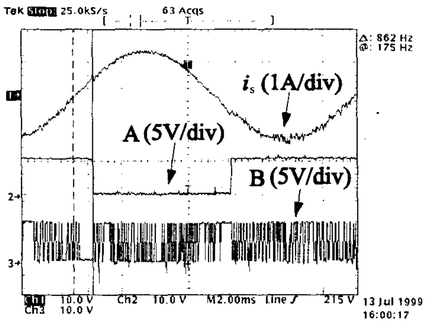
Fig. 2 The proposed hysteresis controller and its transfer characteristic.

4. Experimental Results

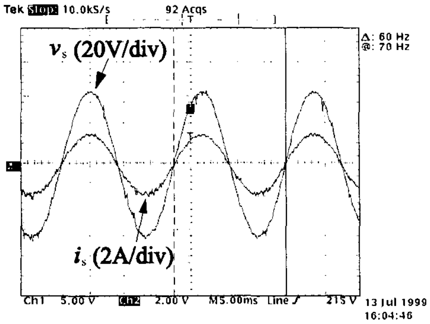
Experiments on a prototype system are performed with the following circuit parameters.

$V_s = 30\sqrt{2}$ V, $I_s = \sqrt{2}$ A, E = 70 V, $\omega = 60\times2\pi$ rad/sec, L = 4 mH, C = 470 μF, inner band = ±15 mA, outer band = ±45 mA, and $\theta_T \cong 3^\circ$.

Here the difference between the inner and outer bands is set larger than required to clearly inspect the outputs of the two comparators. Fig. 3(a) shows the waveforms of i_s, A and B. In the positive cycle, it can be seen that after θ_T, i_s continues to increase even when B is low. When the upper band of the second comparator is exceeded (A is low), the switching patterns are changed to force i_s to remain in the inner loop again. Fig. 3(b) shows the waveforms of v_s and i_s. The input power factor is nearly unity.



(a)



(b)

Fig. 3 (a) The waveforms of i_s, A and B. (b) The waveforms of v_s and i_s.

Table I. Switching States of the four-switch boost rectifier.

	v_μ	v_L	conducting devices
positive cycle	+E	$v_s - E$	D_1, D_4
	0	v_s	S_2, D_4 or D_1, S_3
	−E	$v_s + E$	S_2, S_3
negative cycle	+E	$v_s - E$	S_1, S_4
	0	v_s	D_2, S_4 or S_1, D_3
	−E	$v_s + E$	D_2, D_3

5. Conclusions

This paper has presented a hysteresis current controller with two loops for a four-switch boost rectifier to operate under the phase-adjusted PWM scheme. The inner loop confines the input current ripple within a smaller hysteresis band. The outer loop determines the instants to change the switching patterns. Experimental results has been recorded to verify the effectiveness of the proposed controller. The discussed system is specially suitable and cost-worthy for high-power applications.

References

[1] J. C. Salmon, "Circuit topologies for single-phase voltage-doubler boost rectifiers," IEEE Trans. Power Electron., vol. 8, no. 4, pp. 521-529, Oct. 1993.

[2] J. C. Salmon, "Techniques for minimizing the input current distortion of current-controlled single-phase boost rectifiers," IEEE Trans. Power Electron., vol. 8, no. 4, pp. 509-520, Oct. 1993.

[3] Y,-K. Lo and N.-C. Lai, "On evaluating the input current distortion with current slopes for single-phase switch-mode rectifiers," in Proc. IEEE ISIE'98, 1998, pp. 77-80.