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A FABRICATION PROCESS VARIATION BASED APPROACH TO EVALUATE DESIGN-FOR-TEST TECHNIQUES

製程偏移對可測試性設計技術效能影響的評估

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摘　要

類比／混合信號系統的可測試性設計技術由於缺乏有效的評估方法，接受度一直不高。在這篇論文中，我們提出一個評估可測試性設計效能的技術。該方法考慮無可避免的製程偏移對待測電路與可測試性電路性能的影響，因此比過去的方法更爲實際，也更能反映出實際生產線上的製程缺陷。我們以一個內含 Ramp Generator 可測試性設計的 Flash ADC 爲例，分析的結果發現原來的可測試性設計並不能偵測到動態缺陷，必須重新設計 Ramp Generator。

關鍵詞：可測試性設計、混合信號電路測試、類比／數位轉換器、積分非線性錯誤、微分非線性錯誤。

Abstract

One of the hurdles that prevent the wide acceptance of analog/mixed-signal design-for-test techniques is lack of a realistic and practical evaluation methodology. In this paper, a method to assess the quality of a design-for-test design (together with the associated test set) is proposed. Based on fabrication process variation information, our design-for-test evaluation criterion considers the inevitable adverse effects of fabrication process imperfection on both the functional and design-for-test circuits, and therefore will correlate better with the manufacturing test quality than past proposals. To validate our method, a flash ADC with a built-in ramp generator is used as an ex-ample. The proposed approach shows that the original design-for-test design fails capturing dynamic defects, and a redesign of the ramp generator or the test set is necessary to enhance the manufacturing test quality.

Keywords: design-for-test, mixed-signal testing, analog-to-digital converter, INL, DNL.

1. INTRODUCTION

Even though structural fault test generation techniques have been commercialized and widely adopted in digital designs, functional testing is still the main stream for analog/mixed-signal (AMS) circuits. The reliance on functional testing leads to several challenges in the production testing environment:

1. Transportation of analog test data between the circuit under test (CUT) and the automatic test equipment (ATE) suffers environmental noise and performance variation/degradation of pin-card electronics and probes.
2. AMS functional testing is a time-consuming process. A considerable portion of test time is spent on signal settling and switching, which doesn't scale down with better process technology.
3. In general, the captured CUT responses cannot be interpreted directly. Various signal processing techniques, *e.g.*, FFT, RMS, *etc.*, are applied to extract the desired circuit performance.
4. The growing circuit complexity and functionality of

modern AMS ICs continues pushing for more capable, high-performance, and as a result more expensive test instrument.

In addition to the above challenges, the trend of integrating AMS and digital circuits onto the same die incurs new issues. First, access to the AMS circuits may not always be possible. Furthermore, the effect of noisy digital circuit operations on sensitive AMS circuits must be considered during manufacturing testing to ensure the AMS functionality correct-ness.

As reported in ITRS 2004 update [1], DfT is one promising solution to the above problems, and it is projected that BIST (built-in self-test) for analog cores be in full use by 2006. The basic idea of DfT is to place dedicated test circuits on the same die as the CUT to facilitate manufacturing testing. The added test circuits may range from simple wires and switches for CUT reconfiguration to full-blown on-chip signal generator and response analyzer. Com-pared to traditional ATE-centric AMS testing approaches, AMS DfT possesses the following advantages:

1. The DfT circuits can be made close to the AMS CUT; therefore, accessing embedded signals be-comes much easier and not limited by the I/O pin bandwidth.
2. The DfT and functional circuits are manufactured with the same process technology, which keeps them at the same performance level.
3. DfT circuits can pre-process and transfer the sensitive input test stimuli and/or CUT responses to more noise immune or simpler forms, *e.g.*, digital. This way, the efforts of test data transportation and the cost of DfT ATE can be greatly reduced.

Nevertheless, the main concern of DfT is the incurred area overhead, performance degradation, and the achievable manufacturing test quality.

Since the ultimate goal of any DfT technique is to identify the defective ICs, it is nature to evaluate the DfT quality in terms of its ability to correctly tell the good ICs from bad ones. Unlike digital circuits for which the DfT and test set quality is determined by the achievable fault coverage with respect to the specified fault models, there is still no widely adopted criteria to evaluate AMS DfT and test set quality. As a result, it is not uncommon that in some reported DfT techniques [2~6] no report of the DfT efficiency is given. In [7~14] the injected faults are (1) single or multiple device (usually R or C) parameter variations at a set of discrete values, or (2) short and open faults, with all other circuit parameters fixed at nominal values. Apparently, the simple fault models cannot reflect the realistic process defects in a fabrication line. The fault models are extended in [15] so that the parametric variations of the fault-free parameters are considered. In [16], global and local process variations are utilized to optimize a given test set; however, it is assumed that parameter variations are independent random variables.

In this paper, we propose a method to evaluate the quality of a DfT technique. Utilizing fabrication process variation information, our method can better reflect the manufacturing process perturbations than previous works. Furthermore, the evaluation criteria is based on both the yield and defect coverage and thus is a better indication of the DfT's ability to differentiate good ICs from bad ones. The DfT evaluation results can serve as the guidance to improve the DfT design and/or the test set. In its current implementation, the proposed method is computation intensive due to the analog circuit simulation complexity, and can handle only parametric process variations.

This paper is organized as follows. In Section2, we will briefly discuss the yield analysis techniques. In Section 3, the proposed approach is depicted. Simulation results on a flash ADC is shown in Section 4, and we conclude this paper in Section 5.

2 PRELIMINARIES

In this section, we will first discuss the analog fault models utilized in previous works. Then, we will give some background on fabrication process variations and IC yield analysis.

2.1 Analog Fault Modeling

For analog/mixed-signal circuits, the commonly used fault models are the catastrophic and parametric faults. Catastrophic faults are open and short circuits that modify the circuit topology. They are usually caused by pin holes or unwanted particles that fall on the IC surface during the manufacturing process. Depending on the location and the type of particle, undesired short or open circuits occur. To obtain the catastrophic fault list, inductive fault analysis (IFA) [17,18] can be employed to identify the list of potential fault sites, and estimate their corresponding probabilities of occurrence. Theoretically, the number of catastrophic faults is infinite because the number of possible fault sites is unlimited, and associated with each fault site, the open/short resistor may posses any value within a reasonable range, *e.g.*, from a few ohms to a few mega ohms. In practice, one usually neglects the fault sites of which the possibilities are below a given threshold, and selects only a few representative discrete open/short resistor values, in either log or linear scale, to reduce the size of the fault list.

Parametric faults, on the other hand, are caused by

fabrication process fluctuations. Due to the process variation, the circuit parameters of the manufactured circuit instances deviate from the nominal values and form certain statistical distributions. In most of the past works, a manufactured instance with parametric deviations is considered as faulty if it fails any of the functional specification constraints functional testing and/or some of its circuit parameter values are outside the acceptable ranges. Note that the former is based on functional testing and the latter on structural testing.

2.2 Yield Analysis

During the IC fabrication process, the physical circuits components, *i.e.*, resistors, capacitors, transistors, inevitably deviate from nominal values or de-sign intentions due to a variety of deterministic and random effects. As a result, the performance of the manufactured circuit instances will deviate from the ideal performance, and a manufactured instance will be rejected if its response falls beyond the tolerance limits of the ideal response. To achieve higher yield, the probability that the actual response falling within the tolerance limits of the ideal response should be maximized-called yield enhancement or optimization. Yield enhancement usually involves two tasks, yield estimation (analysis) and yield improvement.

Yield analysis generally consists of two steps, process simulation and circuit simulation, and a number of methods have been proposed [19~23] Given information on fabrication step parameters, such as times and temperatures of different steps, process simulators produces *sets* of device parameters which approximate those parameters produced by the actual process. As for the circuit simulation step, the focus is to reduce the computation efforts required to obtain the performance distribution with respect to the device parameter distribution.

2.3 Fabrication Process Variations

The circuit parameter variations can be divided into two categories, systematic offset and mismatch. Systematic offset is caused by asymmetry in circuit configuration, bias condition and layout, and in general, can be avoided by careful circuit design and fabrication process control. Mismatch, on the other hand, is the process that causes time-independent random variations of physical parameters of identically designed devices. Mismatch is an inherent feature of the VLSI technology. Mismatch cannot be omitted, but it can be understood, and its influence on the performance of ICs can be minimized. The impact of mismatch of MOS transistors becomes more and more important as the dimensions of the devices are reduced and the available signal swing decreases.

In general, there are two kinds of device mismatch: local and global variations. Local variations originates from short distance effects, and is usually a normal distribution with zero mean. The contributing events to local variations have a correlation distance much smaller than the device dimensions. Global variations, on the other hand, is related to the different gradients across the wafer, *e.g.*, oxide thickness. Global variations originates from wafer fabrication process and can be modelled as an additional stochastic process with a long correlation distance. Among the mismatch modeling methods [24~26], we adopt the model proposed in [25]. The variation of parameter ΔP is expressed as

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2 \quad (1)$$

where A_P is the area proportionality constant for variation of parameter P, W, and L are the width and length of rectangular devices, S_P is the constant of variation of parameter P with distance, and D is the spacing distance.

3 THE PROPOSED TECHNIQUE

In this section, we will first describe the DfT evaluation criteria. Then, we will depict the evaluation flow and tool implementation details.

3.1 DfT Evaluation Criteria

The proposed DfT evaluation method use the circuit parameter perturbations (caused by fabrication process variations) as the underlying fault model so that the reported DfT quality can better correlate with the manufacturing test quality.

Let $\mathcal{N}$ be an AMS circuit with DfT feature. $\mathcal{N}_F$ and $\mathcal{N}_T$ denote the functional and DfT part of $\mathcal{N}$, respectively. Note that $\mathcal{N}_F$ and $\mathcal{N}_T$ may be tightly integrated and even share some functionality. To evaluate the DfT quality, two test sets are required. The design specification T_F specifies the performance requirement on $\mathcal{N}_F$. The DfT test set T_T is the test set to be performed in conjunction with $\mathcal{N}_T$. It should be noticed that

1. In general, only a subset of T_F is applied during manufacturing testing to reduce the overall test time and cost.
2. One may not be able to characterize all of the specifications in T_F because of limited access.

3. T_T is not limited to DfT-only tests, *i.e.*, the tests that cannot be performed without $\mathcal{N}_T$. In practice, T_T may contain tests that are applied by external ATE.

Since the ultimate goal of any test set is to differentiate defective ICs from defect-free ones, it is nature to evaluate the quality of a test set in terms of its ability to correctly identify the good and bad manufactured instances. For AMS circuits without DfT, the definition of defective instances is simple-an instance is defective if it fails any of the specification in T_F; otherwise, it is defect-free. For DfT-equipped AMS circuits, the definition is slightly modified to take into account the DfT circuit-an instance is defective if it fails any of the specification in T_F when the DfT part, $\mathcal{N}_T$ is disabled; otherwise, it is defect-free. The defect and fault coverage of T_T, the DfT test set, is then defined as:

D, **defect coverage**. The percentage of defective instances that cannot pass T_T.

Y, **yield coverage**. The percentage of defect-free instances that pass T_T.

Based on the above definitions, the quality of $\mathcal{N}_T$ and T_T is

$$Q = \frac{\alpha Y + \beta D}{\alpha + \beta} \tag{2}$$

where α and β are two application-dependent parameters of which the values depend on whether yield or defect coverage if favorable.

3.2 The Evaluation Flow

The DfT evaluation flow is illustrated in Fig. 1. It consists of three major steps: process simulation, circuit simulation, and coverage analysis. In the following, we will show the details of each of the steps.

3.2.1 ProcessSimulation

In the process simulation step, the inputs are $\mathcal{N}$ and the process variation information. As we have mentioned in Section 2.3, process variations are divided into local and global variations. Thus, two sets of process information are required.

Let *p*1, *p*2, ⋯, *pn* be the set of circuit parameters to be considered. The global variation information includes:

σ_1^G, σ_2^G, ⋯, σ_n^G The standard deviations of p_i's caused by global variations. σ_i^G's are either from the IC foundry or obtained through measure-ment results.

R^G The global correlation matrix. It is an *n*-by-*n* matrix and each entry r_{ij}^G corresponds to the global variation correlation between p_i and p_j.

Given σ_i^G's and R^G, sets of circuit parameters that mimic the global variations can be obtained using a normal random number generator and the Cholesky decomposition method.

For local process variations, the Pelgrom model in Eq. 1 is utilized. However, since the spatial term, S_P, is so smallthat onlythe size-dependent partis considered. The required local variation information includes:

A_{p1}, A_{p2}, ⋯, A_{pn} The area proportionality constant of p_i's.

R^L The local correlation matrix. It is similar to the global correlation matrix except that it characterizes the correlation between local variations.

Generation of sets of circuit parameters that reflect the local variations is similar to that for global variations. The main difference is that local variations are functions of the device sizes.

For each circuit instance, local and global variations are summed up to simulate the overall process variation effect.

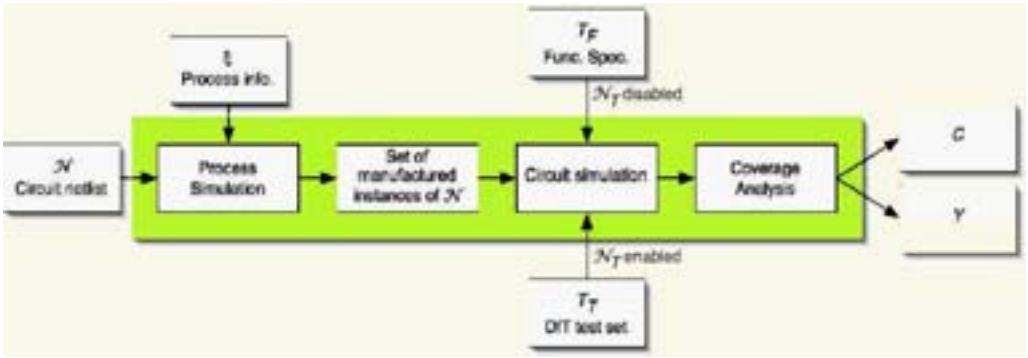

Fig. 1 The DfT evaluation flow

$$p_i = \mu_{p_i} + \Delta p_i^G + \Delta p_i^L \quad (3)$$

where μ_{p_i} is the nominal value of parameter p_i, and Δp_i^G and Δp_i^L are the global and local variations, respectively.

3.2.2 Circuit simulation and coverage analysis

In this work, we use HSpice as the underlying circuit simulator. To realize the above mentioned circuit parameter distribution, each device in $\mathcal{N}$ is assigned a unique model. Then, when simulating each circuit instance, a different set of models obtained in Eq. 3 are assigned to the devices.

Apparently, the simulation time will be unacceptably long if all circuit parameters are considered. In our implementation, only four parameters, θ, V_{T0}, β, and γ, are considered according to [27].

To derive the yield and defect coverage, two runs of circuit simulations are performed for each circuit instance. In the first simulation, $\mathcal{N}_T$ is disabled and T_F is used as the test set. The simulation results in this run determine whether an instance is defective or defect-free. In the second simulation, $\mathcal{N}_T$ is enabled and T_T is used as the test set. After the two simula-tion runs, the circuit instances are divided into four classes shown in Fig. 2, where Ω represents the set of all manufactured instances, Ω_F the set of instances that pass T_F, and Ω_T the set of instances that pass T_T, According to the previous definitions, one has

$$Y = \frac{|\Omega_T \bigcap \Omega_F|}{|\Omega_F|} \quad (4)$$

$$D = \frac{|\{\Omega - \Omega_F\} \bigcap \{\Omega - \Omega_T\}|}{|\Omega - \Omega_F|} \quad (5)$$

where $|X|$ is the size of set X.

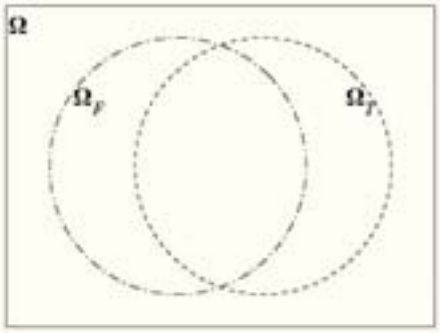

Fig. 2 Yield and defect coverage

4. EXPERIMENTAL RESULTS

In this section, we will first show the flash ADC with built-in ramp generator. Then, we will depict the simulation setup followed by simulations results.

4.1 The Flash ADC Under Test

The CUT to demonstrate the propose DfT evaluation method is shown as the shaded blocks in Fig. 3. The functional part of the CUT is a 6-bit flash ADC of which the main components include a resistor ladder and an array of comparators. The DfT circuit consists of a ramp generator and an analog switch which selects the ADC input. The control block is responsible for (1) selection of the ADC input, and (2) control of the ramp generator. The output codes of the ADC are stored in the memory and analyzed by the DSP block to obtain INL (integral nonlinearity), DNL (differential nonlinearity), and ENOB(effective number of bits). The nominal performance of the ADC and ramp generator are summarized in Table 1.

Although the test control block, the DSP block, and other digital parts are also affected by process variations, they are not included and considered be-cause they are digital circuits and can be effciently tested by already available digital testing techniques.

4.2 Simulation Setup

The design specification of the flash ADC consists of static INL/DNL testing and dynamic ENOB testing. For static testing, an ideal ramp is applied through the functional input and linear histogram analysis is performed to obtain INL and DNL. For dynamic ENOB testing, the test stimulus is an ideal sine wave at 157.92 KHz applied through the ADC's functional input. FFT is performed on the collected ADC output codes to derive SNDR(signal to noise and distortion ratio). ENOB is then obtained by

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02} \quad (6)$$

In this example, the DfT test set consists of only static INL and DNL tests using the linear histogram analysis method. The linear ramp is generated by the ramp generator. The two test sets are summarized in Table 2. Note that

1. The DfT test set does not include dynamic test which, as will be seen later, limits its capability in capturing dynamic defects.
2. Ideal signals are utilized in design specification simulation as it is meant to determine if an instance is defective or not.

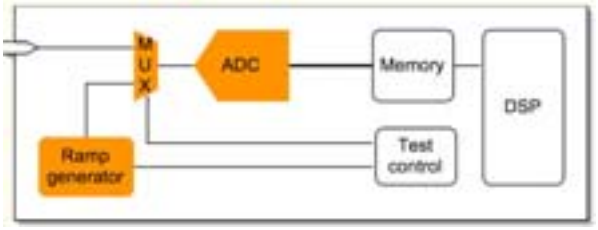

Fig. 3 Block diagram of the CUT

Table 1 Summary of the CUT

ADC	Sampling rate	100 MSPS
	Technology	TSMC .35 μm
	Supply voltage	3.3 volts
	Full scale range (FSR)	1.6–2.5 volts
	INL	0.47 LSB
	DNL	0.22 LSB
	ENOB	5.38 bits
Ramp generator	FSR	1.5–2.6 volts
	Slope	≥ 30 average code bits
	Linearity	≥ 7 bits

Table 2 The test specifications

ADC specification (T_F)	INL	≤ 0.5 LSB
	DNL	≤ 0.5 LSB
	ENOB	≥ 5 bits
DfT test set (T_T)	INL	≤ 0.5 LSB
	DNL	≤ 0.5 LSB

3. The linea rramp produced by the ramp generator suffers process variations and inherent circuit non-linearity which limit the achievable test ac-curacy.

4.3 Simulation Results

One thousand circuit instances are generated to estimate the yield and defect coverage; and they are divided into four classes as shown in Fig. 4. The DfT quality, according to our definition, is

$$Y = \frac{627}{627 + 52} \tag{7}$$

$$= 0.9234 \tag{8}$$

$$D = \frac{206}{115 + 206} \tag{9}$$

$$= 0.6417 \tag{10}$$

$$Q = 0.7825 \tag{11}$$

Here α and β areboth settoone — an unbiased choice between yield and defect coverage.

One can see that high yield coverage is achieved;

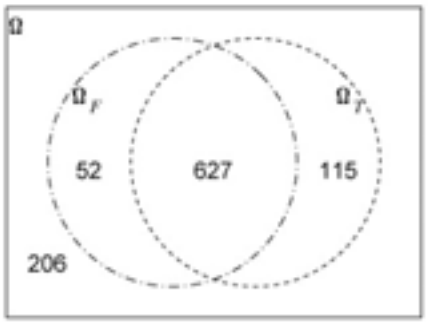

Fig. 4 Results of the first experiment

however, the defect coverage is rather low. Also, it's interesting that only 627 + 52 = 679 instances pass the design specification, which corresponds to a yield of 67.9% and indicates that redesign or design optimization is necessary to enhance the manufacturing yield.

Intuitively, the main cause of the low defect coverage is lack of dynamic test in the DfT test set. To validate this, we purposely remove the ENOB specification from the design specification and redo the coverage analysis. The results are shown in Fig. 5. Compared with the previous results, it is observed that there are 104 defective instances that can only be detected by the dynamic ENOB testing. Thus, one can confirm that the ramp generator (for static testing) alone is insufficient. Two possible ways to enhance the DfT quality are:

1. Redesign the ramp generator so that it can generate high-speed signal to facilitate dynamic testing.
2. Perform dynamic testing using external ATE during manufacturing testing. In this case, DfT is still useful because one doesn't have to apply the extern dynamic test to the instances that fail the DfT static tests. In this example, the percentage is about 33%.

5. CONCLUSION

In this paper, we have proposed an approach to evaluate the quality of a DfT design. Based on process

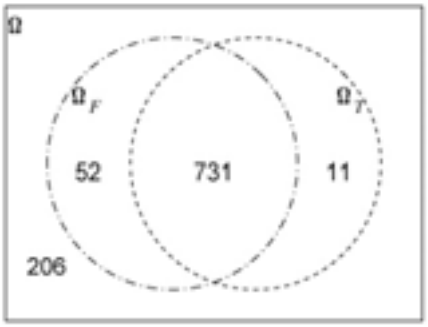

Fig. 5 Results of the second experiment

variation information, the reported DfT criterion is more realistic and practical than past research results. A flash ADC with built-in ramp generator was used to demonstrate our idea. With the proposed method, the weakness of the DfT is found and two possible solutions are identified based on the results.

The DfT evaluation framework currently only supports parametric process variations and suffer long simulation time. We will enhance the tool's capability to handle catastrophic defects and investigate techniques to improve the circuit simulation efficiency.

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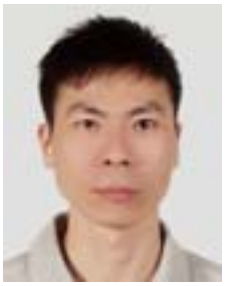

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