A K-Band Miniature, Broadband, High Output Power HBT MMIC Balanced Doubler with Integrated Balun

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***Abstract* — A K-Band frequency doubler using InGaP HBT is developed, which features high fundamental frequency rejection, flat conversion loss over wide bandwidth, and high saturation output power. To obtain a balanced signal, a compact on-chip lumped rat-race hybrid is implemented. The circuit exhibits a measured conversion loss of 4 dB over the output frequencies from 14 to 22 GHz. The fundamental frequency suppression is better than 20 dB and the second harmonic saturation output power is higher than 7.3 dBm with a miniature chip size of 1 mm × 1 mm.**

***Index Terms* — MMIC, Doubler, HBT.**

I. Introduction

High frequency source signals can be either generated by using high frequency oscillators or by multiplying signals from lower frequency signals. The high frequency doublers have been realized using GaAs MESFET or HEMT [1]-[9]. FETs are attractive to generate second harmonic signal due to the square law relation [8]. However, HBT devices are more advantageous to have low 1/f noise and higher output power [10]-[11]. HBT frequency doublers can also be integrated with VCOs in the same HBT process. The frequency multipliers using HBT devices were lately reported [10]-[12]. Si/SiGe HBT doubler has been reported in [10] with promising results with relatively low-power performance. In [12], a doubler using SiGe HBT exhibits high efficiency and high gain but requires an additional off-chip balun. The other doubler using GaAs HBT reported in [10] has good performance, but the doubler core needs an additional buffer amplifier to enhance the signal power.

This paper presents a MMIC balanced frequency doubler based on a 2-μm InGaP/GaAs HBT process to obtain output frequencies from 14 to 22 GHz. By using a lumped rat-race hybrid in the balanced distributed input port [13], the input signal will be 180° out of phase and cancel out at the output port to achieve good fundamental frequency rejection [9]. The measure conversion gain is about -4 dB from 7 to 10.5 GHz fundamental frequency, with the fundamental frequency suppression of higher than 20 dB. The second harmonic saturation output power is higher than 7.3 dBm. To our knowledge, this work demonstrates the highest output power among HBT doublers without buffer amplifiers, and also has a broad bandwidth of 44%, and relatively low conversion loss with no additional buffer amplifiers. Moreover, in spite of the on-chip lumped element rat-race hybrid, the doubler is very compact with a chip size of 1 mm × 1 mm. Table I compares of the previously reported frequency doublers [1]–[12] and our work. It is observed that our MMIC doubler demonstrates wide-band performance and high saturation output power, with good fundamental rejection. The conversion loss is relative low even without a buffer amplifier. This HBT doubler has good performance in all aspects compared with other III-V compound based HBT and HEMT MMIC doubler in this frequency range.

II. Device Characteristics and MMIC Process

The MMIC doubler was fabricated using the 2-μm InGaP/GaAs HBT MMIC process provided by Global Communication Technology (GCT). The HBT device exhibits an f_T of 32GHz, an f_{max} of 60 GHz, a current gain ($ß_f$) of 78, and a power density 2.5 kW/cm^2. The collector to base breakdown voltage BV_{cbo} is higher than 25 V, and the collector to emitter breakdown voltage BV_{ceo} is higher than 14 V. This MMIC process also includes thin-film resistors, MIM capacitors, and spiral inductors. The wafer is thinned to 4-mil for the gold plating of the backside and reactive ion etching via holes.

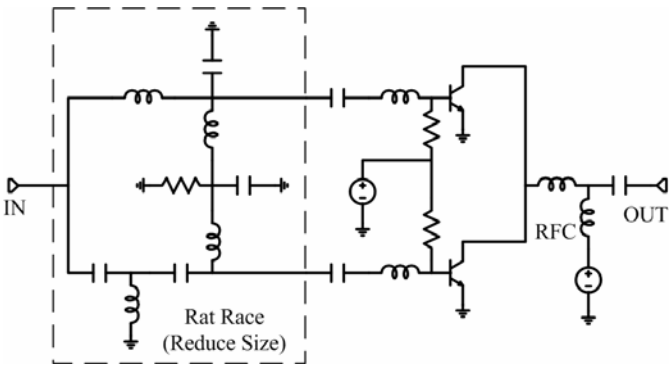

Fig. 1. The schematic diagram of the balanced doubler circuit.

III. Circuit Design

Fig. 1 is the schematic diagram of the doubler. The input fundamental frequency is split into two balanced ports with

identical power and 180° phase difference, which feed into two identical input match circuits and transistors, and then combined at the output port. The second harmonic signals that pass the active transistors will be in-phase combined and the odd frequency components will be 180° out-of-phase and cancelled at the output.

The doubler composes of two identical common-emitter HBTs. In order to reduce dc power consumption and generate higher second harmonic component, the HBTs are biased for class-AB operation, where the nonlinearity of the transconductance versus base-to-emitter voltage can be used for second harmonic frequency generation. The bias conditions are optimized for the conversion gain and the output power.

The 180° balun is a lumped element rate-race design for broadband. Three inductors and four MIM capacitors are used to implement the balun, similar to that reported in [13]. When the sum port is terminated with 50 Ω, the simulation results show that the insertion losses of the rat-race are both 3.2 dB with the phase difference of less than 10°.

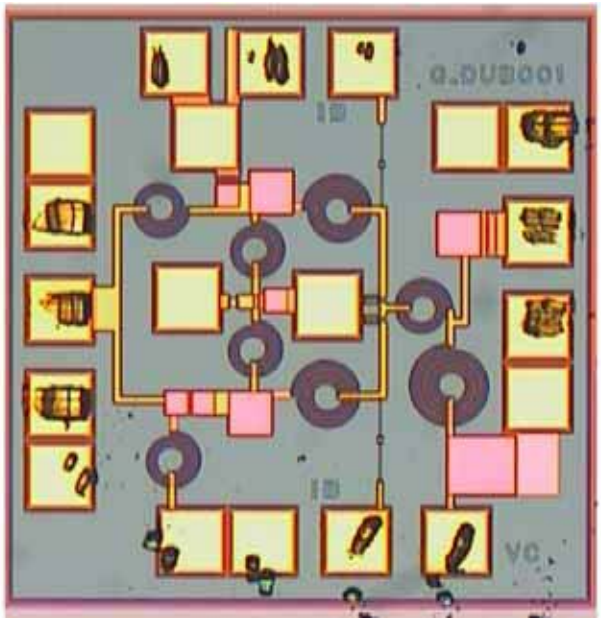

Fig. 2. Chip photograph of the MMIC doubler with a chip size of 1 × 1 mm^2.

The output load impedance is designed for maximizing second harmonic conversion gain (minimizing the loss) and ensuring the stability. Because of the out-of-phase input signal in each transistor, the load for fundamental frequency is virtual-short-circuited and thus higher isolation can be achieved. The doubler performance is simulated via harmonic balanced technique of the commercial computer-aided-design software Microwave Office. The HBT device nonlinear model used in the simulation is Gummel Poon model provided by the foundry. The chip photograph is shown in Fig. 2, with a size of 1 mm × 1 mm including all the testing pads.

IV. Measurement Results

The circuit is measured via on-wafer probing. The two transistors are biased at 5V collector-to-emitter voltage, while the base dc currents are near zero for the class-B operation. The total dc power consumption is approximately 75mW.

The conversion gain and the input fundamental frequency suppression versus input signal power under 9 GHz input frequency are plotted in Fig. 3. It is observed that the output power is not saturated till 7.3 dBm, which is the highest output saturation power among the reported doublers using HBT devices in this frequency range.

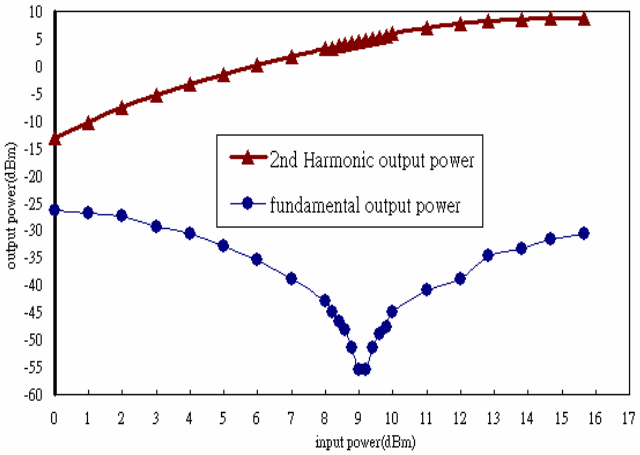

Fig. 3. Measured conversion gain and fundamental frequency rejection at 9-GHz input signal with input power from 7 to 15 dBm.

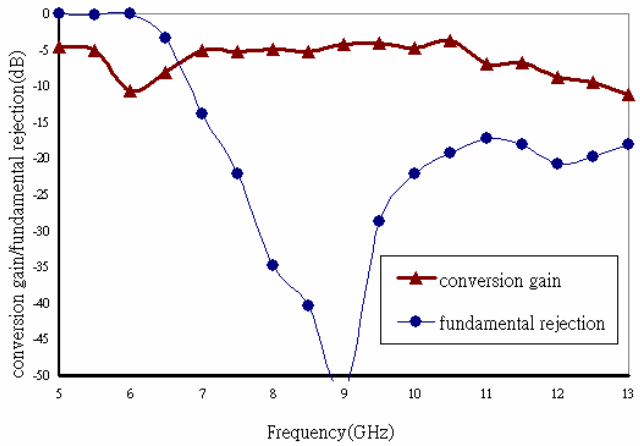

Fig. 4. Measured conversion gain and fundamental frequency rejection at 12-dBm input power with frequency from 5 to 13 GHz.

The conversion gain and the input fundamental frequency suppression versus input frequency under 12 dBm input power are presented in Fig. 4. The doubler has about 4 dB conversion loss from 7 to 10.5 GHz input frequencies and demonstrated a broad-band frequency doubling performance. The fundamental frequency rejection is greater than 20 dB for the entire band, and better than 30 dB at input frequency from 8 to 10 GHz.

TABLE I
COMPARISON OF THE PREVIOUS REPORTED FREQUENCY DOUBLERS

Ref.	Technology	F_0 (GHz)	Bandwidth	Conversion Gain (dB)	Power consumption (mW)	Size (mm^2)	Psat (dBm)	Features
[1]	0.1 μm InP HEMT	82	8.5%	-2	n.a	1.32	5	
[2]	0.1 μm InP HEMT	90	n.a	-6	n.a	3.4	-6	
[4]	0.14 μm InP HEMT	30	20%	1	275	n.a	7	
[6]	0.15 μm pHEMT	26	22%	1	275	3	6	Built-in buffer amplifier
[7]	0.12 μm pHEMT	38	n.a.	1	n.a	n.a	9	
[8]	0.15 μm pHEMT	31	16%	-8.5	50	1	4	Rat-race hybrid
[9]	0.15 μm pHEMT	20	51%	-4	132	1.5	5	Distributed doubler
[10]	InGaP HBT	15	52.6%	7.5	200	0.42	5	Built-in buffer amplifier
[11]	SiGe HBT	13	7.4%	-12	20	n.a	-9	Rat-race hybrid
[12]	SiGe HBT	8.5	27%	4	9.2	0.245	6.5	Additional balun needed
This Work	**InGaP HBT**	**9**	**44.4%**	**-4**	**75**	**1**	**7.3**	**Rat-race hybrid**

V. CONCLUSION

A miniature and wide-band balanced doubler using an on-chip lumped element rat-race hybrid has been described in this paper. The balanced distributed doubler is designed for broadband operation and achieves 14-21 GHz output frequency range. The conversion loss is between 4 and 5 dB with the fundamental frequency rejections are better than 20 dB. The circuit also provides over 7.3-dBm second harmonic saturation output power without a buffer amplifier. Besides, it has a compact chip size of only 1 mm × 1 mm.

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