ANALYTICAL AND T-CAD MODELING OF PENTACENE THIN-FILM TRANSISTORS

Yet- Min Chen [(a)] , Yu-Sheng Chen [(a)] , Jian-Jang Huang [(a),1)], Jiun-Haw Lee [(a)], Yu-Wu Wang [(b)] and Yi-Kai Wang [(b)]
[(a)]Graduate Institute of Electro-Optical Engineering, National Taiwan University,
1 Roosevelt Rd, Sec.4, Taipei,106 Taiwan
[(b)]Electronics Research and Service Organization, Industrial Technology Research Institute
Hsinchu, 310 Taiwan
[1)] Corresponding Author: Phone: 886-2-23635251 ext 408, Fax: 886-2-2367-7467
e-mail: jjhuang@cc.ee.ntu.edu.tw

ABSTRACT

Many researches report that the mobility in organic material is dependent on not only the gate field but also the grain size. There is also some evidence to prove that the gate length is strongly related to the carrier mobility. We construct both the analytical model of organic thin film transistor and the large signal circuit model designed by T-CAD to fit the measured $I_{DS}-V_{DS}$ curves. We first apply basic $I_{DS}-V_{DS}$ equations in both triode and saturation regions with mobility μ best fitted to measured I-V curves. The "best-fitted" μ increases with the gate length, and is related to the increase of total channel resistance due to the presence of small grains size of pentacene next to source/drain electrodes. We then use the Advanced Design System software to design the large signal circuit model. Similar to the MOSFET, we add the additional parameters to fit the $I_{DS}-V_{DS}$ curves, ex: Rgd, Rgs, and Rp. Here, Rgd. With the circuit simulation, we find that Rgd presents the leakage current from gate to source, and it affects the slope of curves in the saturation region in the $I_{DS}-V_{DS}$ curves. The equivalent circuit can fit the $I_{DS}-V_{DS}$ curves very well with the proper parameter set.

Keywords: organic, transistor, analytical model, DC model

1. INTRODUCTION

1.1 Potential of OTFTs

Over the past several years, organic thin film transistors (OTFTs) have become popular due to their unique properties compared with other semiconductor electronic devices. Low cost process and large area applications which inorganic semiconductor based device can't achieve is the biggest advantage of OTFTs, and these advantages create lots of opportunities for commercial products. Low temperature processing and substrates with structural flexibility make all impractical applications before become real. For example, OTFT circuits can be applied to flexible circuit boards for mobile phones and digital cameras, opening up a new arena for flexible electronics in the consumer market. Furthermore, the low-cost, large-area advantages have enabled OTFTs logic circuits good candidates for identification tags. Except the potential of the application of the radio frequency Identification (RFID), e-paper, OTFTs could be fabricated by printing which has large potential for low-cost and easy process.

The flexible and low temperature process allows organic transistors to be applied to several substrates which were reported by numerous papers. Jackson reported transistors on substrates such as a key ring and a cotton-polyester bed sheet [1], and a project is developing organic electronics on a sheet of paper [2]. Another issue of organic material has the sensitivity of the atmosphere, which is regarded as a disadvantage could be used in a special application. The ambient atmosphere can alter the conducting of an organic semiconductor, such as the mobility, drain current of OTFT. These characters were utilized by Crone et al as odor sensor based on OTFT technology [3]. Vapors could be sensed by odor sensor by changing its current characteristic which could recover to within 2% of the original value after exposure in about one minute.

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Utilizing organic characteristics as odor sensor is not the only application of OTFT technology, conducting polymers also used in different applications as well. Polymers made as capacitors and batteries were published by Yasafuku, which shows the potential of the integration of these with electronics can envision all-polymer organic circuit in the future. We other than odor sesor, RFID, e-paper, all polymer circuit, the display applications is anther promising field for organic material. Organic light-emitting diode (OLED) has attracted a lot of concentration recently due to its flexibility, low response time, RGB availability, good contrast ratio, and the potential of low cost.

An integration of OLED and OTFT was published by Henning Sirringhaus et al [4]. They fabricated an all-polymer integrated device that demonstrated a high-mobility conjugated polymer field-effect transistor to drive a polymer light-emitting diode of similar size. The field effect transistor (FET) uses regioregular poly(hexylthiophene). The performance is comparable to inorganic amorphous silicon FETs, with field-effect mobilities of 0.05 to 0.1 $cm^2/(V*Sec)$ and ON-OFF current ratios reaches 6 orders. The OTFT-OLED integrated device represents a step toward all-polymer optoelectronic integrated circuits such as active-matrix OLED displays.

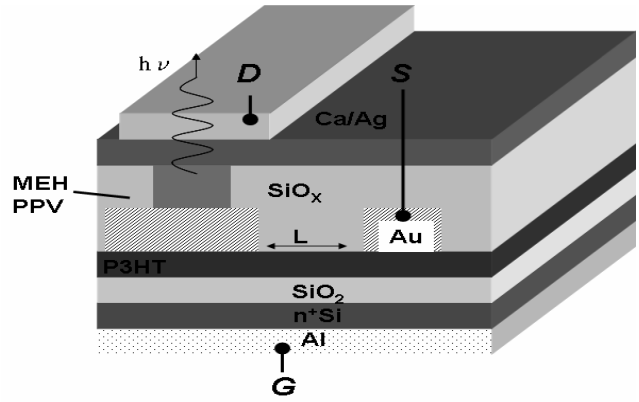


Fig. 1. Cross section of the integrated P3HT OTFT and MEH-PPV LED. The device is a part of a full active-matrix polymer LED pixel. The lamellar structure of the regioregular P3HT and its orientation relative to the SiO2 substrate. Resource : ref. [4]

Anther applications include in switching devices, such as active-matrix flat-panel displays (AMFPDs) based on either liquid crystal pixels (AMLCDs) [6] or organic light-emitting diodes (AMOLEDs) [7, 8]. Polycrystalline silicon or hydrogenated amorphous silicon (a-Si:H) are most commonly used in the active layer in thin film transistor backplane of AMLCDs at present, and polycrystalline silicon based thin film transistors (TFTs) have better performance but involve more complicate process. And all these inorganic materials have common characteristics that they all use high temperature process which is not suitable for plastic substrate. Organic characteristics, low temperature process and well performance OTFTs have a lot of potential in display applications. "Electronic paper" displays [9] based on pixels comprising is an new applications of OTFTs, along with electrophoretic ink-containing microcapsules [10], smart cards, electronic identification tags, or "twisting balls." [11]

OTFTs are regarded as a competitive alternative to the traditional inorganic semiconductor based field effect transistors, Low cost, large area, and low process temperature bring new opportunities where inorganic semiconductor could not obtain, and open the new market for this new technology.

1.2 Mobility issue

Organic thin-film transistors have been developed for more than a decade. Conjugated polymers, oligomers, or other small molecules have been envisioned as viable alternative to more traditional, mainstream FETs based on inorganic materials. Due to the relative low mobility of the organic semiconductor, OTFTs cannot compete with other field effect transistors based on silicon inorganic semiconductor, such as amorphous-silicon, polymer-silicon. These materials also have field effect mobility as organic material, but with three orders of magnitude higher [5]. Because of the lower mobility, instead of applications at very high switching speed and fast response time, such as telecommunication, OTFTs have been used in novel thin film transistors which require large-area coverage, structural flexibility, low-temperature processing, and, especially, low cost.

Cost down principle can bring OTFTs to the consumer market, but all the applications is mostly limited to the research field. So far, there are only a few commercial products made by OTFTs.

One bottleneck is the device geometry result from the limited methods of patterning the organic semiconductor layer. Organic material is not suitable for photolithography, therefore we have to use shadow mask, spin coater and sputter. Limited methods means undesired effects might dominate the characteristics, such as increased leakage and subthreshold slope stem from less control of the charge induced by the gate metal. Bottom contact structure affects the grain size and the crystal disordering due to the surface energy of the contact metal and interface issue between metal and organic material.

Process condition is another significant issue of organic material. Low cost and large scale fabrication can be performed by spin-coating, stamping, and printing. These easy processes make the fabrication cost lower than inorganic material, but the organic must be soluble during these processes. However, most of the organic materials are not soluble unless side chains are added to the molecules of the polymer material. But the side chains could alter the chain arrangement of polymer and affect the performance of the current characteristic. Vacuum deposition which requires more expensive processes and higher process temperature has better performance, but is not suitable to plastic substrates.

More significant than all issues mentioned above is the mobility problem. Even operating at large voltage (10~50 V), organic transistor render only several μA/μm. The power consumption results from the high operating voltage and could cause the devices unreliable. Mobility is mainly dependent on the semiconductor material, different material results in different mobility.Among the OTFT devices reported, pentacene is typically employed as the channel layer due to its the superior carrier mobility, which results from the high degree of molecular ordering seen during its film growth [12-15].

The magnitude of mobility is dominated by carrier transport and the number of traps at the grain boundaries and the semiconductor insulator interface. The carrier transport behavior in organic semiconductor is very different from that in conventional crystalline semiconductor. Carriers traveling through organic molecules are experiencing large numbers of traps and hence the carrier mobility in OTFTs is much lower than conventional crystalline field effect transistors FETs. Up to now, numerous papers have been published on the device modeling of OTFTs by modifying conventional FET models [16-18]. The model [16] is based on the trap distribution deduced from temperature-dependent current-voltage measurements on Au/alpha-sexithienyl (a6T)/Au symmetrical structures, which comprises a dominant single shallow trap level located near the valence-band edge. Numerical and approximate analytical derivations of the saturation current density as a function of the gate voltage have been made. From these calculations, it appears that the threshold voltage corresponds to the filling of traps, and is a surface equivalent of the trap-filled limit voltage in bulk space-charge-limited current.

Some papers also described the dependence of pentacene mobility on the channel length [8-10]. They found the mobility decrease with the channel length and concluded that the low extrinsic mobility of short channel bottom gate OTFTs is attributed to high series channel resistance [1, 10]. Despite the discussion of mobility dependence on channel lengths, a physical model to describe the carrier transport behavior in the pentacene channel layer and an empirical model to correlate $I_{DS} - V_{DS}$ OTFT performance at different channel lengths are hardly seen.

In this paper, we develop a model for bottom gate pentacene OTFTs that takes various channel lengths into account. We first employ a conventional FET model by varying the mobility term to best fit measured $I_{DS} - V_{DS}$ curves, at separate channel length. The relationship between channel length and carrier mobility is plotted and analyzed. And then we use the Advanced Design System (ADS) software to design the large signal circuit model. Different from the MOSFET, we add the additional parameters to fit the $I_{DS} - V_{DS}$ curves, ex: Rgd, Rgs, Rp, and Ro. Here, Rgd, Rgs is the resistance between gate to drain and gate to source, Rp is plastic resistance in series with the Ro resistance, this resistance has to be considered when the short cannel effect appears. Ro is the resistance refer to channel length modulation (CLM) effect in filed effect transistors. With the circuit simulation, we find that Rgd presents the leakage current from gate to source, and it affect the slope of saturation region in the $I_{DS} - V_{DS}$ curves. The equivalent circuit can fit the $I_{DS} - V_{DS}$ curves very well with the proper parameter set.

Finally, we propose a pentacene grain size model to explain the behavior of carrier transport through the channel layer, and describe al the physical behavior at the channel layer with proper math expression.

2. EXPERIMENTAL

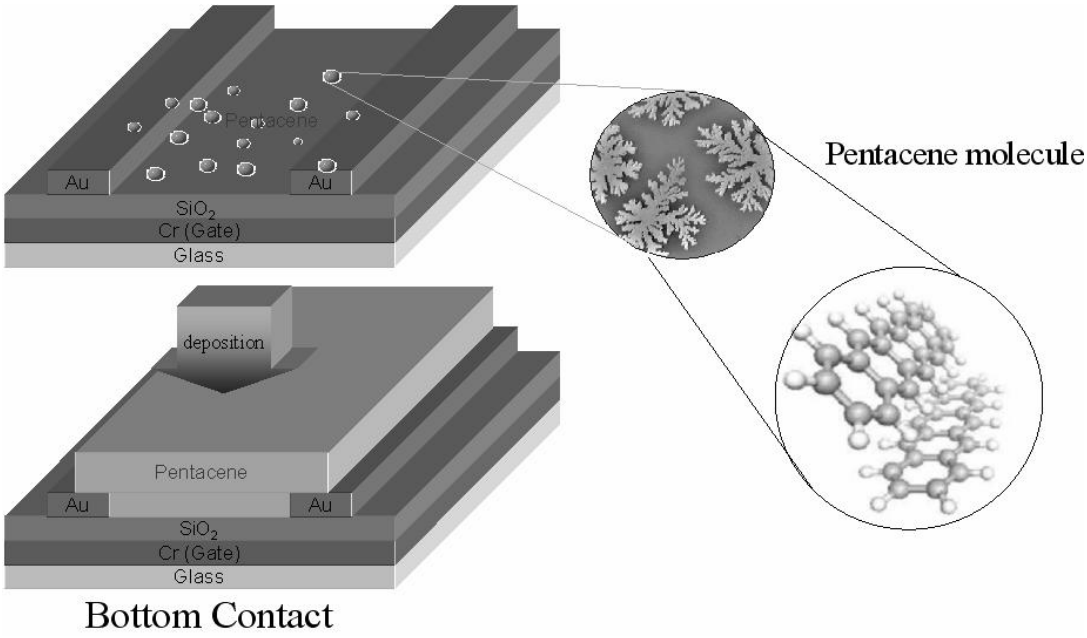


Fig. 2. Schematic diagram of a bottom-gate pentacene transistor with Au top contact.

Fig. 2 schematically shows the structural of a bottom gate TFT device. First, a 1500 Å metal layer of Cr was deposited on a glass substrate by sputtering and patterned by photolithography as the gate electrode. Silicon dioxide with a thickness 3000 Å was deposited as the insulating layer, fabricated by plasma-enhanced chemical vapor deposition (PECVD) with He, O2 and tetraethylorthosilicate at 800 mTorr and 380 ℃.

The semiconductor material in the active layer is Pentacene, which was purchased from FLUKA Chemical (97+%) and used without any further purification. The pentacene layer with a thickness of 1000 Å was deposited at a rate 0.5 of Å /s. To make the grain size larger, the substrate was maintained at 70 ℃. The pentacene active layer was thermally sublimated in a vacuum at a pressure of 10-5Torr. The pentacene film morphology was characterized using a Seiko Instruments. SPA-500 scanning probe microscope with DF20 tip and operated in non-contact mode at 1 Hz scan rate. Finally the gold source-drain electrodes were deposited on the surface of the pentacene film with shadow mask. We have designed OTFT devices with different channel lengths (57μm, 47μm, 37μm, 27μm and 17μm, respectively). The channel width was fixed to 10000μm. An HP 4155A Precision Semiconductor Parameter Analyzer was used to measure the electrical characteristics of the organic TFTs. The pentacene active layer was patterned using a shadow mask around the measured organic TFTs to minimize the drain current leakage.

3. ANALYTICAL MODEL

We have designed OTFT devices with different channel lengths (L=57μm, 47μm, 37μm, 27μm and 17μm, respectively). Examples of devices measured show as solid lines in Fig. 3. To predict the analytical behavior of these OTFTs, we applied basic $I_{DS} - V_{DS}$ transistor equations in the triode and saturation regions. The onset of transistor mode from triode to saturation regions is determined when drain to gate voltage is equal to the threshold voltage, which is measured from $I_{DS} - V_{GS}$ curves.

At low drain voltage (V_{DS}), the drain current (I_{DS}) increases linearly with V_{DS} (triode regime) and is approximately given by using the traditional equation at triode regime:

$$I_D = \frac{w\mu C_i}{L}\left((V_G - V_T)V_{DS} - \frac{1}{2}V_{DS}^2 \right) + I_{dark} \quad (1)$$

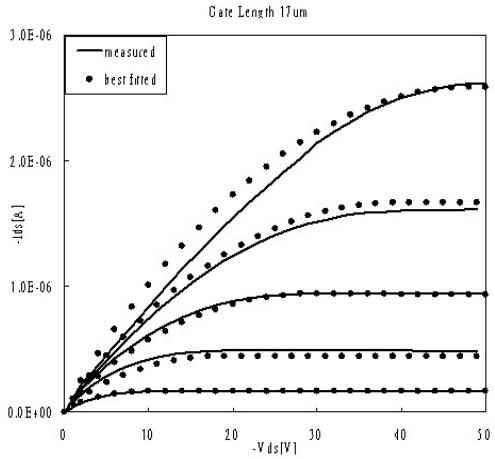
where W and L represent the gate width and gate length respectively, and Ci is the capacitance per unit area of the insulating layer. V_T is the threshold voltage, μ is the field effect mobility, and Idark refers to the dark current or leakage current.

Drain current tends to saturate when $V_D << (V_G - V_T)$. This regime is the saturation regime, and the drain current can be describe by the equation below,

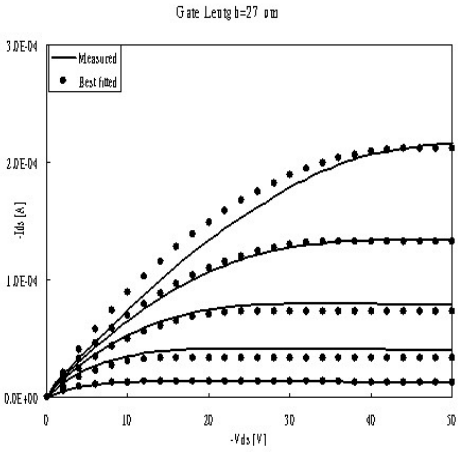
$$I_D = \frac{w\mu C_i}{2L}(V_G - V_T)^2 + I_{dark} \quad (2)$$

In both equations, the leakage current, Idark, in our simulation is assumed zero.

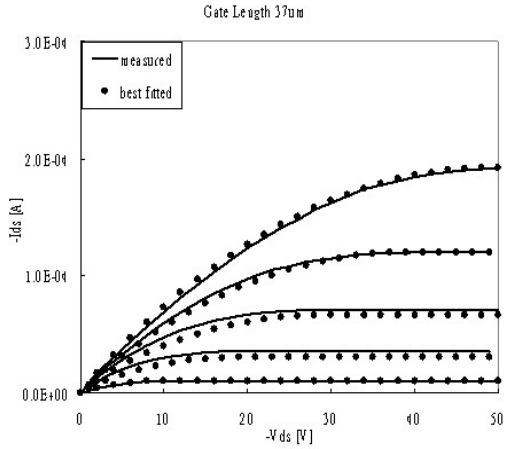
The measured results on channel lengths 57μm, 47μm, 37μm, 27μm and 17μm are show as solid lines in Fig. 2. To elaborate the behavior of these devices, we applied equation (1) and equation (2) with mobility μ best fitted to measured I-V curves. The "best-fitted" mobility μ is illustrated in Fig. 3, and is related to the increase of total channel resistance due to the presence of small grains size of pentacene next to source/drain electrodes.



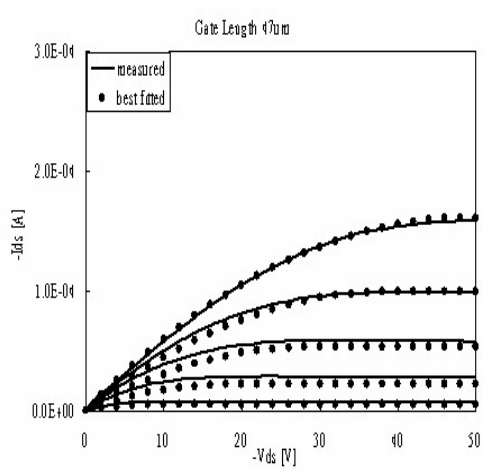
(a) Gate length 17μm



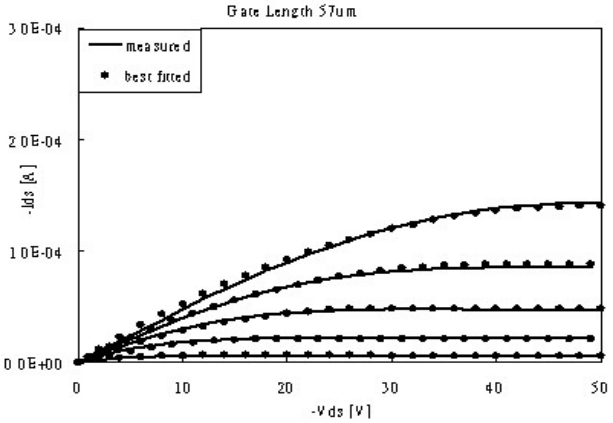
(b) Gate length 27μm



(c) Gate length 37μm



(d) Gate length 47μm



(e) Gate length 57μm

Fig. 3. $I_{DS} - V_{DS}$ characteristics of OTFT at various gate voltages, where channel width was 10000μm and channel length was 17-57μm.

4. CIRCUIT SIMULATION

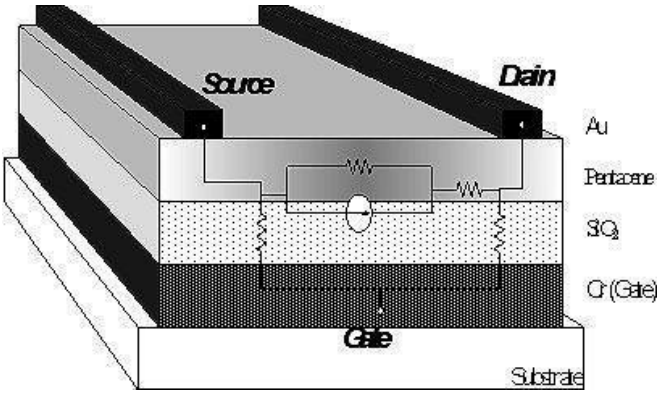


Fig. 4. Schematic diagram of a bottom-gate pentacene transistor with Au top contact, circuit is shown on the device scheme.

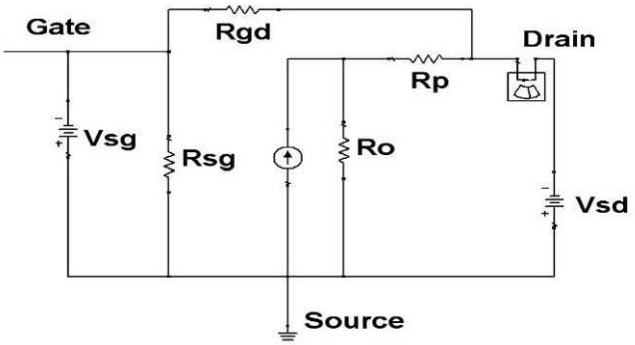


Fig. 5. The large signal circuit model of OTFT. We add the additional parameters to fit the $I_{DS}-V_{DS}$ curves, ex: Rgd, Rgs, and Rp.

We then use the Advanced Design System (ADS) software to design the large signal circuit model. It is shown in Fig. 4. The voltage control current source in the center of the circuit is controlled by two basic formulas used in analytical model. However, unlike the analytical model, we include the leakage current in the circuit simulation. And we add the additional parameters to indicate some physical phenomenon, ex: Rgd, Rgs, and Rp. Here, Rgd, Rgs is the resistance between gate to drain and gate to source, Rp is plastic resistance in series with the Ro. Here, Rp has to be considered when the short cannel effect appears. With the circuit simulation, we find that Rgd presents the leakage current from gate to source, and it affect the slope of saturation region in the $I_{DS}-V_{DS}$ curves., Ro is the resistance refers to channel length modulation (CLM) effect, and it could deduce from the traditional formulas shown below, and V_A can be derived from the :

$$R_o = \frac{\partial I_D}{\partial V_D}\Big| \qquad V_G \quad cons\tan t \tag{3}$$

$$I_D = \frac{w\mu C_i}{2L}\left(V_G - V_T\right)^2\left(1+\lambda V_D\right) \tag{4}$$

$$R_o = \left[\frac{w\mu C_i}{2L}\left(V_G - V_T\right)^2\lambda\right]^{-1} \tag{5}$$

$$R_o \sim \left[\lambda I_D\right]^{-1} \sim \frac{V_A}{I_D} \tag{5}$$

The equivalent circuit can fit the $I_{DS}-V_{DS}$ curves very well with proper parameter. The fitting result is shown in Fig. 6. The channel length modulation effect is not so obvious in our device. The best fitted mobility consist with the analytical model mentioned above.

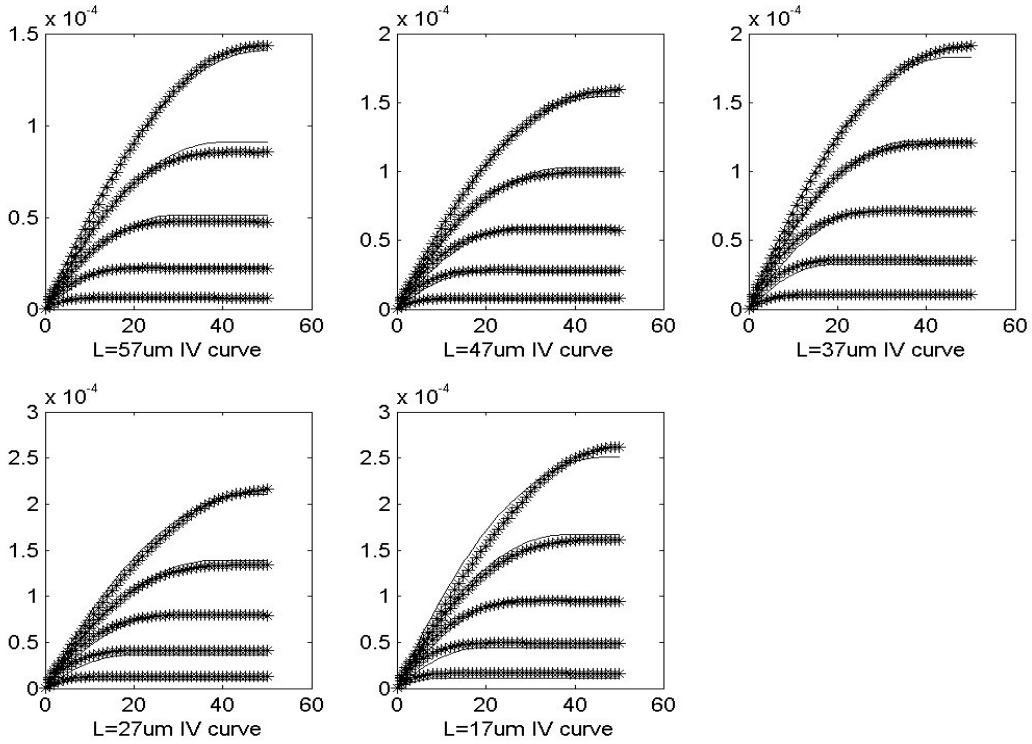


Fig. 6. The equivalent circuit fitting result.

5. DISCUSSION

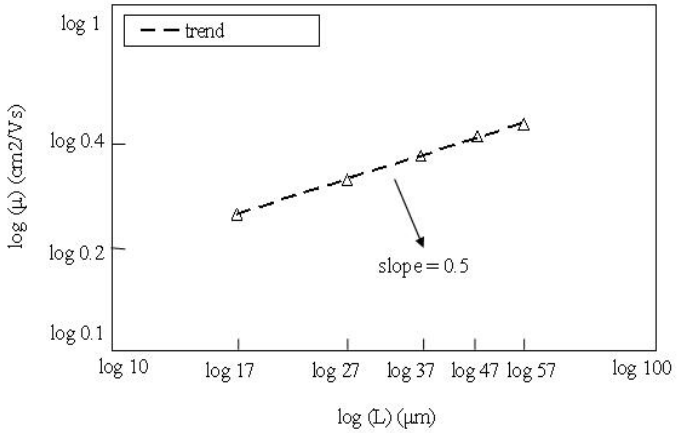
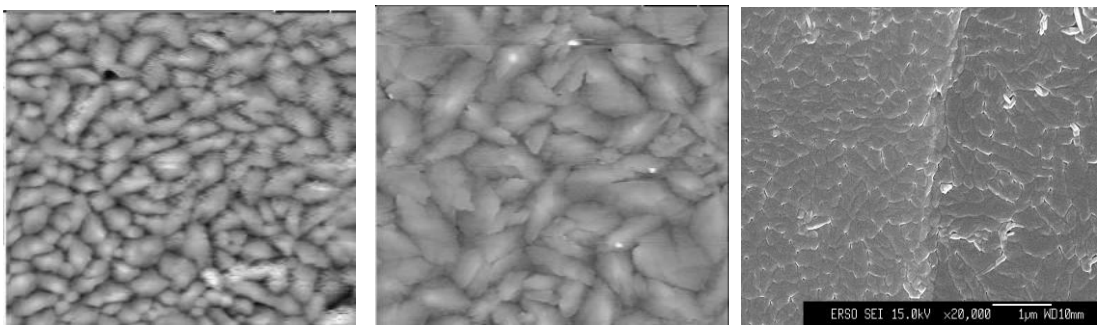


Fig. 7. "Best fitted" mobility v.s. channel length for all of the OTFTs under investigation. α is determined from the slope in log scale.

With the analytical model and circuit simulation, we can extract the carrier mobility μ best fitted to the measured $I_{DS} - V_{DS}$ curves are illustrated as square dots in Fig. 3 and Fig. 6. We plot log μ v.s. log L in Fig. 7 in order to understand the behavior of carrier mobility in pentacene active layer with different gate length, while the μ is the best fitted carrier mobility extracted from analytical model and circuit simulation. From this plot, we can see mobility increases with the channel length easily, which can be attributed to the presence of small grains of pentacene next to source-drain electrodes as published in [19]. We can use the formula to express the physical relationship:

$$\mu \propto L^{\alpha} \tag{5}$$

where α is a parameter related to process condition, and it is 0.5 in our device.



(a) (b) (c)

Fig. 8. AFM photos of pentacene under the source electrode (a) and the channel (b), the image scale size is 5 um x 5 um. And SEM picture is taken on the pentacene near the edge of metal contact (c).

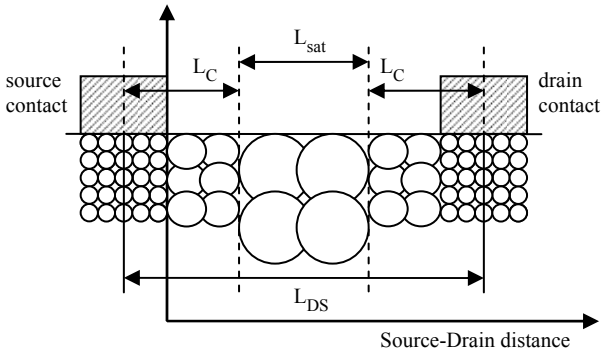
AFM (atomic force microscopic) photos can explain the physical relationship more clearly. AFM photos are taken on pentacene under the source electrode (Fig. 8(a)) and in the center of the channel (Fig. 8(b)). We can learn that smaller grains of pentacene grown on the metal electrode and larger grains grown in the center of the channel. SEM (scanning electron microscopic) photos are also taken on the interface between pentacene and metal contact. The average grain size implies the physical relationship. The average grain size under metal contact is estimated around 0.127 μm*μm while that of the channel is around 0.235 μm^2 .

The microcrystalline structure in smaller-grain pentacene is attributed to the less ordering of molecules on the source and drain electrode, which the grain boundaries could be the obstacle when the carriers move in the region [20]. This results in higher resistance in the interface between patacene and metal contact. The overall resistance in channel could be express as

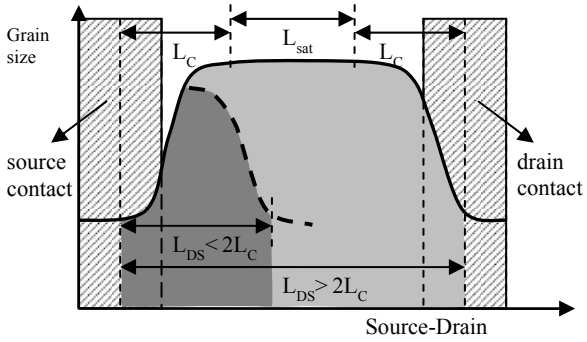
$$R_{Total} = R_{contact} + R_{channel} \tag{6}$$

where Rcontact and Rchannel represent resistances near the contact and in the center of the channel, respectively. The overall channel resistance and thus the carrier mobility will be determined by the dominance of Rcontact or Rchannel, depending on the geometrical size of contact electrode and channel.

With the confirmation of AFM and SEM photo, now we have more confidence on the physical relationship between the carrier mobility and gate length. However, the physical meaning of the exponential term α in the formula is not clear. We propose a model to express the mechanism of the increase of mobility with gate length. We believe the grain size would increase as the L_{DS} increases until it saturates. As shown on the fig. 9, L_C is the critical length for small grain size region, and L_{SAT} is the length for uniformly large grain size region. If the total gate length (L_{DS}) is not long enough, the carrier moving in the active channel will experience an increase and then a decrease of grain size when the transistor is turned on. The larger grain size, the less grain boundaries are, which makes carriers moving in the channel easier. Therefore the larger size region would results in the higher mobility. And if the total gate length is longer, carriers would move faster until the grain size saturates at L_C . When the grain size saturates, the carriers traveling along the channel will experience primarily the larger-grain pentacene (thus low contact resistance and high mobility) region. Generally, since carriers can move more quickly in regions without too many boundaries, the effective channel resistance of large-grain region is smaller.



(a)



(b)

Fig. 9. Illustration of pentacene grains along the channel layer (a). Depending on the source-drain distance, carriers will or will not travel through constantly large (saturated) pentacene grains (b).

From the discussion above, the exponential term α is contributed by both small-grain and large-grain regions. In our devices, since the relationship works for all of the channel lengths and fits the measured $I_{DS} - V_{DS}$ curves pretty well, the grain size in the channel is dominant by smaller-grain pentacene. Therefore, L_{DS} is much smaller than $2L_C$ for all of our devices according to the proposed model mentioned above. And it is believed that α will be higher if large grains dominate in the channel region when L_{DS} is much larger than $2L_C$. We plot the carrier mobility v.s. channel length extracted from [21] to verify our theory. Two distinct slopes are clearly seen in the log μ v.s. log L plot. For channel length shorter than 50~ 60 μm, α is around 0.85, while α is around 1.46 for channel length above 50~ 60 μm. Those two distinct slopes confirm our model of the dependence of carrier mobility on the pentacene grain sizes.

In conclusion, we measured $I_{DS} - V_{DS}$ curves from pentacene OTFTs with channel length from 17μm to 57μm. The results can be fitted pretty well in analytical model and circuit simulations, and the carrier mobility could be explained by the exponential expression above, where α is 0.5 in our devices. We then develop a grain size model along the channel region to explain the carrier behavior. For our devices, since $L_{DS} << 2L_C$, where L_C is the critical distance between large and small grain size, smaller-grain pentacene dominant in the device channel. We expect the slope α will be larger for large channel length devices ($L_{DS} >> 2L_C$), which is verified from carrier mobility reported from other group.

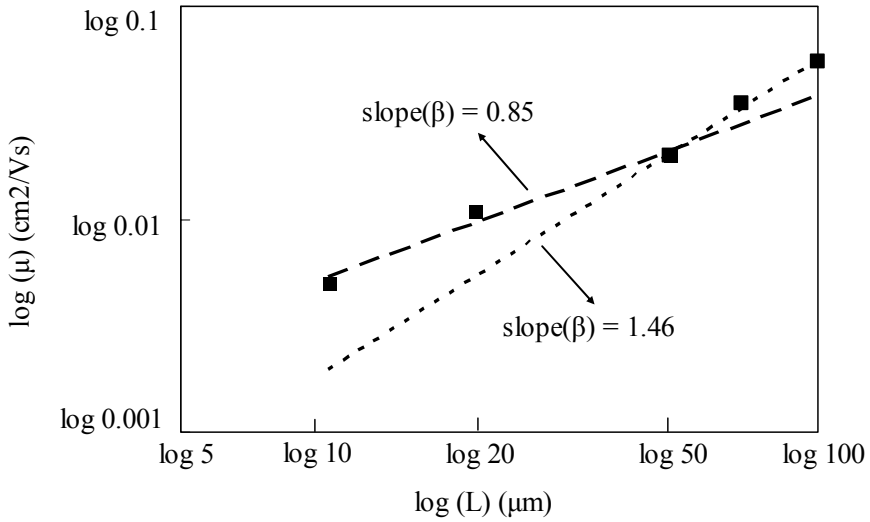


Fig. 10. Carrier mobility as a function channel length (extracted from ref. [21]). The slope α can be separated into two values depending on the channel length.

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