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Abstract

An intermediate Si layer in $Si_{1-x}Ge_x$ film, replacing the conventionally compositional graded buffer layer, was used to fabricate a relaxed SiGe substrate of high quality. The intermediate Si layer changes the relaxation mechanism of the SiGe thin film via the generation of {3 1 1} dislocation loops. The {3 1 1} dislocation loops are formed in the intermediate Si layer to prompt a state of relaxation in the SiGe overlayer, provide the defects for trapping of threading dislocations (TDs) and leave a SiGe top layer with low dislocation density. For the SiGe/Si/SiGe samples, the residual strain and TDs on the top SiGe layer are independent of the SiGe underlayer thickness. With a 700 nm thick $Si_{0.8}Ge_{0.2}$ overlayer, such a $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ heterostructure with a smooth surface has a TD density of 8.9×10^5 cm^{-2} and 3% residual strain. Owing to the different main relaxation mechanisms in SiGe films, the surface root mean square roughness of this relaxed buffer with a low density of surface pits was measured to be about 3 nm, which is lower than that of the sample without any intermediate Si layer (13 nm). Relaxation of the SiGe overlayer depends on the thickness of the intermediate Si layer. Optimization on relaxation in the SiGe/Si/SiGe structure with an intermediate Si layer of 50 nm is done. Strained Si *n*-channel metal-oxide-semiconductor field effect transistors with various buffer layers were fabricated and examined. The effective electron mobility for the strained Si device with this novel substrate technology was found to be 80% higher than that of the Si control device. The SiGe thin films with the intermediate Si layer serve as good candidates for high-speed strained Si devices. The global strain in the Si channel with a SiGe/Si/SiGe buffer is still beneficial for short channel devices.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Due to the carrier mobility enhancement in the channel, strained Si complementary metal oxide semiconductor field effect transistors (CMOSFETs) have been reported to have a great improvement on dc and RF characteristics [1, 2]. In order to introduce tensile stress into Si, strain-relaxed SiGe layers grown on a Si substrate are required to serve as virtual substrates [3, 4]. The conventional method for achieving fully relaxed SiGe epilayers with low TDs densities is to

grow 1–2 μm thick CGB SiGe layers, in which mismatch strain is gradually released by a modified Frank–Reed (MFR) mechanism [5, 6]. However, such a process takes a long growth time, reduces the throughput, increases the cost and results in surface roughness, which were induced by the buried misfit dislocations and TDs. Therefore, a thin buffer layer that relaxes the strain and reduces the total thickness of epilayers is desired.

Thin relaxed SiGe layers grown onto a low-temperature (LT) Si or SiGe buffer have been reported with an MBE method [7, 8]. The LT layer provides low-energy sites for dislocation nucleation, point defects for trapping of threading dislocation propagation and plays the role of template to adjust the mismatch strain. Powell *et al* made SiGe deposited on silicon on insulator (SOI) to obtain a thin relaxed SiGe buffer [9]. There are several reports which use the H- and He-implantation and subsequent annealing to initiate the relaxation process of thin strained SiGe layers [10–12]; the formation of defect bands induced by ion implantation improves relaxation in SiGe layers via preferred nucleation of dislocation loops in the defect region which extend to the SiGe heterostructure to form the misfit dislocation.

We have fabricated high-quality relaxed SiGe films using an intermediate Si or $Si_{1-y}C_y$ layer [13, 14]. The misfit dislocations induced by the SiGe overlayer were formed or confirmed at the interface of SiGe overlayers and the intermediate $Si_{1-y}C_y$ layers. In the case of SiGe/$Si_{1-y}C_y$/SiGe by employing C atoms of 1.4%, an array of misfit dislocations at the interface of the top SiGe and SiC layer was responsible for the release of mismatch strain on the top SiGe layer [14]; however, the dislocation loops in the intermediate Si layer of SiGe/Si/SiGe samples enhanced the relaxation in the SiGe overlayer [13]. Addition of C atoms in the inserted Si layer led to the SiGe/$Si_{1-y}C_y$/SiGe films with a rough surface and increased the complexity of process integration. Hence, the intermediate Si layer may be an appropriate choice for the application of SiGe/$Si_{1-y}C_y$/SiGe samples. In this paper, a systematic investigation of the dependence of surface morphology and relaxation of the SiGe films on the thicknesses of the top SiGe, the inserted Si layer and the SiGe underlayer was done. The defect structures and surface morphology in the SiGe samples with or without an inserted Si layer were examined. The thermal stability of SiGe/Si/SiGe with a thin SiGe upper layer was also carried out. A strained Si *n*-channel MOSFET with compositional graded $Si_{1-x}Ge_x$ buffer layers, this new structure and a control Si device were fabricated and their electrical characteristics and electron mobility were examined.

2. Experiment

The starting materials adopted were 4 inch diameter, 15–25 Ω cm, *p*-type (0 0 1)-oriented Si wafers. All the epitaxial films investigated in this work were grown at 600 °C in a commercially available multi-wafer UHV/CVD system (Unaxis Sirrus 400) [15]. During the entire process step, the growth temperature was holding the same. The base pressure of the reactor is typically below 8×10^{-9} mbar. High purity SiH_4, 5% GeH_4 diluted in He, 100 ppm B_2H_6 diluted in He

Table 1. Summary of the structure for the samples in this work. Here, t_{2SiGe} and t_{1SiGe} indicate the thickness of the SiGe overlayer and the underlayer.

| Sample no.	Structure of sample	t_{2SiGe} (nm)	t_{Si} (nm)	t_{1SiGe} (nm)	Density of TDs (cm^{-2})
A	SiGe/Si/SiGe	70	50	70	$< 10^4$
B	SiGe/Si/SiGe	140	50	70	$< 10^4$
C	SiGe/Si/SiGe	280	50	70	$< 10^4$
D	SiGe/Si/SiGe	420	50	70	$< 10^4$
E	SiGe/Si/SiGe	700	50	70	8.9×10^5
F	SiGe/Si/SiGe	700	25	70	5×10^5
G	SiGe/Si/SiGe	700	75	70	10^6
H	SiGe/Si/SiGe	700	100	70	5×10^5
I	SiGe/Si/SiGe	700	No	70	$> 10^9$
J	CGB	700	No	70	5×10^5

were used as Si, Ge and B sources, respectively. Prior to the epitaxial growth, the *p*-Si wafers were dipped in a 10% HF solution to maintain the H-termination on the surface of the substrate before transferred to the UHV/CVD reactor in a quartz wafer boat through a load lock which is pumped down to a base pressure of 1×10^{-6} mbar within 10 min. A 60 nm thick Si buffer layer was first grown to cover the wafer surface. The details of the following epitaxial structure for the samples are listed in table 1. In the SiGe/Si/SiGe structure, the intermediate Si layer was sandwiched between the SiGe underlayer and the overlayer. Finally, a strained Si layer of 20 nm was deposited as a channel for the fabrication of *n*-channel strained Si MOSFETs.

The SiGe epitaxial films have been characterized using high-resolution x-ray diffraction (HRXRD), atomic force microscopy (AFM), cross-sectional transmission electron microscopy (XTEM) and Raman scattering. After performing the rocking curve around the (0 0 4) reciprocal lattice with HRXRD (model: Bede QC 200), the Ge fraction and thickness of SiGe were determined with commercial analysis software Bede RADS®. The thickness of SiGe was also verified by XTEM (model: JEOL 2010F). The surface morphology of the samples was characterized by Normaski microscopy and AFM in a tapping mode. The density of TDs was estimated by Schimmel etch pit methods [16]. The degree of strain relaxation was determined by Raman scattering and HRXRD. After epitaxial growth, strained Si *n*-MOSFET with various SiGe virtual substrates was fabricated by a standard MOSFET process, which is listed in table 2 [3]. For comparison, 770 nm thick $Si_{0.8}Ge_{0.2}$ films grown on a 2 μm thick CGB layer with the Ge concentration linearly graded from 0% to 20% and controlled epitaxial Si devices were also prepared. Some modified processes were used to avoid the high-temperature exposure of the strained Si device. Figure 1 shows the schematic diagram of surface-channel strained Si *n*-MOSFETs with the structure of SiGe/Si/SiGe in this work. Control devices were also prepared with the epitaxial Si on a bulk Si substrate with the same process flow. All devices have a channelling doping with B of 3×10^{16} atoms cm^{-3}. The electron effective mobility was extracted from the drain current and split-CV measurements on a large-area device.
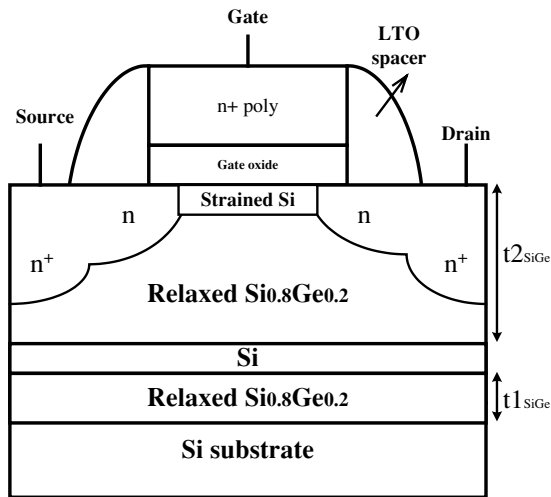
Figure 1. Schematic illustration of strained Si *n*-MOSFETs on relaxed $Si_{0.8}Ge_{0.2}$ with an intermediate Si layer.

Table 2. Process flow of the fabrication of *n*-MOSFET devices in this work.
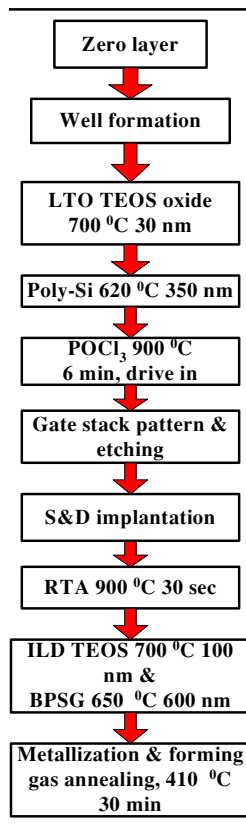

3. Results and discussion

3.1. Microstructure of SiGe/Si/SiGe

Figure 2 shows an XTEM image of the $Si_{0.8}Ge_{0.2}$ film with a 50 nm thick intermediate Si layer and a SiGe overlayer of 770 nm (sample E). The defects in the inserted Si and TD density on the top SiGe layer were not influenced by the thickness of the SiGe underlayer ($t1_{SiGe}$). It was found that most of the TDs were prevented from propagating into the
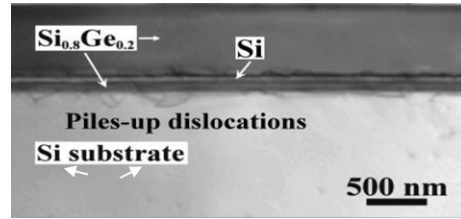
**Figure 2.** XTEM image of sample E with an intermediate Si layer.
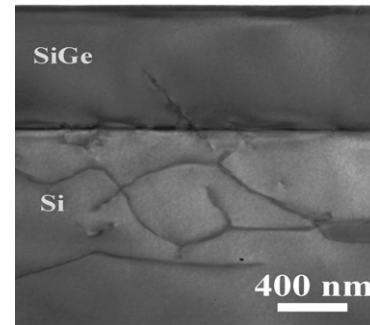
Figure 3. XTEM image of sample I without the intermediate Si layer.

top SiGe layer, remained trapped at the $Si/Si_{0.8}Ge_{0.2}/Si$ buffer interface and left a $Si_{0.8}Ge_{0.2}$ overlayer with low defect density. Using the Schimmel etch method, the TD density in the $Si_{0.8}Ge_{0.2}$ film was measured to be 8.9×10^5 cm^{-2}. However, low density of pile-up dislocations which are threading down several micrometres into the Si substrate is also seen in the observed image. From the high-resolution TEM (HRTEM) image of the sandwiched Si layer in the $Si_{0.8}Ge_{0.2}$ film, numerous dislocation loops lying on {1 1 3} planes were found to form and were confined in the intermediate Si layer [13]. The microstructure of a 770 nm thick $Si_{0.8}Ge_{0.2}$ film on Si (sample I) with a lot of pile-up dislocations is presented in figure 3. In this sample, the pile-up dislocation in the SiGe layer and the Si substrate were induced by the MFR mechanism. The density of TDs in the SiGe/Si/SiGe buffer is of the same order (10^5–10^6 cm^{-2}) as that of the samples with CGBs (sample J), and less than the sample without the intermediate Si layer (10^9 cm^{-2}). This indicates that the intermediate Si layer provides enough and effective nucleation sites for the dislocation loops to relax the mismatch strain and offers the defects to trap the propagation of TDs; this behaviour is similar to that of LT [7]. The density of dislocations, which penetrated into the Si buffer for the sample with an intermediate Si layer, is higher than that of the sample without any intermediate Si layer. It was obvious that the inserted Si layer changed the relaxation mechanism during the growing process. It was well known that the surface morphology of epitaxial SiGe is determined by the buried misfit and TDs. The surface morphology of $Si_{0.8}Ge_{0.2}$ on different buffers will be discussed in the next section.

3.2. Surface morphology of SiGe/Si/SiGe

In the previous study, numerous shallow pits were formed on the surface of the samples without the intermediate Si
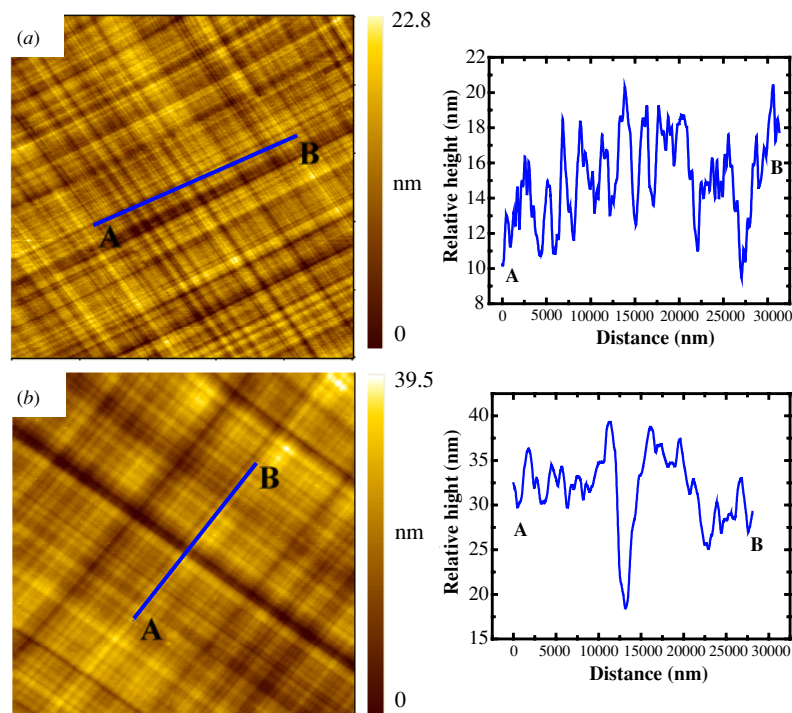
Figure 4. AFM scanned image ($50 \times 50 \ \mu m^2$) and the associated line scan showing the surface morphology of strained Si on (*a*) a relaxed SiGe buffer with an intermediate Si layer (sample E) and (*b*) relaxed SiGe on the graded buffer structure (sample J).

layer. These shallow pits were formed at regions with high and inhomogeneous strain to relax the mismatch strain on the sample surface [13]. On the other hand, in samples with an intermediate Si layer, almost a pit-free surface was observed (not shown here). This observation implies that the intermediate Si layer in the SiGe film indeed changes the strain relaxation mechanism during the growth. As a result, it is not necessary to induce pits to reduce the strain energy and maintain a smooth surface [13, 17, 18]. The AFM measurements were carried out on $50 \times 50 \ \mu m^2$ areas. For this sample E (SiGe/Si/SiGe), the RMS surface roughness was obtained from AFM to be about 3 nm as shown in figure 4(*a*). For samples I and J (figure 4(*b*)), the RMS surface roughness was measured as 13 and 6 nm, respectively. There are some deep troughs induced by the pile-up of buried dislocations. This scenario is the same as the XTEM observation of microstructure. A drastic decrease in the surface roughness of $Si_{0.8}Ge_{0.2}$ of 770 nm can be achieved using an intermediate Si layer.

3.3. Strain relaxation SiGe/Si/SiGe

The x-ray (0 0 4) rocking curves of samples A to E with increasing thickness of $Si_{0.8}Ge_{0.2}$ overlayers are shown in figure 5(*a*). We compared the x-ray diffraction spectrum near Si (0 0 4) and SiGe (0 0 4) of sample A with a 70 nm thick SiGe top layer on the Si/SiGe buffer and the simulated curve obtained from Bede RADS®. The good agreement between the experimental XRD spectrum and the associated dynamical scattering simulation indicated that the multilayer is a pseudomorphic stack of $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ as shown in figure 5(*b*). Both the SiGe layers were chosen to be 70 nm,
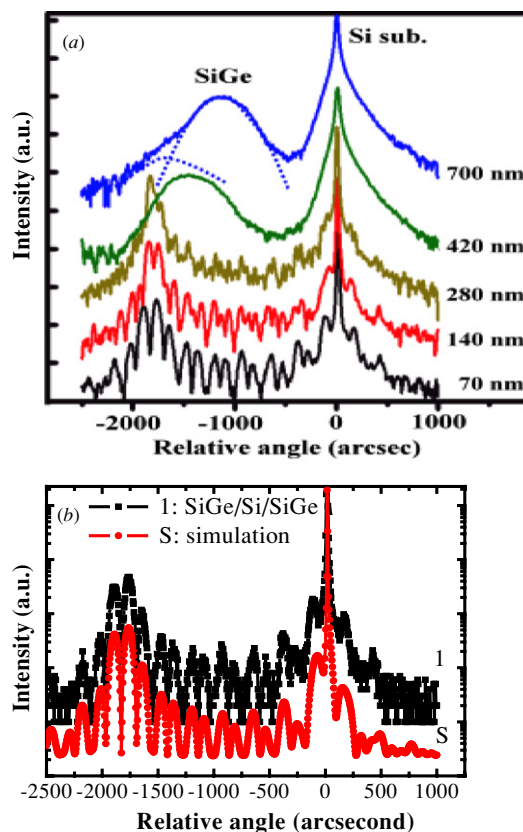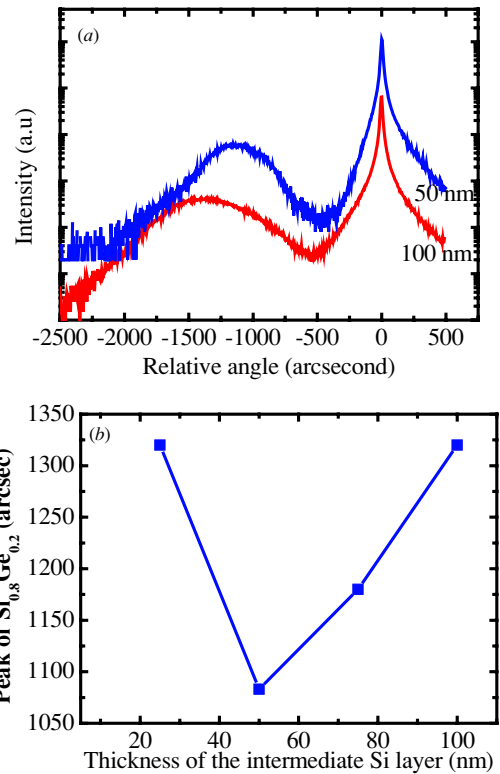

Figure 5. X-ray (0 0 4) rocking curves of (*a*) the samples with the $Si_{0.8}Ge_{0.2}$ overlayers of 70, 140, 280, 420 and 700 nm and (*b*) sample A and the associated dynamical scattering simulation. The thicknesses of the underlayer $Si_{0.8}Ge_{0.2}$ and the Si intermediate layer are 70 and 50 nm, respectively.

which is below the critical thickness predicted by the Mattews–Blakeslee theory. No strain relaxation in sample A was observed. The obvious strain relaxation was observed when the SiGe overlayer thickness increases from 280 to 420 nm. Furthermore, the sample with a 700 nm thick SiGe overlayer is already close to full relaxation. Meanwhile, by analysing the peaks of Si–Si and Si–Ge in the Raman spectrum of 700 nm thick $Si_{0.8}Ge_{0.2}$ overlayers for sample E, we obtained the Ge composition in the uniform layer of 19.5% with a residual strain of only 3%. The controlled sample (sample I) without the intermediate Si layer has a residual strain of up to 25%. These results indicated that the $Si/Si_{0.8}Ge_{0.2}$ structure can help to reduce the equilibrium critical thickness of the SiGe overlayer. The rate of strain relaxation is influenced by the density of nucleation sites for misfit dislocations, effective stress and growth temperature [19]. The {3 1 1} dislocation loops in the intermediate Si layer and the SiGe underlayer may also play the role for strain adjusting template, and provide enough nucleation centres for the generation of the misfit dislocations. These results will enhance the propagation of misfit dislocations and prompt the relaxation process on the top SiGe layer with a flat surface and low residual strain for the SiGe/Si/SiGe samples. However, the accumulated stress in the SiGe film without the intermediate Si layer was released via the formation of pits on the surface and the generation of misfit dislocations between the SiGe film and the Si substrate; the release of mismatch strain was ineffective. The total $Si_{0.8}Ge_{0.2}$ thickness (770 nm) of sample E is smaller than that of CGBs with a relaxation of 88% (2770 nm). The relaxed SiGe buffer can be achieved for required relaxation using the intermediate Si layer instead of CGBs.

In figure 6(a), two x-ray (0 0 4) rocking curves of sample E with a 50 nm thick inserted Si layer and sample F with a 100 nm thick inserted Si layer are depicted. For sample E, two peaks of SiGe (0 0 4) can be well resolved. The asymmetric peak shape of SiGe (0 0 4) indicated the different degrees of strain in the overlayer and the underlayer SiGe layer. The x-ray peak of SiGe (0 0 4) is located at −1100 and −1836 arcsec, which originate from the $Si_{0.8}Ge_{0.2}$ overlayer and the underlayer, respectively. The effect of the intermediate Si thickness on the relaxation of the $Si_{0.8}Ge_{0.2}$ overlayer is presented in figure 6(b). The strain relaxation in the $Si_{0.8}Ge_{0.2}$ overlayer reached a maximum as the thickness of the intermediate Si is 50 nm. A thinner (<25 nm) or thicker (>75 nm) intermediate Si layer could result in poor strain relaxation. We further found that the strain relaxation in the $Si_{0.8}Ge_{0.2}$ overlayer is independent of the thickness of the $Si_{0.8}Ge_{0.2}$ underlayer.

Figure 7(a) shows a series of XRD rocking curves for the as-grown sample C and samples annealed at different temperatures for 30 s. Relaxation in SiGe/Si/SiGe with a 280 nm thick SiGe upper layer is a function of annealing temperature as shown in figure 7(b). After annealing at 800 °C, the $Si_{0.8}Ge_{0.2}$ film was 32% relaxed. Even when the annealing temperature increased up to 1000 °C, relaxation in sample C reached only 54%. Houghton [19] suggested that relaxation in SiGe depends on its thickness, Ge composition and annealing temperature. According to the results of relaxation in SiGe in samples A to E, the dominant factor of relaxation in SiGe/Si/SiGe was determined by the thickness of the SiGe


Figure 6. (a) X-ray (0 0 4) rocking curves of 50 and 100 nm thick Si intermediate Si layers and (b) the degree of strain relaxation in the $Si_{0.8}Ge_{0.2}$ overlayer as a function of the intermediate Si thickness.
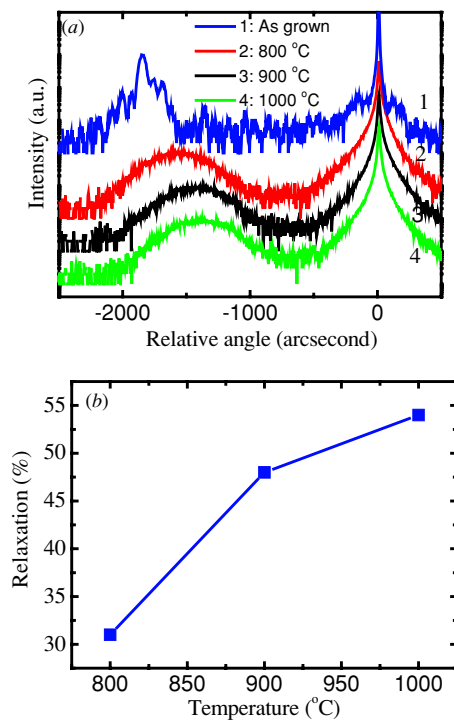

Figure 7. (a) A series of x-ray (0 0 4) rocking curves of sample C before and after annealing at different temperatures for 30 s and (b) relaxation in sample C as a function of the annealing temperature.

upper layer. The state of relaxation in SiGe/Si/SiGe with a SiGe upper layer of 280 nm was limited by its thickness.

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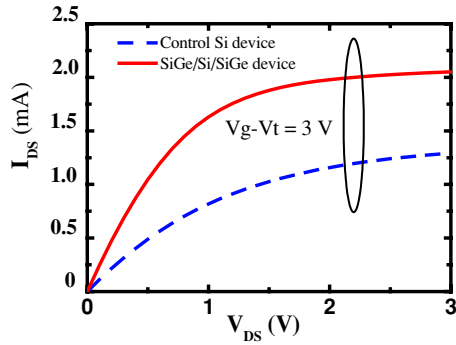
Figure 8. Drain current (I_D) versus drain voltage (V_D) as a function of overdrive (V_{GS}–V_T) for strained Si *n*-MOSFETs with an epitaxial Si control device and $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ with an intermediate Si layer.
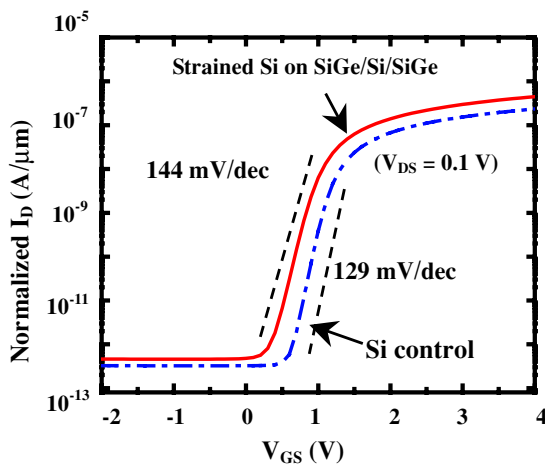
Figure 9. Subthreshold I_{DS}–V_{GS} characteristics of strained Si on a SiGe/Si/SiGe buffer and Si control devices at $V_{DS} = 0.1$ V.

3.4. Performance of the n-MOSFETs

Strained Si *n*-channel MOSFETs were fabricated, and their drain current and carrier mobility enhancement characteristics were also examined. As shown in figure 8, all devices show good linear and saturation characteristics. In addition, the strained Si devices exhibit a similar enhancement with different V_{GS}–V_T of the output characteristics. The drain current (I_{DS}) of the device (gate length/width = 1/25 μm, thickness of gate oxide = 30 nm) with an intermediate Si layer as buffer is about 60% higher than that of epitaxial Si control devices, and compared favourably with that of the CGBs layer. Long-channel strained Si *n*-MOSFETs (gate length/width = 100/200 μm, thickness of gate oxide = 30 nm) with various relaxed $Si_{1-x}Ge_x$ substrates as well as Si control devices were fabricated to extract the effective electron mobility μ_{eff} in the strained Si channel by the split CV methods. Both strained Si and bulk Si control devices show an excellent subthreshold behaviour and a low off-state leakage current as shown in figure 9. Compared with the controlled Si devices, the subthreshold characteristics were not degraded by the introduction of the SiGe film into devices. The effective mobility μ_{eff} calculated from the split capacitance–voltage measurements and a universal mobility representing an
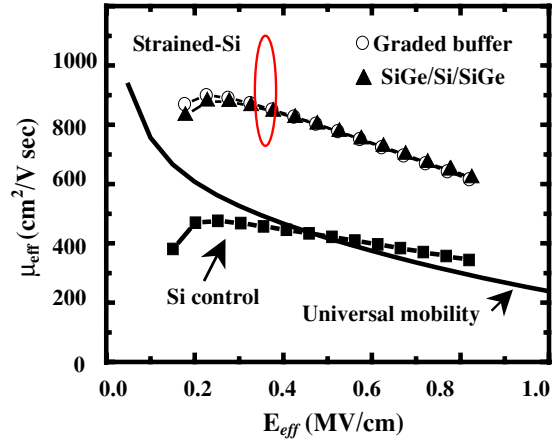
Figure 10. Effective electron mobility of strained Si *n*-MOSFETs with various relaxed SiGe structures as a function of the effective electric field (E_{eff}).

n-MOSFET is shown in figure 10. The peak electron mobility for the device with the 800 nm thick $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ structure was found to be 80% higher than that of the Si control device at the effective electric field of 0.8 MV cm^{-1}, and compared favourably with that of the device using the conventional graded buffer layer (81% enhancement). This is due to the preferential occupation of electrons in the lower-energy Δ_2 conduction band valleys with reduced effective mass and higher mobility in strained Si. These results indicate the potential of the $Si_{1-x}Ge_x/Si/Si_{1-x}Ge_x$ multilayer structures to replace the much thicker graded buffer layer for high-speed CMOS in the next generation.

4. Conclusions

A simple method using an intermediate Si layer in a 770 nm thick $Si_{0.8}Ge_{0.2}$ film to grow the relaxed $Si_{0.8}Ge_{0.2}$ epilayer with a low density of dislocation and smooth surface is developed. The HRTEM image shows that the intermediate Si layer with {3 1 1} dislocation loops changes the relaxation mechanism in $Si_{0.8}Ge_{0.2}$ films, acts as an effective nucleation site for misfit dislocations to relax the mismatch strain and suppresses the propagation of TDs. The thickness of the $Si_{0.8}Ge_{0.2}$ underlayer did not influence the TDs density and surface roughness of the top SiGe layers. Using a 50 nm thick Si layer and a 70 nm thick SiGe underlayer, a dramatic decrease in roughness was observed in the surface of the $Si_{0.8}Ge_{0.2}$ layer (3 nm) with the $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ structure. Such a SiGe/Si/SiGe heterostructure has a high degree of strain relaxation up to 97% and a TD density of as low as 8.9 × 10^5 cm^{-2}. Inferior relaxation in the SiGe overlayer was found for the 770 nm thick SiGe films with a thinner (<25 nm) or thicker (>75 nm) inserted Si layer. Under RTA treatment, relaxation in the 210 nm thick SiGe overlayer reaches only 54%, which is limited by its thickness. Thickness of the $Si_{0.8}Ge_{0.2}$ overlayer will influence the final state of strain in the $Si_{0.8}Ge_{0.2}/Si/Si_{0.8}Ge_{0.2}$ structure. Effective electron mobility for the strained Si device was found to be 80% higher than that of the Si control device. This method suggests a useful way to fabricate high-quality relaxed epilayers with large lattice mismatch.

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