The Effect of Patterned Susceptor on the Thickness Uniformity of Rapid Thermal Oxides

Kuo-Chung Lee, Hong-Yuan Chang, Hong Chang, Jenn-Gwo Hwu and Tzong-Shyan Wung

***Abstract*— A temperature compensation concept suitable for rapid thermal processing (RTP) with a nonuniform wafer temperature distribution is proposed in this work. Concentric Si rings with different diameters are placed on planar quartz or Si susceptors and are regarded as patterned susceptors for temperature compensation. We put monitor wafers on the patterned susceptor and see the effect of the patterned susceptor on the oxide thickness uniformity of the monitor wafers. The Si rings work as radiation barriers when placed on the quartz susceptor, but as heat conduction media when placed on the Si susceptor. By properly arranging the Si rings on the planar susceptors, the monitor wafers' oxide thickness uniformity can be improved.**

***Index Terms*— Oxide uniformity, patterned susceptor, RTO, RTP.**

I. Introduction

As device dimension shrinks to the submicrometer range, reduction of thermal budget during microelectronic processing is becoming a crucial issue. In order to develop ultra large-scaled integrated (ULSI) circuit technology, rapid thermal processing (RTP) is becoming a more and more important technology. The short time at high temperature afforded by the RTP system is desired for minimizing dopant redistribution. RTP also has the advantage of single-wafer processing. However, wafers' temperature nonuniformity is indeed a critical issue for RTP which will thus induce problems associated with thermoplastic stress, such as wafer warpage and slip dislocation. Therefore, considerable efforts have been undertaken to improve the wafers' temperature uniformity. These efforts include the considerations of the lamp number and location [1]–[3], patterned reflectors [4], [5], individually adjusting the electrical power applied to each lamp [6], [7], system geometry [8], [9], and patterned wafers [10], [11].

Temperature uniformity is also affected by the radiation properties of the wafers' pattern, film thickness, and surface roughness [5], [11]. The specific geometry of the patterns and film thickness will affect the wafer's own processing uniformity. Even if one has the reactor perfectly tuned for a nonpatterned test wafer, the temperature nonuniformity may be unacceptable for the patterned product wafer if the pattern size is sufficiently large (>5 mm) [12].

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K.-C. Lee, H.-Y. Chang, H. Chang, and J.-G. Hwu are with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. (e-mail: hwu@cc.ee.ntu.edu.tw).

T.-S. Wung is with the Institute of Applied Mechanics, National Taiwan University, Taipei, Taiwan, R.O.C.

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From the above point of view, the pattern effect is severe for RTP systems. However, one can also utilize pattern effects to make the semiconductor wafers have more uniform temperature distribution in a nonuniform temperature RTP system. In this work, we present a temperature compensation method to improve the oxide thickness uniformity in an RTP system. Concentric Si rings with different diameters are placed between the monitor wafers and the planar susceptors. The Si rings and the planar susceptors are regarded as patterned susceptors for temperature compensation. By properly arranging the Si rings on the planar susceptors, the monitor wafers' oxide thickness uniformity can be improved. The temperature compensation method proposed in this work is useful in solving the temperature nonuniformity problem in the RTP system.

II. Experimental

P-type (1 0 0) 3-in Si wafers with a resistivity of 1–10 Ω-cm were used as the monitor wafers. Concentric Si rings were fabricated by chemical wet etching of 4-in Si wafers. Each Si ring is 3.4 mm in width and 300 μm in thickness. The distance between adjacent rings is 1.4 mm. The Si rings, placed on the planar quartz or Si susceptor, are used as temperature compensation means to get uniform temperature distribution on the monitor wafers. Fig. 1 shows the construction of the RTP system. A water-cooled metal tube surrounds the processing quartz chamber. In addition, there is a nitrogen gas cooling metal sheath coupling to a steel tank. Mass flow controllers are used to control the flow rates of the activation gases fed into the chamber. Eight halogen lamps with reflectors were arranged above the quartz chamber. The power of the halogen lamps is feedback-controlled through the thermocouple. We put a piece of Si on the thermocouple to measure the effective temperature of the monitor wafer. Fig. 2 shows the set up of the patterned susceptor with the denoted number of each of the 3.4-mm Si rings. The monitor wafers with different combinations of Si rings as patterned susceptors are oxidized in the RTP system. The oxidation condition is 960 °C, 500 torr in pure O_2 without wafer rotation. The oxide thickness of the processed wafers is measured by ellipsometry using a refractive index of 1.46.

III. Results and Discussion

A. Oxide Thickness Distribution with Planar Susceptors

Fig. 3(a)–(c) shows the oxide thickness distribution of monitor wafers on planar quartz susceptor, three-quartz-pins sus-

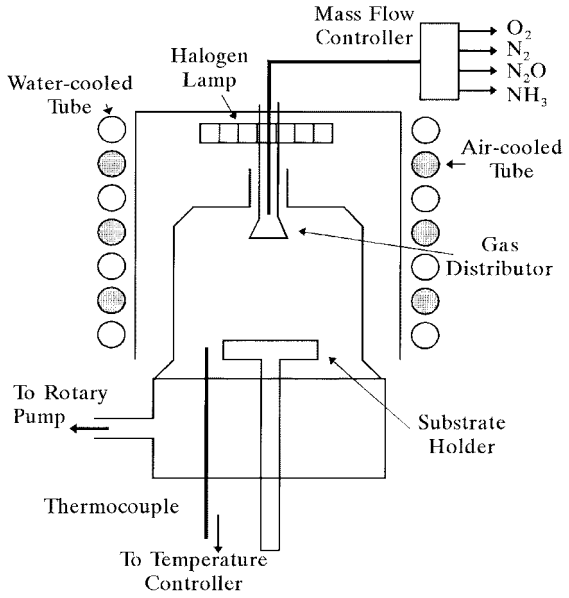


Fig. 1. Construction of the RTP system.

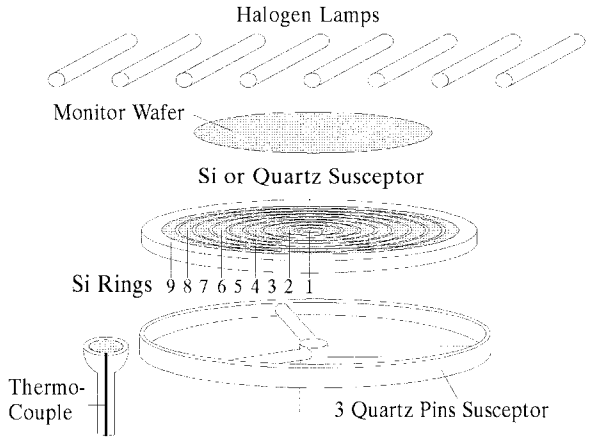


Fig. 2. Setup of the patterned susceptor.

ceptor, and planar Si susceptors, respectively. The inserted figures show the set up configurations and the oxide thickness distribution profiles. In these figures, one can see that the monitor wafer on the planar quartz susceptor has the largest oxide thickness variation. The monitor wafer on the planar Si susceptor has the smallest oxide thickness variation. From the thickness distribution profile of the monitor wafer on the three-quartz-pins susceptor, we find that there are three lower channels from the center to the edge. This is mainly due to the three contacts between the three quartz pins and the monitor wafer. Fig. 4 shows the oxide thickness at the center of the wafer versus oxidation time for monitor wafers on the three different susceptors as described above. From Fig. 4, one can see that the monitor wafer on the planar Si susceptor has the thickest oxide thickness in the center. The monitor wafer on the three-quartz-pins susceptor has the thinnest oxide thickness in the center. The reason is described below. For the three-quartz-pins susceptor, there is more heat loss (radiation and convection) from the backside of the monitor wafer than the other susceptors. Therefore, the oxide thickness in the

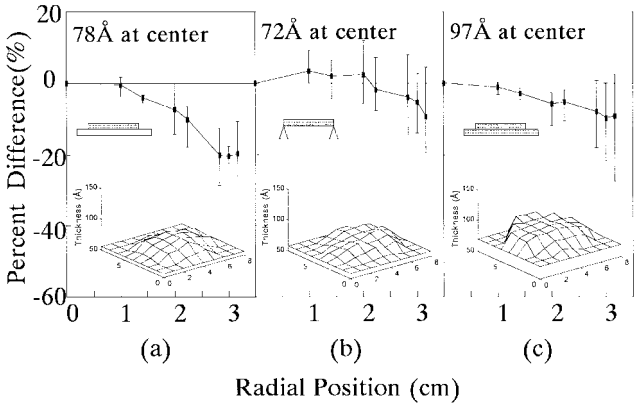


Fig. 3. Oxide thickness distribution for 30 s RTO of monitor wafers on (a) planar quartz susceptor, (b) three-quartz-pins susceptor, and (c) planar Si susceptor.

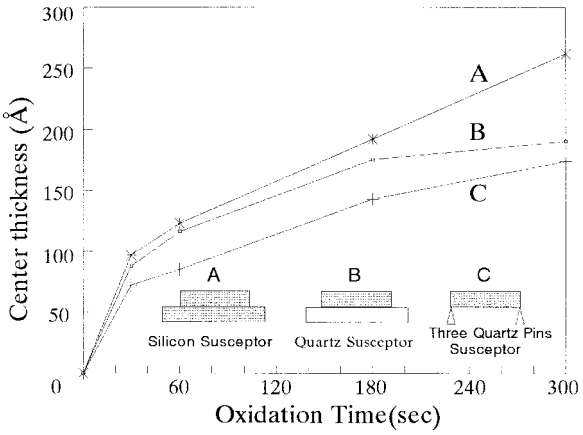


Fig. 4. Centric oxide thickness versus oxidation time for monitor wafers on different susceptors.

center of monitor wafer on the three-quartz-pins susceptor is the thinnest. For the planar quartz susceptor, since the planar quartz susceptor is a poor thermal conductor and will block the convection loss from the backside of the monitor wafer, the center oxide is thicker than that of the three-quartz-pins susceptor. As for the planar Si susceptor, since Si is nearly opaque to the heat radiation for temperature above 600 °C [13], the planar Si susceptor will block the radiation loss in addition to the convection loss of heat from the back surface of the monitor wafer. Therefore, the oxide at the center of the monitor wafer on the planar Si susceptor is the thickest. In addition, since the planar Si susceptor is a good heat conductor, the oxide thickness distribution is more uniform than the others.

B. The Insertion of Si Rings as Patterned Susceptors for Temperature Compensation

Fig. 5 shows the oxide thickness distributions of monitor wafers on the planar quartz susceptor with insertions of (a) no Si ring, (b) Si rings 1, 3, and 4, and (c) Si rings 5, 6, and 7. As shown in Fig. 5(b), since the Si rings will block the radiation loss from the center part of the monitor wafer's back surface, the centric oxide thickness is thicker than at

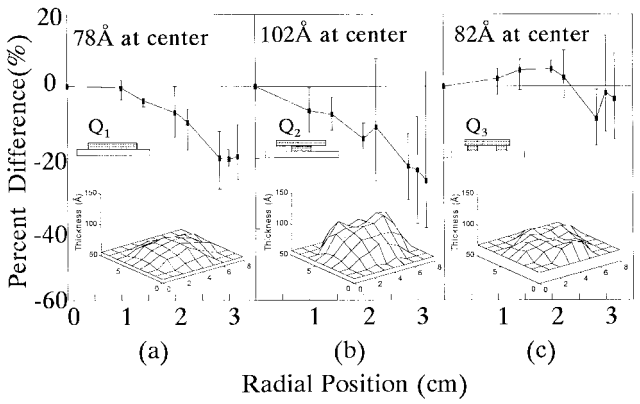


Fig. 5. Oxide thickness distribution for 30 s RTO of monitor wafers on the planar quartz susceptor with insertions of (a) no Si ring, (b) Si rings 1, 3, and 4, and (c) Si rings 5, 6, and 7.

the edge. As for the monitor wafer on Si rings 5, 6, and 7 as shown in Fig. 5(c), one can find that the center oxide is not the thickest. The thickest oxide segment appears at the place near Si ring number 5. This is because the heat radiated from that place is blocked by Si rings 5, 6, and 7. The oxide thickness becomes thin at the edge because of the additional heat loss to the ambient. Considering the thickness of the oxide at the center of the wafer, from Fig. 5 one can find that the oxide of the monitor wafer on Si rings 1, 3, and 4 is the thickest because the Si rings 1, 3, and 4 will reduce the radiation loss from the center part of the monitor wafer's back surface. The center oxide thickness of monitor wafer without an Si ring is thinner because it experienced more radiation heat loss through the transparent planar quartz susceptor. Table I shows the detailed experimental data of the monitor wafers on different combinations of Si rings on a planar quartz susceptor. From the data of a planar quartz susceptor in Table I, the deviation of oxide thickness for monitor wafer on Si rings 1, 3, and 4, i.e., sample Q2, is the largest. This is because Si rings reduce the radiation heat loss from the wafer's center and therefore induce a temperature gradient. For the monitor wafer on Si rings 5, 6, and 7, i.e., sample Q3, although the monitor wafer edge loses heat to the cold-wall ambient, it experienced less radiation loss from the edge's back surface. From the experimental result as described above, using Si rings 5, 6, and 7 on the planar quartz as patterned susceptor, the monitor wafer exhibits the best thickness uniformity in this work.

Fig. 6 shows the oxide thickness of monitor wafers on a planar Si susceptor with insertions of (a) no Si ring, (b) Si rings 1, 3, and 4, and (c) Si rings 5, 6, and 7. It is noted that the planar Si susceptor is almost opaque to most of the heat radiation for temperatures above 600 °C, and the convective heat loss from the back surface of the monitor wafer is blocked by the susceptor. By comparing Fig. 6(a) with Fig. 5(a), one can see that the center oxide of monitor wafer on the planar Si susceptor is thicker than that on the planar quartz susceptor. In addition, since the planar Si susceptor is a good heat conductor, heat flow will reduce the monitor wafer's temperature gradient. Thus the oxide thickness for the monitor wafer on the planar Si susceptor should be more uniform than that on the planar quartz susceptor.

As can be seen in Fig. 6(b), since the Si rings work as conduction media to transfer the heat from the monitor wafer to the planar Si susceptor, the monitor wafer's center oxide is thinner than at the edge. Although there are large heat losses from the monitor wafer's edge to the ambient, from the experimental result one can see that the heat conduction effect at the center is larger than the heat loss at the edge. Because we did not use Si ring 2 in Fig. 6(b), the monitor wafer's oxide thickness above the segment of Si ring 2 is thicker than the surrounding area. We can predict that if we insert Si ring 2, the oxide thickness above that segment will be similar to the nearby area.

As shown in Fig. 6(c), for the monitor wafer on the Si susceptor with insertion of Si rings 5, 6, and 7, part of the heat at the center and the edge of the monitor wafer will be transferred to the Si susceptor through Si rings 5, 6, and 7. In addition, since the periphery of the planar Si susceptor is also heated by the halogen lamps, part of the heat in that area will also be transferred to the monitor wafer's edge by conduction or radiation. These mechanisms make the monitor wafer with Si rings 5, 6, and 7 have the best oxide thickness uniformity among the three samples. The oxide thickness of the monitor wafer without the Si ring is the thinnest because the contact area between the monitor wafer and the planar Si susceptor is the largest. The monitor wafer on Si rings 5, 6, and 7 exhibited the thickest oxide at the center because it loses less heat by conduction. The detailed experimental data of the monitor wafers on different combinations of Si rings on planar Si susceptor are also shown in Table I.

We also examined the combination of Si rings 1, 2, 3, 4, 8, and 9 and the combination of Si rings 5, 6, 7, 8, and 9 on the planar quartz and Si susceptors for temperature compensation. Figs. 7 and 8 show the oxide thickness distributions of monitor wafers for 30-s RTO oxidation on planar quartz and Si susceptors, respectively, with insertions of (a) no Si ring, (b) Si rings 1, 2, 3, 4, 8, and 9, and (c) Si rings 5, 6, 7, 8, 9. The detailed experimental data are also shown in Table I. When comparing Fig. 5(c) with Fig. 7(c), the latter's edge oxide is thicker than the center oxide. This is because of Si rings 8 and 9, which block radiation loss from the monitor wafer's edge back surface. When comparing Fig. 6(b) with Fig. 8(b), the edge oxide in the former is much thicker than the center oxide. This may be due to the multiple light reflections between the Si susceptor and the wafer edge. As for Fig. 8(b), the insertion of Si rings 8 and 9 will block the multiple light reflections between the Si susceptor and the wafer edge. Si rings 8 and 9 will also conduct some heat from the monitor wafer to the Si susceptor. Therefore, in Fig. 8(b), the edge oxide is not much thicker than the center oxide, and the oxide thickness distribution is more uniform.

From this discussion, one can find a way to improve the oxide thickness uniformity by inserting Si rings. When using planar quartz as the susceptor, radiation loss will dominate the temperature distribution. The insertion of Si rings will block the radiation heat loss from the wafer back surface, and therefore the wafer's temperature will be increased. When using planar Si as the susceptor, conduction heat loss will dominate the temperature distribution. The insertion of Si

TABLE I
EXPERIMENTAL DATA USING 3.4 mm WIDTH Si RINGS, 960 °C, 500 torr

No.	Susceptor	Silicon Ring No.	t (s)	Centric T_{ox} (Å)	Average($\overline{T_{ox}}$) (Å)	STDEV(S) (Å)	$S/\overline{T_{ox}}$ (%)
Q1	Quartz	none	30	78	68.57	6.549	9.55
Q2	Quartz	1,3,4	30	102	85.54	14.019	16.39
Q3	Quartz	5,6,7	30	82	81.36	6.16	7.57
Q4	Quartz	1,2,3,4,8,9	30	113	98.84	16.164	16.35
Q5	Quartz	5,6,7,8,9	30	85	89.9	5.242	5.83
S1	Silicon	none	30	97	90.79	6.517	7.17
S2	Silicon	1,3,4	30	115	122.67	6.817	5.56
S3	Silicon	5,6,7	30	137	132.98	5.973	4.49
S4	Silicon	1,2,3,4,8,9	30	127	131.35	4.38	3.33
S5	Silicon	5,6,7,8,9	30	142	133.24	7.297	5.48

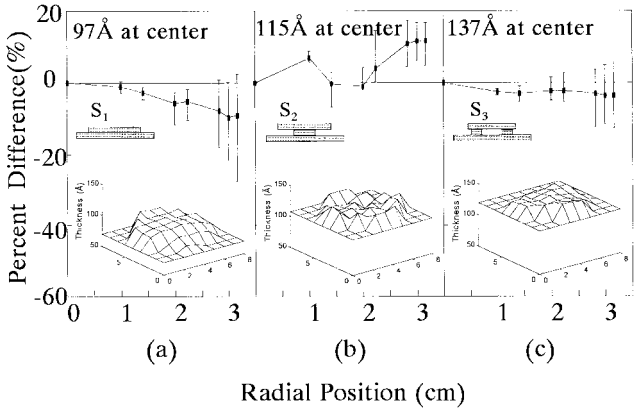


Fig. 6. Oxide thickness distribution for 30 s RTO of monitor wafers on the planar Si susceptor with insertions of (a) no Si ring, (b) Si rings 1, 3, and 4, and (c) Si rings 5, 6, and 7.

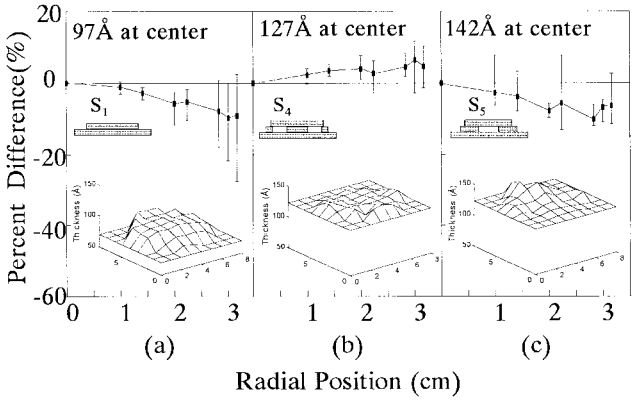


Fig. 8. Oxide thickness distribution for 30 s RTO of monitor wafers on the planar Si susceptor with insertions of (a) no Si ring, (b) Si rings 1, 2, 3, 4, 8, and 9, and (c) Si rings 5, 6, 7, 8, and 9.

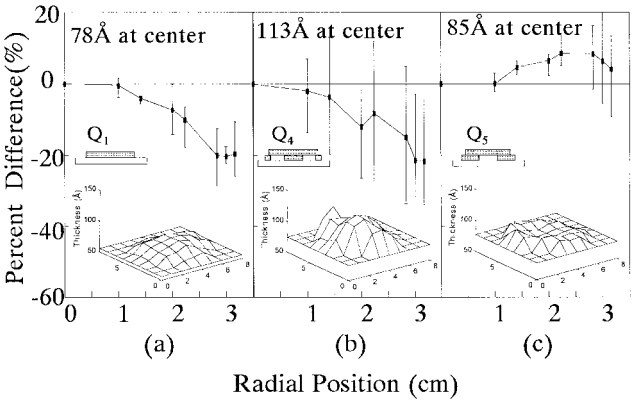


Fig. 7. Oxide thickness distribution for 30 s RTO of monitor wafers on the planar quartz susceptor with insertions of (a) no Si ring, (b) Si rings 1, 2, 3, 4, 8, and 9, and (c) Si rings 5, 6, 7, 8, and 9.

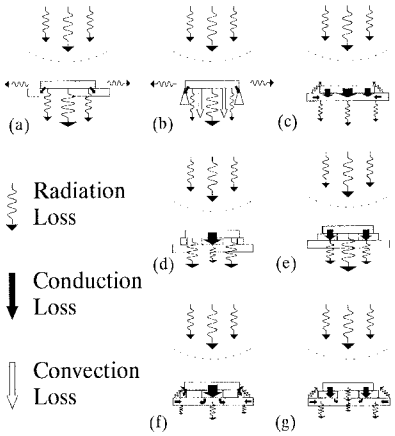


Fig. 9. Representative model of heat flows for monitor wafers on (a) a quartz susceptor, (b) a three-quartz-pins susceptor, (c) an Si susceptor, (d) a quartz susceptor with Si rings 1, 2, 3, 4, 8, and 9, (e) a quartz susceptor with Si rings 5, 6, 7, 8, and 9, (f) an Si susceptor with Si rings 1, 2, 3, 4, 8, and 9, and (g) an Si susceptor with Si rings 5, 6, 7, 8, and 9.

rings will conduct more heat from the back surface to the Si susceptor. Therefore the wafer temperature will be decreased.

Fig. 9(a)–(g) shows the representative mechanisms of heat flow for monitor wafers on different susceptors that correspond to Figs. 3(a)–(c), 7(b) and (c), and 8(b) and (c), respectively. In Fig. 9, the width and length of the arrows represent the amount of heat flows. From Fig. 9, one can expect that proper insertions of Si rings can redistribute the temperature on the Si wafer via various heat transfer paths and make the Si wafers have more uniform oxide thickness distributions.

IV. Conclusion

A temperature compensation method using separated Si rings as a patterned susceptor to improve the oxide thickness uniformity in a nonuniform temperature RTP system is proposed in this work. The action of Si rings is different for different susceptors. In a transparent susceptor with poor thermal conductivity such as a planar quartz susceptor, Si rings work as radiation barriers to prevent heat radiation loss through the quartz susceptor. In a good thermal conductivity susceptor such as Si, Si rings work as conductive media to transfer heat from the monitor wafer to the Si susceptor. It is believed that the method of using separated Si rings as a patterned susceptor can add flexibility and effectively improve the thickness uniformity of oxides in RTP systems.

References

[1] J. M. Dilhac, N. Nolhier, and C. Ganibal, "Thermal modeling of a wafer in a rapid thermal processor," *IEEE Trans. Semiconduct. Manufact.*, vol. 8, pp. 432–439, Nov. 1995.

[2] R. Henda, E. Scheid, and D. Bielle-Daspet, "A 3-dimensional thermal processing furnace," *Mat. Res. Soc. Proc.*, vol. 342, pp. 419–424, 1994.

[3] F. Y. Sorrell, M. J. Fordham, M. C. Ozturk, and J. J. Wortaman, "Temperature uniformity in RTP furnace," *IEEE Trans. Electron Devices*, vol. 39, pp. 75–80, Jan. 1992.

[4] G. L. Young and K. A. McDonald, "Effect of radiation shield angle on temperature and stress profiles during rapid thermal annealing," *IEEE Trans. Semiconduct. Manufact.*, vol. 3, pp. 176–182, 1990.

[5] J. P. Hebb, K. F. Jensen, and E. W. Egan, "The potential effect of multilayer patterns on temperature uniformity during rapid thermal processing," *Mat. Res. Soc. Symp. Proc.*, vol. 387, pp. 21–27, 1995.

[6] K. L. Knutson, S. A. Campbell, and F. Dunn, "Modeling of three-dimensional effects on temperature uniformity in rapid thermal processing of eight inch wafer," *IEEE Trans. Semiconduct. Manufact.*, vol. 7, pp. 68–72, Feb. 1994.

[7] A. Tillmann, "Optimization of process parameter and temperature uniformity of wafers for rapid thermal processing," *Mat. Res. Soc. Symp. Proc.*, vol. 387, pp. 3–14, 1995.

[8] B. J. Cho, P. Vandenabeele, and K. Maex, "Development of a hexagonal-shaped rapid thermal processor using a vertical tube," *IEEE Trans. Semiconduct. Manufact.*, vol. 7, pp. 345–353, Aug. 1994.

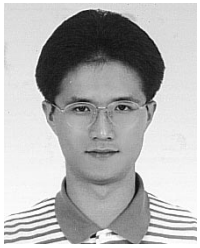
[9] Y. T. Lin, R. Subrahmanyan, A. R. Sitaram, and M. Orlowski, "Combined simulation and measurement study of temperature uniformity in rapid thermal processing," *Mat. Res. Soc. Symp. Proc.*, vol. 303, pp. 231–236, 1993.

[10] P. Y. Wong and I. N. Miaoulis "Thermal radiation absorption characteristics of patterned wafers during rapid thermal processing," *Mat. Res. Soc. Symp. Proc.*, vol. 342, pp. 395–400, 1994.

[11] P. Y. Wong, I. N. Miaoulis, and C. G. Madras, "Transient and spatial radiative properties of patterned wafers during thermal processing," *Mat. Res. Soc. Symp. Proc.*, vol. 387, pp. 15–20, 1995.

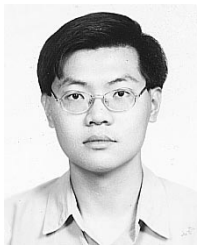
[12] P. Spence, C. Schaper, and A. Kermani, "Concurrent design of an RTP chamber and advanced control system," *Mat. Res. Soc. Symp. Proc.*, vol. 387, pp. 75–86, 1995.

[13] T. Sato, "Spectral emissivity of silicon," *Jpn. J. Appl. Phys.*, vol. 6, no. 3, p. 339, 1967.



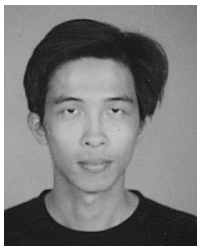
Kuo-Chung Lee was born in Taiwan, R.O.C., on May 24, 1969. He received the B.S. degree in electro-physics from National Chiao-Tung University, Hsinchu, Taiwan, in 1991, and the M.S. and Ph.D. degrees in electrical engineering from National Taiwan University, Taipei, in 1993 and 1998, respectively. The title of his doctoral thesis was "Temperature Compensation Techniques for High Temperature Rapid Thermal Processor and Fabrication of Si Opto-Electronic Devices Utilizing Room Temperature Processes."

Currently, he is serving in the Academia Sinica of the Republic of China.



Hong-Yuan Chang was born in Taiwan, R.O.C., in 1973. He received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, in 1995 and 1997, respectively. The title of his master's thesis was "The Effect of Susceptor on the Thickness Uniformity and Electrical Characteristics of Rapid Thermal Oxides."

Currently, he is serving in the Republic of China Army as a Second Lieutenant.



Hong Chang was born in Taiwan, R.O.C., in 1974. He received the B.S. degree in electro-physics from National Chiao-Tung University, Hsinchu, Taiwan, in 1996 and the M.S. degree in electrical engineering from National Taiwan University, Taipei, in 1998. The title of his master's thesis was "Study of the Thermal Analysis and the Improvement in Thickness Uniformity of Rapid Thermal Oxides."

Currently, he is serving in the Republic of China Army as a Second Lieutenant.

Jenn-Gwo Hwu was born in Taiwan, R.O.C., on August 29, 1955. He received the B.S. degree in electronic engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1977 and the M.S. and Ph.D. degrees in electrical engineering from National Taiwan University (NTU), Taipei, in 1979 and 1985, respectively.

Presently, he is a Professor in the Department of Electrical Engineering, NTU. He joined the NTU faculty in 1981. His research work is mainly concerned with the characterization of MOS devices, especially the thin gate oxide growth technique and the radiation effect. He has experience in teaching courses in circuits, electronics, solid-state electronics, semiconductor engineering, and MOS capacitor devices.

Dr. Hwu was the recipient of the 1986 Excellent Teaching Award sponsored by the College of Engineering, National Taiwan University. In 1988, 1989, 1990, 1991, and 1993, he was a nominee for the above award. In 1991, he was also the recipient of the Outstanding Teaching Award sponsored by the Ministry of Education, Republic of China. In 1999, he was the recipient of the Excellent Teaching Award sponsored by the College of Electrical Engineering, NTU.

Tzong-Shyan Wung received the M.S. degree in power mechanical engineering from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 1976. He received the Ph.D. degree in 1986 from the Department of Mechanical Engineering, University of Iowa, Iowa City.

He worked with Chung Shan Institute of Science and Technology for four years in the field of thermal design and temperature control of electronic instruments. He has been with the Institute of Applied Mechanics, National Taiwan University, Taipei, since 1986. His current research subjects are numerical simulation of rapid thermal processor, flow visualization of micro jets, and micro misty cooling using direct imaging techniques.