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# Accumulation-Type vs. Inversion-Type of an Ultra-Thin SOI PMOS Device Operating at $300K$ and $77K$: Subthreshold Behavior and Pull-up Switching Performance of a CMOS Inverter

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**Abstract**

This paper presents two-dimensional simulation study on the accumulation-type vs. the inversion-type of an ultra-thin SOI PMOS device operating at $300K$ and $77K$ in terms of its subthreshold behavior and pull-up switching performance of a CMOS inverter, using low-temperature PISCES [1].

**Summary**

**Ultra**-thin SOI MOS devices have advantages in high speed, reduced second order effects, which are attractive for deep submicron CMOS VLSI. For ultra-thin SOI structures, enhancement-type PMOS devices may be difficult to build using an n-type ultra-thin film with an N+ polysilicon gate. An accumulation-type SOI PMOS device using a p-type ultra-thin film and an N+ polysilicon gate has been introduced to produce an enhancement-type PMOS device [2]. Recently, the subthreshold behavior and the switching performance in an ultra-thin SOI CMOS inverter using inversion-type CMOS devices operating at liquid nitrogen temperature have been reported [3]. This paper reports the accumulation-type vs. the inversion-type of an ultra-thin SOI PMOS device operating at $300K$ and $77K$ in terms of its subthreshold behavior and pull-up switching performance in an ultra-thin SOI CMOS inverter using the inversion-type and the accumulation-type PMOS devices.

**Fig. 1** shows the cross section of the SOI CMOS device structure using a SIMOX process [4] under study. The ultra-thin SOI CMOS devices using an $N+$ polysilicon gate, have a front gate oxide of $200\,\mathring{A}$, a channel length of $1\mu m$, a thin silicon film of $1000\,\mathring{A}$, and an insulator of $3500\,\mathring{A}$. In the NMOS device, a p-type thin film with a doping density of $5 \times 10^{16} cm^{-3}$ has been used. For the ultra-thin SOI structures, enhancement-type PMOS devices may be difficult to build using an n-type ultra-thin film with an N+ polysilicon gate. An accumulation-type SOI PMOS device using a p-type ultra-thin film and an N+ polysilicon gate has been introduced to produce an enhancement-type PMOS device [2]. Here, as shown in Figs. 1(a)&(b), both the inversion-type and the accumulation-type PMOS devices have been studied. Fig. 2 shows the subthreshold characteristics of the SOI inversion-type and accumulation-type PMOS devices biased at $V_{DS} = -0.1V$, operating at $300K$ and $77K$ using low-temperature PISCES [1]. As shown in Fig. 2, at $77K$, the accumulation-type PMOS device demonstrates a unique "delayed-turn-on" behavior. Generally speaking, the subthreshold slope of the SOI inversion-type PMOS device at $77K$ improves about 4 times as compared to the $300K$ operation as a result of the change in the thermal voltage. As for the accumulation-type SOI PMOS device, at $77K$, its subthreshold slope is much worse as a result of the freezeout phenomenon in the thin film at low temperature. Fig. 3 shows the hole concentration distribution in the center of the PMOS devices biased in the subthreshold region at a drain current level of $0.1\mu A/\mu m$ at $300K$ and $77K$. In the inversion-type PMOS

device, no obvious hole pile-up at the back surface can be identified in the subthreshold region – the current conduction is always through the front channel. As for the accumulation-type PMOS device, at a current density level of $0.1\mu A/\mu m$, a buried channel exists for both the $300K$ and $77K$ operations. As shown in Figs. 1(a)&(b), in order to facilitate transient analysis, two CMOS inverter structures using the NMOS device and the inversion-type and the accumulation-type PMOS devices have been used. In each inverter structure, NMOS and PMOS devices are placed against each other separated by an oxide layer of $5000\mathring{A}$ [3]. An output capacitive load of $10fF/\mu m$ is placed. Low-temperature PISCES has been used in the transient analysis [1]. By imposing an input step from $5V$ to $0V$ in $10ps$ at the input, pull-up transient analysis of the SOI CMOS inverter structure has been obtained.

Figs. 4 show the hole concentration distributions in the inversion-type and accumulation-type PMOS devices of the corresponding SOI CMOS inverters operating at $300K$ and $77K$ at $0ps$, $10ps$, and $80ps$ during the pull-up transient. Initially, in the accumulation-type PMOS device, for both the $300K$ and $77K$ operations, substantial holes already exist at the back surface. On the other hand, in the inversion-type PMOS device at $300K$, electrons exist at the front interface. At $10ps$, the hole density at the front interface already exceeds $10^{18}cm^{-3}$ in both devices at $300K$ and $77K$. In the whole thin film, the hole density is higher than its neutral value in both devices at $300K$ and $77K$. At the back interface, substantial hole pile-up can be identified for all cases. At $80ps$, both PMOS devices are fully turned on. The difference in the hole density at the front interface among all cases is small. The difference in the hole density in the center portion of the thin film in both devices at $300K$ and $77K$ is mainly due to the difference in the doping density in both devices and the incomplete ionization effect at $77K$.

Fig. 5 shows the output voltage of the SOI CMOS inverter using the inversion-type and accumulation-type PMOS devices during the pull-up transient. During the initial $10ps$, the output voltage shows an undershoot below $0V$ [3]. After the initial $10ps$, the $77K$ cases demonstrate much faster pull-up transients. The reduction in rise time of the accumulation-type case at $300K$ is mainly due to a smaller absolute value in the threshold voltage of the accumulation-type PMOS device. On the other hand, at $77K$, the rise time of the CMOS inverter using the inversion-type PMOS device reduces about one half as compared to the $300K$ case. The rise time of the accumulation-type case at $77K$ shrinks only by one third. The more improvement of the rise time for the inversion-type case at $77K$ is attributed to the much larger effective hole mobility in the inversion-type PMOS device as a result of the less heavily doped thin film.

### References


[1]J. Kuo et.al., *IEEE TED*, 2/92

[2]J. Colinge, *IEEE TED*, 3/90

[3] J. Kuo, *IEEE TED*, 12/92

[4] T.MacElwee, et.al., " *IEEE TED* 6/90

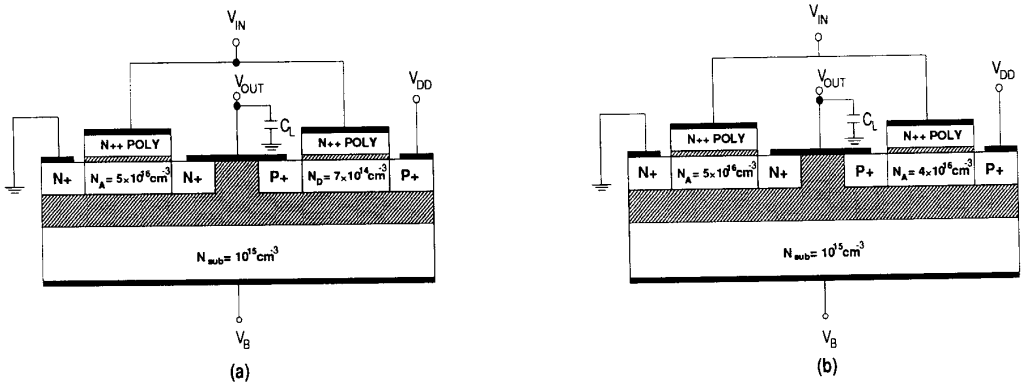


Fig. 1 The SOI CMOS Inverter structure under study. (a) with inversion-type PMOS device. (b) with accumulation-type PMOS device.

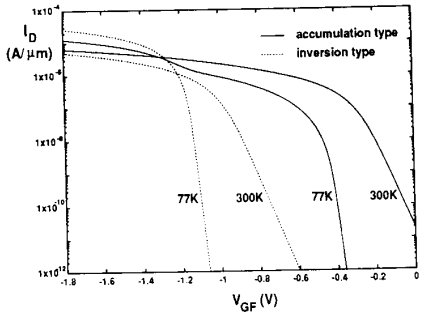


Fig. 2 The subthreshold characteristics of the SOI inversion-type and accumulation-type PMOS devices.

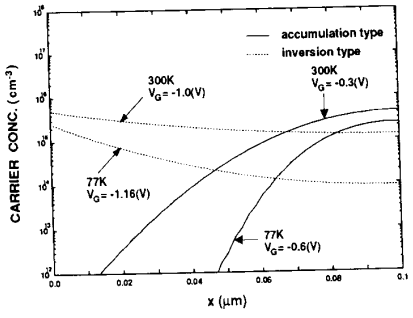


Fig. 3 The hole concentration distribution in the center of the PMOS devices biased in the subthreshold region at a drain current level of $0.1\mu A/\mu m$ at $300K$ and $77K$.

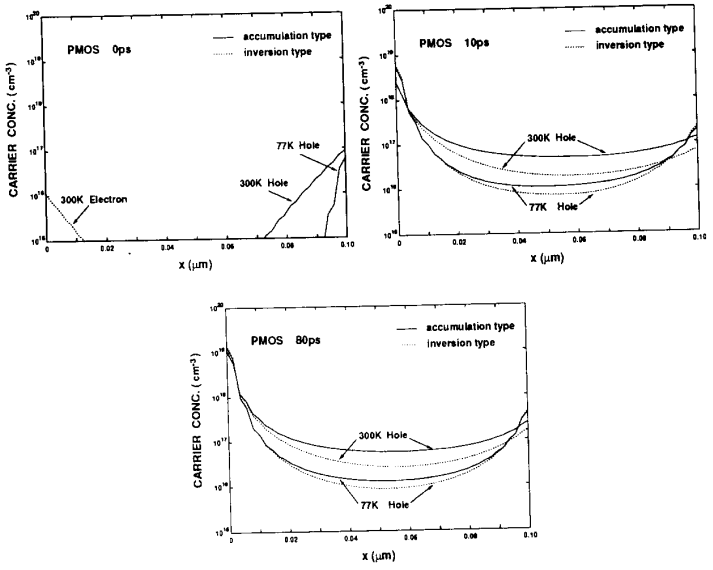


Fig. 4 The hole concentration distributions in the center of the inversion-type and accumulation-type PMOS devices at $0ps$, $10ps$, and $80ps$ during the pull-up transient.

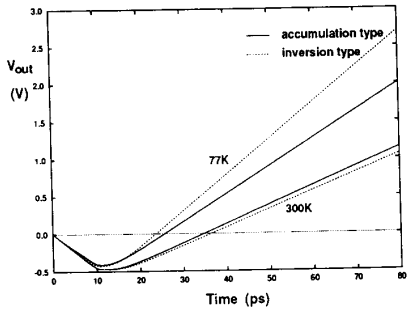


Fig. 5 The output voltage of the SOI CMOS inverter using inversion-type and accumulation-type PMOS device operating at $300K$ and $77K$ during the pull-up transient.