only an approximation to the true d_{33} value:

$$d_{33} = \frac{\partial D_3}{\partial T_3} \qquad (2)$$

where T_3 is the normal stress in a point of the film surface, D_3 is the electric displacement and the boundary conditions imply that no clamping of the film is assumed: the film is free to expand along directions 1 and 2 (in contrast to the definition of d_{33}^*, where the impinging probe may be responsible for some clamping effects).

In spite of being just an approximation to d_{33}, d_{33}^* is often used in order that the apparatus used for making the measurement can be simplified. For planar films, a non-metallised piezoelectric film is sandwiched between an aluminum plate, acting as the ground reference, and a flat impinging metallic probe forming the second electrode needed for the measurement. By connecting the two electrodes to a charge amplifer, ΔQ can be measured. The force convertor ΔF exerted on the polymer film is usually measured by a load cell, incorporated in the impinging probe.

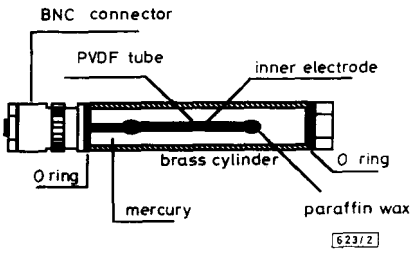

Fig. 2 *Schematic view of measuring apparatus*

Description of measurement cell: To implement the described measurement technique on tubular devices, we have designed an *ad hoc* measuring apparatus, see Fig. 2. The chamber is formed by a hollow brass cylinder, threaded at both its ends; one end is capped with a BNC connector (Amphenol RG 178), endowed with a metallic needle soldered to its hot lead. At the other end the cylinder can be connected to a simple pneumatic circuit consisting of a compressor capable of injecting air into it; a manometer measures the air pressure in the circuit. Before screwing the BNC connector to the cylinder, the tubular device to be measured is snugly fitted into the needle; small pieces of an insulating material such as paraffin wax are then spread over that metallic part of the needle which remains exposed. After the BNC connector has been placed *in situ*, the hollow cylinder is filled with mercury and then vertically positioned by means of a suitable support: note that the shield of the BNC connector is connected to the outer liquid electrode through the brass cylinder itself. Provided that any short-circuit condition between the two electrodes has been avoided by the wax covering, the pneumatic circuit is connected to the cylinder by means of its threaded end. For the pressures p of interest to our application, ranging between 0.5 and 5atm, the mercury leakage is easily prevented by placing two O rings at both threaded ends. Finally, a coaxial cable allows us to connect the measuring chamber to a charge amplifer (Kystler Type 5011). The measurement is made when the mercury is pressurised within the cylinder; given that the length of the tubular device portion exposed to the liquid mercury is L, and the outer diameter of the tubular device is Φ, we obtain:

$$d_{33}^* = \frac{\Delta Q}{\pi \Phi L p} \qquad (3)$$

Experiment: The preparation of an electrically active piezoelectric device made from PVDF is quite complex. Starting from an extruded tube of PVDF (SOLEF X10N, Solvay, Brussels, Belgium), the stretching phase of the material processing consists of stretching the material at 110°C (drawing ratio 1:3.5). The material is then subjected to a thermal annealing, a procedure of maintaining the sample clamped at constant tension for a while (3h at 110°C), in order to heal the damage induced in the material by the stretching phase. After stretching, the tubular device, presenting an outer diameter Φ = 0.9mm, is submitted to the corona poling procedure for making it piezoelectrically active. An array of regularly spaced needle electrodes is circumferentially arranged around the cylindrical surface of the tube at a distance of d = 2 mm from it. A brass wire fitted into the lumen of the tube is used as an inner electrode. A high intensity electric field (15–20kV) is applied to the sample for ~12h. After poling, the PVDF tubular device is placed in the measuring chamber for performing the d_{33}^* measurement. We have obtained d_{33}^* values from –6 to –10pC/N (values for piezoelectric films of PVDF manufactured by Solvay are d_{33}^* = –13.5pC/N [5]); inert devices, that is devices not subjected to the poling procedure, were unable to elicit any significant readings from the charge amplifier at any pressure.

Conclusions: The measuring technique described in this Letter represents an inexepensive means for evaluating the piezoelectric constant d_{33}^* of tubular devices. The proposed measuring technique allows us to select batches of devices with similar electrical characteristics. It should be pointed out that:

(i) it is difficult to compare the results of our measurements to the figures currently given for commercially available films, because they are subjected to a mechanical/thermal process quite different from the process to which we subject our devices

(ii) our home-made procedure of preparing samples is unable to provide a degree of uniformity and reproducibility in the electrical properties of the proposed tubular devices comparable to that obtained in films of industrial origin: this might account for the observed spreading in the measured values.

29 September 1993
Electronics Letters Online No: 19931362

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1.5V BiCMOS dynamic multiplier using Wallace tree reduction architecture

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Indexing terms: BiCMOS integrated circuits, Multiplying circuits

A 1.5V BiCMOS dynamic multiplier is presented which is free from race and charge sharing problems, using Wallace tree reduction architecture and a 1.5V full-swing BiCMOS dynamic logic circuit. Based on a 1μm BiCMOS technology, a designed 1.5V 8×8 multiplier shows a ×2.3 improvement in speed as compared to the CMOS static multiplier.

Introduction: High-speed multipliers are usually realised by parallel architectures [1], where a Wallace reduction structure [1] and carry look ahead circuit have been used to enhance the speed performance. In a high-speed parallel multiplier using the Wallace tree reduction structure, the most important building cells are the full adder circuit and the carry look-ahead circuit. Although the CMOS dynamic technique [2] can provide a speed advantage over the static technique for implementing serial adders, it is not

suitable for realising the full adder circuit for parallel multipliers using Wallace tree reduction structure due to race problems [2]. Recently, a 5V BiCMOS dynamic carry look ahead circuit, which is built by cascading BiCMOS dynamic logic gates without race problems, was reported [3, 4]. For a deep sub-half-micrometre BiCMOS technology, a 1.5V supply is necessary [5]. In this Letter, a 1.5V BiCMOS dynamic multiplier using Wallace tree reduction techniques and 1.5V full-swing BiCMOS dynamic logic circuit without race and charge sharing problems is described.

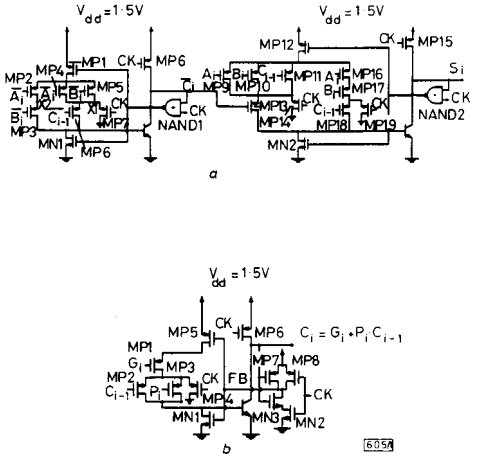

Fig. 1 *1.5V full swing BiCMOS dynamic full adder and carry look-ahead circuit*

a Adder
b Carry look-ahead circuit

1.5V BiCMOS dynamic full-adder and CLA circuit: Fig. 1*a* and *b* show the 1.5V BiCMOS dynamic full adder and CLA circuit. As shown in Fig. 1*b*, the BiCMOS dynamic full adder circuit is composed of two cascaded non-inverting BiCMOS dynamic logic cells [6] for 1.5V operation. The first BiCMOS dynamic logic cell is used to implement the $\overline{carry}$ signal and the second cell is used to realise the *sum* signal. As in a dynamic BiCMOS digital circuit [6], during the precharge period, the clock signal (CK) is low the outputs of two cells are charged to high, and the bipolar devices are turned off by MN1 and MN2. In addition, MP1 and MP2 are off at this time. During the logic evaluation period, the clock signal (CK) is high. During the initial period of the logic evaluation period, MP1 and MP12 are on and MN1 and MN2 are off. If at least any two of the three inputs are low, the $\overline{carry}$ signal is pulled low by the pull-down bipolar transistor. The sum signal will then be pulled down only when all of the three inputs are low or when the $\overline{carry}$ signal is low and at least one of the three inputs is low. Using the non-inverting BiCMOS logic circuits, the full adder can be used in a high-speed parallel multiplier with Wallace reduction structure without race problems. Furthermore, to avoid charge sharing problems [7], MP7, MP14, MP19 have been used. Fig. 1*b* shows the BiCMOS dynamic carry look-ahead circuit. In the carry look-ahead circuit, each bit of the *carry* signal is high if the generated signal is high or if the propagating signal is high and the *carry* signal of the previous bit is high.

BiCMOS dynamic multiplier: BiCMOS dynamic circuits are appropriate for implementing the Wallace tree reduction architecture with complicated wiring. To show the versatility of the BiCMOS dynamic circuit for constructing parallel multipliers with Wallace tree reduction structure, the 8×8 parallel multiplier shown in Fig. 2 was designed. The die area is 3144 μm × 1455 μm. Fig. 3 shows the propagation delay of the critical path against the supply voltage in the 8×8 parallel multiplier using Wallace tree reduction architecture and the 1.5V full-swing BiCMOS dynamic logic circuit. As shown in this Figure, at a power supply voltage of 5V, the speed advantage of the BiCMOS dynamic multiplier compared with CMOS is ×3.67. At a supply of 1.5V, the speed advantage is ×2.26.

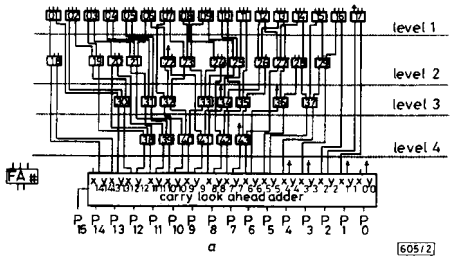

Fig. 2 *Block diagram of 8×8 parallel multiplier and layout of BiCMOS dynamic 8×8 parallel multiplier*

a 8×8 parallel multiplier
b Layout of BiCMOS dynamic 8×8 parallel multiplier; die area is 3144 × 1455μm²

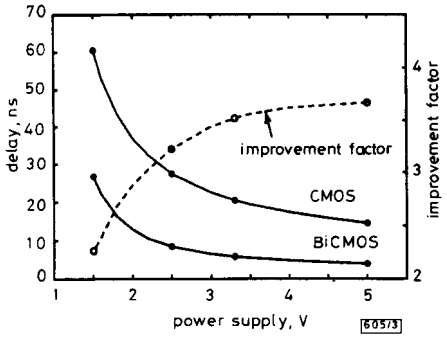

Fig. 3 *Propagation delay of critical path against supply voltage in 8×8 parallel multiplier*

27 September 1993
Electronics Letters Online No: 19931371

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