An 8-bit 2-V 2-mW 0.25-mm^2 CMOS DAC

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ABSTRACT

A low-voltage low-power small area digital-to-analog (DAC) for mixed-signal applications is introduced. A full equally weighted current steering DAC is a performance-efficient architecture for 8-bit resolution, due to almost all the current taken from the supply is used for the output signal. The current steering architecture is also highly suitable for high-speed operation and requires no calibration, trimming, or dynamic averaging. The circuit operates from a 2-V power supply in a standard 0.25um CMOS technology. The measured DNL/INL is 0.23/0.3, and output 200-kHz signal achieves 50 dBc SFDR at 10 MS/s update rate with power dissipation of 2 mW.

1. INTRODUCTION

In the telecommunication systems of today, the interface between the digital signal processing systems and the analog part of the chip has become one of the key building blocks. Current steering DAC architectures are intrinsically fast, cost effective, and have high power efficiency [1][2].

The fastest DAC operates in current steering principle, feeds all the current directly to the output, achieving almost 100% power efficiency. The most straightforward approach is to use the bits of the digital input word to control a set of binary weighted current source. A high-resolution binary weighted current steering DAC suffers from limited matching properties of technologies, large DNL errors, potential non-monotonicity, and non-equal switching time of the different sized currents cause glitches in major code transitions. These glitches cause large spurs in the frequency domain, especially for small signal. Complex trimming circuits are needed to improve the matching [3].

Segmented higher bits with equally weighted and lower bits with binary weighted [4], monotonicity is not guaranteed and suffers from SFDR degrade as bias circuits of the two MSB/LSB arrays are unmatched [5].

In this paper, a full equally weighted current steering DAC is a performance-efficient architecture for 8-bit resolution. Although the resolution of the DAC increases by a single bit, the number of current sources in the current-source array doubles. The area occupied by a single equally current source also doubles because of the random matching constraint. This leads to a four times area increase for the current-source array for each additional bit. This architecture features minimum requirements on matching, and all the glitches are equally proportional to the signal step that becomes part of the signal and causes no distortion. This is a big advantage in the frequency domain and monotonicity is guaranteed.

Section II discusses the circuit design consideration in the full equally weighted current steering DAC. Section III presents results from measurements, and Section IV summarizes the conclusions.

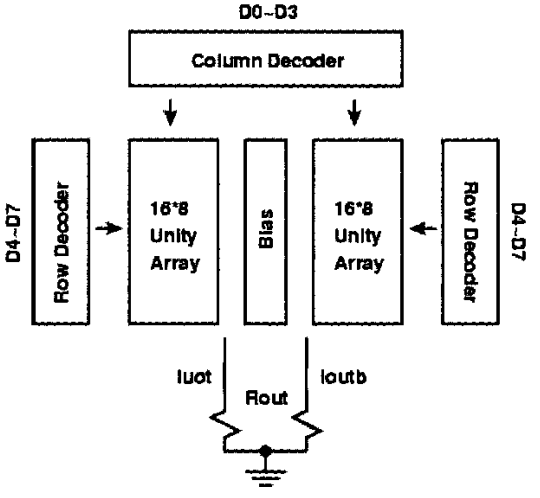

Fig. 1. Block diagram of the DAC.

2. CIRCUIT OPERATION

Shown in Fig.1, the block diagram of the DAC employs full equally weighted current sources.

Three fundamental building blocks, including the decoding latch logic, the switching element and the current source, are required by the DAC, The two-stage decoding logic is implemented with conventional combinational gates optimized for speed and with no pipelining. A key aspect of the performance of the DAC is its extremely small glitch energy. In order to achieve the small glitch energy, a number of problems have been solved:

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1. The imperfect synchronization of the input signals at the gates of the current switches.
2. The digital signal feed through the gate-drain capacitance from the current switches directly to the output.
3. The current variation due to a drain voltage variation of the current sources if both current switches are simultaneously in the off state.
4. The stray capacitance from the drain of the current sources must be small.

The key point to preserve a very high update rate is to keep an intrinsically simple and compact thermometer decoding logic. The best alternative consists of implementing a fast two-stage row-column decoding, symmetrical switching scheme [6]. Unfortunately, this decoder makes it difficult to compensate for systematic errors both in the vertical and horizontal dimensions of the matrix, so that applying the hierarchical symmetrical switching sequence [7][8] to both row and column decoders only compensates the error well in one dimension, while in the other dimension the error is accumulated along the selected line, and in worst case it is multiplied by the number of elements along the dimension. An architecture alternative that overcomes the above using double centroid switching scheme [9][10] that complicates the routing. And this paper uses interleaved column signal in even and odd order, reverse the order of the two row signals, and the bias circuit is inserted in the right/left equally weighted current cell array that surrounds the dummy cell outline.

One stage of latch has been inserted between the peripheral thermometer decoders and the current matrix to suppress the glitch and to enhance the decoding speed. The latch is used to synchronize all DAC cells and to improve the crossing point of the switching control signals, as well. In such a way, switching transistors Ms/Msb in Fig. 2 are never simultaneously in the off state to minimize the recovery time of the node during the switching transition. The current source and the switching elements are basically a differential pair, and design aspect ratio with:

$$(WL)_{min} = \frac{1}{2}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2}\right] \Big/ \left(\frac{\sigma_I}{I}\right)^2 \qquad (1)$$

where A_{VT} and A_β are mismatch technology parameters, $(V_{GS}-V_T)$ is the gate overdrive voltage of the current source transistor and σ_I/I is the relative standard deviation of a unit current source. And the current source transistor has been designed to have a low transconductance in order to enhance the immunity against voltage fluctuation along the ground line, and also, against noise at the node of the primary gate bias voltage.

The influence of the dynamic output impedance in each current cell has been identified as an important limitation for the spurious free dynamic range (SFDR). The relation between this output resistance and the achievable INL specification is given by:

$$INL = \frac{I_{unit} \times R_{out}^2 \times N^2}{4 \times R_{imp}}, \qquad (2)$$

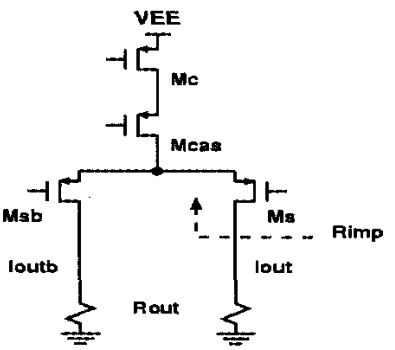

Fig.2 The unit current cell.

where R_{out} is the load resistor and I_{unit} is the LSB current and N is the total number of unit current sources. And for SFDR bandwidth limitation, the required R_{imp} for a given resolution equals [11]:

$$R_{imp,req} = \frac{N \times R_{out}}{4 \times SFDR} \qquad (3)$$

Short channel switch transistors are used to achieve the maximum speed and minimum glitch energy, thus cascode current sources are needed to obtain high output impedance. And the capability of driving low impedance load is embedded in the chip, the unit current is selected as low as 4uA. It is important to keep the voltage in the drain of the cascode current sources as constant as possible during switching. The voltage variation in this node causes the stray capacitance to be charged and discharged which in turn slows down the settling of the output current. The voltage variation is minimized by overlapping the control signals in such a way that their cross point lies slightly below the maximum voltage level.

The clock and input data drivers that are implemented as inverter chains with exponential scaling have been added to the chip, is distributed through a binary tree, to ensure low skew between the different latches.

To attain 8-bit resolution, special attention is paid to the layout design. The unit current sources are distributed in two arrays surrounded by dummy transistors. The systematic error can arise from the voltage drop along the metal ground connections. So the ground lines are made

wide and short to make the voltage drop along them negligible.

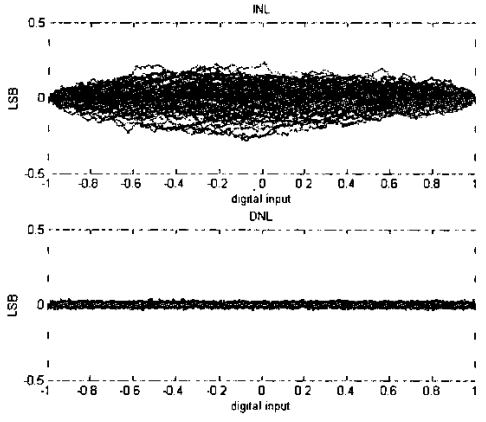

Fig. 3 Matlab 100 simulations DNL/INL profile versus input.

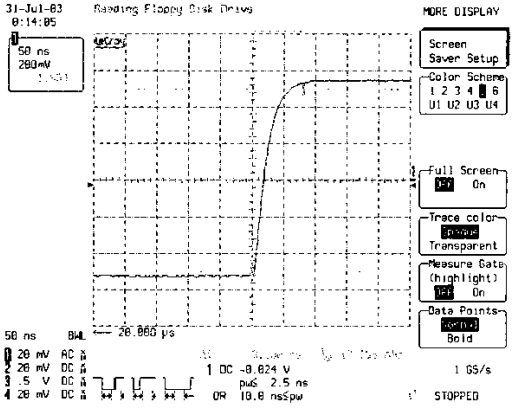

Fig. 4 Measured full-scale DAC output waveform.

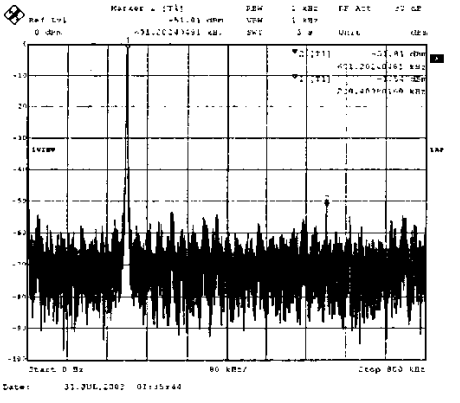

Fig. 5 The output spectrum for a 200KHz signal.

3. EXPERIMENTAL RESULTS

In the realistic circuit implementation, the circuit is verified with a supply voltage 2 V generated by a bandgap circuit and regulator not shown here. Measurements set-up is perform with differential to single-ended conversion of the amplifier component.

To predict the performance of the equally weighted current steering DAC, a MATLAB simulation was performed. The 256 normally distributed unit current sources were generated, with a mean of 1LSB and a standard deviation of 0.02 LSB. Fig. 3 is shown the static linearity profile.

The measured settling time of full-scale step is 80ns as shown Fig. 4. The single-tone output spectrum has been measured for several values of the signal frequency. Fig. 5 shown the DAC output frequency 200KHz spectrum with update rate 10MS/s. At 10MHz clock the SFDR is greater than 50dBc. The power consumption in this clock rate is 2mW. The output spectrum shows no significant inter-modulation spurs.

The active are of the DAC are measured 0.5 mm × 0.5 mm. Fig. 7 shows a die photo of the fabricated chip that does not include the bandgap and regulator integrated in one chip. It is fabricated in a 0.25-um CMOS mix-mode technology. A summary of the basic chip characteristics is given in Table I. This result corresponds to an intrinsic accuracy of 8 bits without any calibration, trimming, or dynamic averaging.

4. CONCLUSION

An 8-bit full equally weighted current steering DAC was implemented in a deep sub-micron mix-mode process without using any calibration options. By using the full equally weighted structure design in 8-bit resolution, the die area and current consumption can be significantly reduced, as compared. Some major dynamic linearity limitations have been analyzed and solved. The DAC has a 1 V full swing output voltage and consumes 2 mW for 200-kHz analog signal at 10Msample/s clock. Measurements confirm that 8-bit linearity is easily reached with this kind of configuration. The glitches in the output are minimized, by using properly overlapped and full equally weighted architecture, eliminating the output deglitch circuit, such as S/H.

This DAC is used in embedded applications with large amount of digital and RF circuitry in a transmitter for Bluetooth, it is shown without loss of performance.

Table I Summary of experimental results.

Technology	0.25um CMOS
Resolution	8 bits
INL	< 0.23 LSB
DNL	< 0.3 LSB
Update Rate	10 MS/s
Full-Scale Output Range	1 Vppd
SFDR @ 200kHz	50dBc
Rise/Fall Time	80ns
Power Consumption	2 mW
Supply Voltage	2 V
Die Area	0.25 mm^2

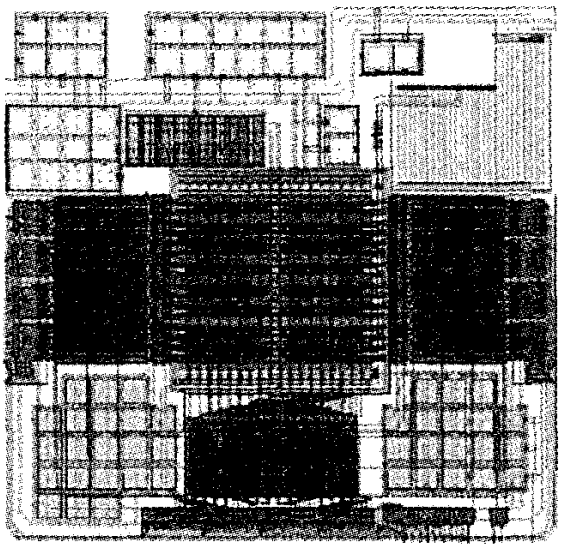

Fig.6 Chip layout.

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