Novel implementation method to realize all-optical logic gates

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Abstract. A novel implementation method based on the principle of optical interference to realize all-optical logic gates without the need of nonlinear optical materials is proposed. A general design rule of implementing the logic gates is obtained from the dimensionless intensity distribution of interference fringes formed by multiple equally spaced slits. Various designs of logic gates such as NAND, XOR, and so on are presented. The feasibility of implementing the logic gates and their exemplary applications to edge detection are demonstrated in several proof-of-principle experiments. System issues are discussed. [S0091-3286(98)03803-3]

Subject terms: optical logic gates; optical interference; optical computing.

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1 Introduction

Optical computing has inherent advantages such as massive connectivity, fast speed, and freedom from electromagnetic interference over electronic counterparts. Therefore, optical computing can be potentially applied to the fields where electronic computing finds itself either inappropriate or too time-consuming.[1–3] According to their functionality, optical computing systems can be divided into two categories: analog and digital ones for special and general purposes, respectively. Recently, the digital ones have been emphasized more because of the advances in opto-electronic materials, which make energy-efficient, ultra-fast digital switching in the optical domain feasible.[4] For the realization of digital optical computing, the very basic building block is an optical gate capable of performing universal logic functions, such as a NOR or a NAND gate. All other functional devices can then be built by employing different combinations of such basic gates.[2] To implement the optical logic gates, various physical mechanisms which enable switching light with another light have been proposed and demonstrated. These mechanisms include intrinsic optical bistability,[5] hybrid self-electro-optic effects,[6,7] hybrid transmitter/receiver combinations,[8,9] optical shadow casting,[10,11] image subtraction,[12,13] etc.

Another way of realizing optical switches is to shift and combine optical interference fringes.[14] Such an approach does not require particular encoding for input, and can be employed to generate parallel outputs of multiple logic functions. In these studies, nonlinear optical materials should be utilized to generate necessary phase changes, which in turn induce the shifting operation of interference fringes. In practice, however, these materials may not be satisfactory due to their poor time response and efficiency. In addition, different wavelengths are required for input and readout beams,[14] which may complicate system implementation. In this paper, we propose a novel implementation method which does not require nonlinear optical materials nor the shifting operation nor multi-wavelength operation but simply utilizes interference fringes produced by input signals in the object plane. In fact, the all-optical logic gates are constructed by employing electronic thresholding on some specifically designed locations in the observation plane; therefore, nonlinear optical materials are not needed. Note that the phase change in our method results from the distance difference rather than intensity-dependent index difference. In addition, the logic gate operation is obtained by spatially positioning a thresholding device instead of relying on nonlinear optical devices. Based on the concept, an optical binary data processor was proposed to perform combinational logic functions.[15] Here, we extend to unveil the underlying design principles and demonstrate the realization feasibility and their potential applications. We also note that as crossed laser beams illuminate colloidal particles, a diffraction grating can be formed to scatter the beams into certain positions so that optical logic gates are realized.[16] Our work, however, differs in working principle and implementation method as will be seen. The remaining paper is arranged as follows. In Section 2 the basic principle of the proposed logic gates is described. The design steps are detailed in Section 3, and some exemplary results are shown. Several proof-of-principle experiments on implementing such logic gates are described in Section 4. In Section 5, the proposed logic gates are demonstrated for the application of edge detection. The constraints of utilizing the logic gates for general digital computing are discussed in Section 6. Finally, in Section 7 we conclude our study.

2 Basic Principle

Schematically shown in Fig. 1 is a traditional optical system that performs the Fourier transform on which the design and demonstration of the all-optical logic gates to be discussed in the next few sections are all based. A collimated coherent beam is incident on the object region located at the plane $z=z_1$. The Fourier transform of the object, taken by a lens at $z=z_2$, is observed at $z=z_3$ when the

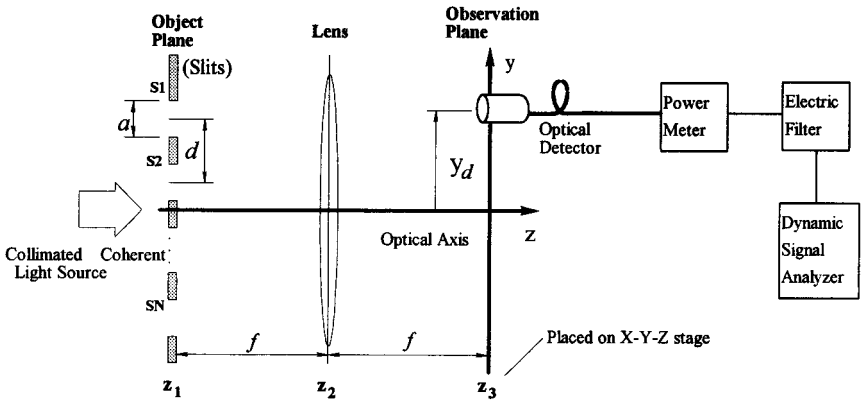


Fig. 1 Schematic setup of an optical system utilized to implement all-optical logic gates.

distance (z_2-z_1) and (z_3-z_2) are equal to the focal length of the lens f. Assume L_1 and L_2 are the maximum radial extents of the object and the observation regions, respectively. The following Fresnel conditions should be satisfied[17]:

$$f \gg L_1+L_2 \tag{1}$$

$$f^3 \gg \frac{\pi(L_1+L_2)^4}{4\lambda} \tag{2}$$

where λ is the wavelength of the incident beam. The first condition describes the paraxial approximation while the other implies that the higher order terms can be neglected. Equally spaced N slits are used as an object. The width of each slit is a, and d is the center-to-center spacing of the two neighboring slits. The intensity distribution in $z=z_3$ can be expressed as

$$I_N(y)=\frac{a^2 I_0}{(\lambda f)^2}\left(\frac{\sin\alpha}{\alpha}\right)^2\left(\frac{\sin N\beta}{\sin\beta}\right)^2$$
$$\alpha=\frac{\pi a}{\lambda}\frac{y}{f}, \quad \beta=\frac{\pi d}{\lambda}\frac{y}{f} \tag{3}$$

where I_0 is the intensity of light source, and $I_N(y)$ is the intensity variation along the y axis at $z=z_3$. The light intensity I_N can be further expressed as the dimensionless intensity I_N^*

$$I_N^*(y)=\frac{I_N(y)}{I_1}=\left(\frac{\sin\alpha}{\alpha}\right)^2\left(\frac{\sin N\beta}{\sin\beta}\right)^2 \tag{4}$$

where $I_1=a^2 I_0/(\lambda f)^2$. When the slit width a is relatively small as compared with the spacing d, the dimensionless intensity can be simplified as

$$I_N^*(y)=\left(\frac{\sin N\beta}{\sin\beta}\right)^2. \tag{5}$$

Fig. 2 shows the relationships between I_N^* $(N=1,2,...)$ and β. It is noted that, from these curves, the following relationships which lead to the determination of logic ''1'' or ''0'' are observed:

(1) At the position of $\beta=p\pi/2\pm\pi/M$, I_N^* $(N=1,2,...)$ would have m_M numbers of finite values. Each finite value of I_N^* is called level X, $X=0,1,...,m_M-1$. m_M is given by $m_M=[M/2]+1$, where [ ] denotes the integer part of the division result; M and p are integers. For example, for $p=0$ and $M=4$, then $m_M=3$; namely, I_N^* curves at $\beta=\pi/4$ have three finite values of 0, 1, and 2, i.e., three levels: level 0 is 0, level 1 is 1, and level 2 is 2.

(2) At the position of $\beta=p\pi/2\pm\pi/M$, the value of I_N^* in the X level is defined as I_{MX}, and $I_{MX}=((\sin X\times\pi/M)/(\sin\pi/M))^2$, where $X=0,1,2,...,m_M-1$.

(3) At the position of $\beta=p\pi/2\pm\pi/M$, each finite (level) value of I_N^* composes a finite set of N. The specific numbers, N's, allowed in the set (or level) depends on a given M. Fig. 3 shows examples of the tree diagram for $M=4$ and $M=9$. The numbers marked in circles are added

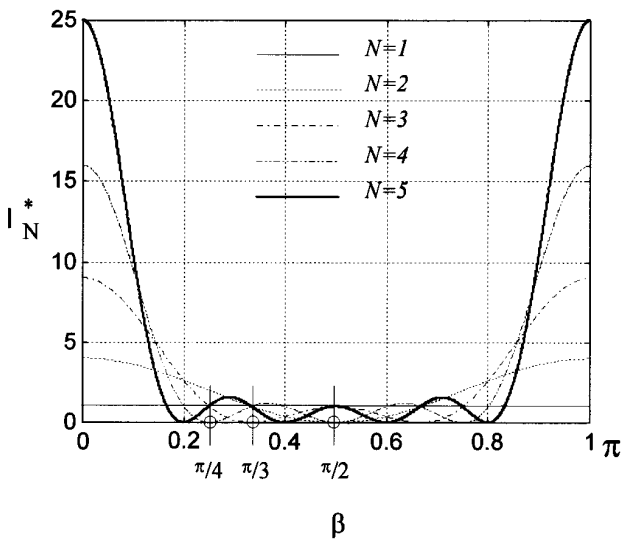


Fig. 2 Curves of dimensionless intensity I_N^* from equally spaced slits.

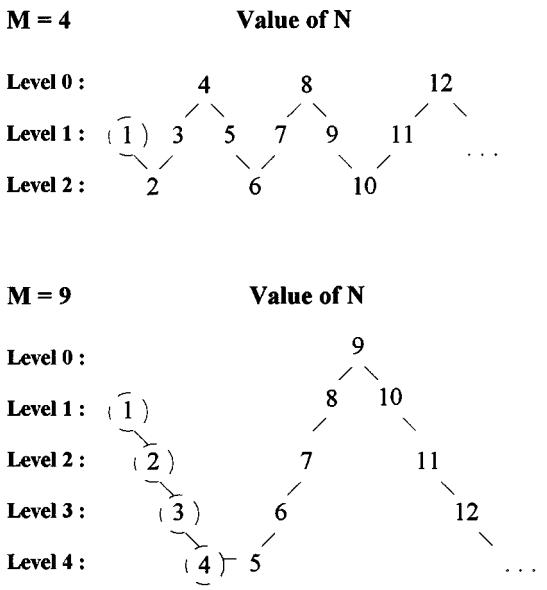


Fig. 3 Tree diagrams for $M=4$ and $M=9$.

to the levels to which they should correspond. For example, for $M=4$, $p=0$, the finite value $I_N^*=2$ (level 2) is contributed from $N=2,6,10,\ldots$.

(4) The portion $0\leqslant\beta\leqslant\pi/2$ of I_N^* is assigned as the basic unit of I_N^*, which repeats itself every $\pi/2$ period.

The tree diagram can be constructed to illustrate the relation of M, N, and level X. It starts with a given M, and the total level m_M is then determined. Next, the diagram continues the fill from the most upper level (i.e., level 0) which begins with multiples of M. The numbers in the next lower levels are filled by either adding or subtracting ''one'' from the numbers in the upper level. The tree diagram then expands downwards until all positive integers appear. However, any number ''N'' cannot expand beyond the m_M-1 level. Note that the number of levels, m_M, and light intensity at each level are determined for a given β. We will hereafter focus on the level $X=1$ where the dimensionless intensity $I_N^*=1$ is utilized to represent logic ''1'', and $I_N^*=0$ as logic ''0'' with appropriate corresponding β values.

3 Design of All-Optical Logic Gates

3.1 *Design Steps*

We designate ''1'' and ''0'' to represent respectively ''ON'' and ''OFF'' states of the slits ($S1,S2,\ldots,SN$). By switching ''ON'' and ''OFF'' of any arbitrary combination of the slits, different intensity distributions in the observation plane can be obtained. When a detector placed at y_d has an intensity equal to ''I_1'' (i.e., $I_N^*=1$) and null (i.e., $I_N^*=0$), its output signal is set to ''1'' and ''0'', respectively. The ranges of optical power that defines logic ''0'' and logic ''1'' determine the tolerance of positioning a detector. The power representing logic ''0'' is in turn determined by the detector's sensitivity while the one for logic ''1'' depends on the value of I_N^*. If $I_N^*<1$, it is always feasible to set a lower limit only above which the output signal is considered as logic ''1''. Conversely, if $I_N^*>1$, an electronic latching or limiting device can be utilized to hold the output after optical-to-electrical conversion at the level equivalent to ''1''. Since the thresholding is performed electronically in the detection plane, issues pertaining to the utilization of nonlinear optical materials therefore do not exist. Note that the positioning tolerance of a detector varies with the types of logic gate. Generally, one can design any desirable all-optical logic gates by appropriately choosing physical parameters. The design procedures are highlighted below with the flow chart shown in Fig. 4.

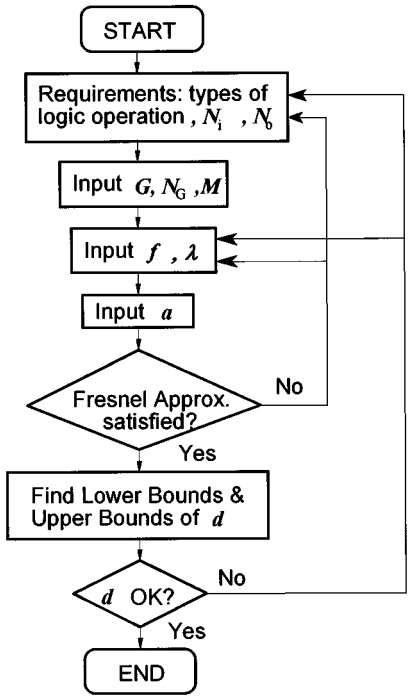


Fig. 4 Flow chart of design steps. See the text for each symbol definition.

Step 0. to specify functional requirements: the desired logic gate operations, input signal number (N_i) and output signal number (N_o).
Step 1. to decide slit patterns: the set number of equally spaced slits (G), the slit number of each set (N_G) and M value.
Step 2. to select the focal length of a lens (f) and light source's wavelength (λ).
Step 3. to specify slit width a.
Step 4. to examine the required Fresnel conditions as described in Eqs. (1) and (2).
Step 5. to decide the upper and the lower limits of d.
Step 6. both Step 4 and Step 5 are used to specify a suitable d for a given logic gate operation.

In Step 1, for simplicity, we always start with one set number of equally spaced slits, i.e. $G=1$. If the desired logic operation cannot be obtained, then two sets are used ($G=2$) where the second set is also equally spaced but with twice the spacing of the first one. In the same way,

more sets can be used to constitute the desired logic gates. The slit number, N_G, is determined by the input signal number, N_i. For an n-input logic gate, at least n slits ($S1,...,SN$) are required. Nevertheless, if the desired logic gate cannot be obtained for a given n slits, then additional reference slits ($R1,R2,...$) may be added to increase the number of curves in the I_N^* plot. It should be noted that in Step 5 the upper and the lower limits of d are determined separately by several factors. The factors include the slit width a and the assumption of $(\sin \alpha)/\alpha \sim 1$ for the determination of the lower limit, whereas the upper limit of d is determined by the instrumentation resolution. Hence, the upper and the lower bounds of d for various types of logic gates may be different.

3.2 *Design Examples*

In this section, we show some design examples to illustrate that all logic gates can be realized by employing the aforementioned principle and the design procedure. One can achieve NOT (invertor), OR, XOR, XNOR, NAND gates by utilizing one set of equally spaced slits. The design of the first three gates can be achieved by using two slits while an XNOR gate and an NAND gate require three slits. The design parameters of these logic gate operations are listed in Table 1 along with their intensity distributions and truth tables. In the calculation of dimensionless intensity and design parameters, the slit width is assumed to be 50 μm and a He-Ne laser is the light source. The optical axis always bisects the slit pattern so that any intensity distribution is symmetric to $y=0$ in the observation plane. The spacing between two adjacent slits may vary with logic gate operations. The circles on the horizontal axis of the pattern column in Table 1 indicate the detector positions for each logic operation. The corresponding β values are also specified. It is apparent that the positioning of the detector is not unique for each logic gate operation. Neither is the amount of positioning tolerance. For example, as seen from Table 1, a NOT gate has a smaller positioning tolerance than an OR gate owing to its steeper slope in the I_N^* curves. It is also noted that a well-designed all-optical logic gate can have not only more than two output ports, i.e. $N_o > 2$, but also more than one concurrent logic operation. For instance, as shown in Table 1, a set of two equally spaced slits ($d=1000$ μm) can have both NOT and XOR logic operations at the same location ($\beta = \pm \pi/2$).

4 Experiment Verification of Realization Feasibility

4.1 *Experimental Setup*

As shown in Fig. 1, an experimental system was set up to demonstrate the realization feasibility of the logic gates. Expanded light from an s-polarized He-Ne laser was used to illuminate the slit patterns located in the object plane. The intensity variation across the overall slits was within 5%. The slit patterns were lithographically fabricated according to the design parameters given in Table 1. The Fourier-transform lens had a focal length of 200 mm. A single-mode optical fiber whose core was small enough to be viewed as an effective ''point'' detector was used to collect light. The fiber was then connected to a power meter for optical-to-electrical conversion. The estimated error due to the discrepancy between the sizable and an ideal point detectors was less than 5% for the logic gates considered in Table 1. The ''point'' detector was mounted on a computer-controlled translation stage which had a resolution of less than 1 μm. The alignment of the detector and the laser was made by utilizing a precision gauge, and an average angular tilt of less than 0.01 radian was obtained. The electrical output signal was filtered and processed by a dynamic signal analyzer analyzed (HP 35665A). Other controllable errors that may affect system performance were either measured or estimated. These errors include the ones from lithographic fabrication of the slits (<1 μm), thermal expansion of the slit substrate (in the range of 0.005 to 0.705 μm/°C depending on which materials were being used), resolution and backlash of the translation stages, etc.

4.2 *Experimental Results*

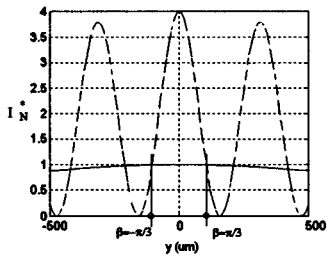
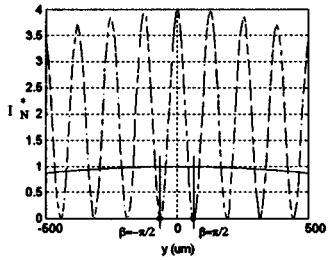
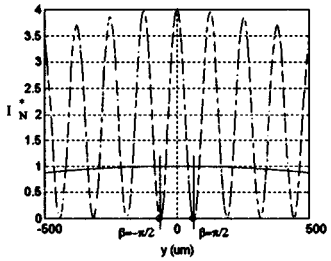
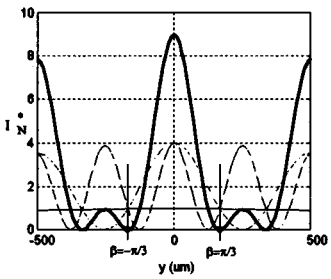
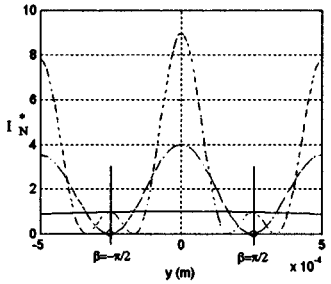
According to different values of d, the logic gates described in Table 2 can be divided into three categories, shown in Table 1, on which the experiments were based. Item I is for the ''OR'' gate operation, Item II is for the ''NOT'' and the ''XOR'' gates, and Item III is for the ''NAND'' and the ''XNOR''. Figs. 5(a), (b) and (c) show the experimental results and the calculation results of I_N^* from Items I, II and III, respectively. The experimental results are consistent with the calculated ones, verifying the feasibility of the proposed logic gate operations. The solid triangles shown in the figures mark the detector positions where desired logic operations occur.

Since parallelism is one of the advantages for all-optical logic gates, we set up an experiment to examine such a feature. Two sets of slits of different spacings spacing (250 and 400 μm) were placed next to each other, and two logic gate operations were performed simultaneously and independently by separate Fourier-transform lenses of the same focal length, 15 mm. No crosstalk between the two logic gate operations was observed, suggesting that the proposed system is indeed capable of parallel processing. It is expected that the extension to two-dimensional (2-D) massive parallel processing can be realized by utilizing, for example, a pair or more pairs of equally spaced slits and a lenslet array.

5 Application Example: Demonstration of Edge Detection

Since the optical logic gates are capable of parallel processing, many potential applications can therefore be explored. We now consider one of the applications, namely edge detection. Detecting the edge is an important and very basic function in the field of pattern recognition. Many all-optical and opto-electronic methods such as shadow casting,[18] polarization-encoded optical shadow casting (POSC),[19] and so on have been proposed for edge detection. These methods generally require multiple light sources and a coding scheme. In contrast, our method is similar to that described in Ref. 14 in the sense that both do not need coding; however, ours represent a simpler configuration since shifting operation and nonlinear optical materials are not required.

Table 1 Exemplary designs of all-optical logic gates ($a = 50\ \mu$m, $\lambda = 0.63\ \mu$m).

Logic Gate	Parameter	Patterns	Slits Schematic & Truth Tables
OR	$N_i = 2$ $N_o = 2$ $G = 1$ $N_1 = 2 = N$ $M = 3$ $d = 400$ um (550 um $\geq d \geq$ 13 um) $f = 200$ mm $y_d = \pm 105$ um		S1 S2 Pattern | S1 | S2 | S1+S2 No | 0 | 0 | 0 ——— | 0 | 1 | 1 ——— | 1 | 0 | 1 – – – | 1 | 1 | 1
NOT	$N_i = 2$ $N_o = 2$ $G = 1$ $N_1 = 2 = N$ $M = 2$ $d = 1000$ um (3.372 mm $\geq d \geq$ 13 um) $f = 200$ mm $y_d = \pm 63$ um		R S1 Pattern | S1 | $\overline{S1}$ ——— | 0 | 1 – – – – – | 1 | 0
XOR	$N_i = 2$ $N_o = 2$ $G = 1$ $N_1 = 2 = N$ $M = 2$ $d = 1000$ um (3.372 mm $\geq d \geq$ 13 um) $f = 200$ mm $y_d = \pm 63$ um		S1 S2 Pattern | S1 | S2 | S1 ⊕ S2 No | 0 | 0 | 0 ——— | 0 | 1 | 1 ——— | 1 | 0 | 1 – – – | 1 | 1 | 0
NAND	$N_i = 2$ $N_o = 2$ $G = 2$ $N_1 = 3 = N$ $N_2 = 2$ $M = 3$ $d = 250$ um $f = 200$ mm $y_d = \pm 169$ um		R S1 S2 Pattern | S1 | S2 | $\overline{S1}$ $\overline{S2}$ ——— | 0 | 0 | 1 – – – | 0 | 1 | 1 – · – · – | 1 | 0 | 1 ——— | 1 | 1 | 0
XNOR	$N_i = 2$ $N_o = 2$ $G = 1$ $N_1 = 3 = N$ $M = 2$ $d = 250$ um (2.532 mm $\geq d \geq$ 13 um) $f = 200$ mm $y_d = \pm 253$ um		S1 R S2 Pattern | S1 | S2 | $\overline{S1} \oplus \overline{S2}$ ——— | 0 | 0 | 1 – – – | 0 | 1 | 0 – – – | 1 | 0 | 0 – · – · – | 1 | 1 | 1

Note: "R" is for reference signal, and always set as "1".

Table 2 Categorized items of Table 1 for proof-of-principle experiments.

Item	f (mm)	d (μm)	Logic Gate
I	200	400	OR
II	200	1000	NOT,XOR
III	200	250	NAND,XNOR

To detect the edge of a binary image input, a basic building block is schematically shown in Fig. 6(a). An XOR gate is placed at the boundary of two image pixels. Only when one of the pixels is bright the output becomes ''1'' and thus completes the edge detection. Fig. 6(b) depicts a physical implementation. A simple proof-of-principle experiment was performed to demonstrate the detection of the edge of two adjacent pixels, each of $8 \times 8\ \text{mm}^2$. Two slits with width 50 μm were employed in the experiment to perform XOR logic operation. The results are shown in Fig. 6(c). Three cases representing different combinations of logic inputs were investigated. The input images shown in the left side of Fig. 6(c) were taken behind the slits in a way such that both input profiles and slit patterns could be observed. Shown in the right side are the corresponding interference patterns. The output signals of XOR gates are marked in rectangles. Only the second case, namely with the input of either (1,0) or (0,1), shows an output of logic ''1''. These results clearly indicate the feasibility of using the XOR logic gates for the edge detection. Since the interference pattern in the observation plane is symmetric to the optical axis, there are at least two locations with the same results from the XOR logic operation. The optical power from these two locations can then be combined to enhance the output signal level as depicted in Fig. 6(b).

6 Discussion

Although all basic logic gates can be realized by the proposed optical interference method, several constraints are observed. First, the cascading capability of optical output from one stage to the next, which is a common issue to most other systems, will pose a limitation because of the inefficiency in energy transport. Most losses occur in both the object and the observation planes. One way to reduce light losses while still maintaining reasonable positioning tolerance of the detector in the object plane is to increase the slit width to some extent. Another more effective way is to replace the slits with an array of point sources which may be generated by a lenslet array in its focal plane. In the observation plane, the output signal can be increased when light from the multiple output ports of the same logic function is collected by, for example, a fiber bundle. However, it is expected that the optical logic gates initially may find their best applications for those requiring only one-stage but capable of multiple gates operations. For the applications requiring cascading capability, an optical gain may be required for loss compensation like most other systems.

Secondly, since nonlinear optical materials are not involved in logic operation, the data processing time from object to observation planes (excluding input/output time) is basically equal to the transport time for light to travel over that distance and does not involve any material response time. For example, switching on time of 1 ps is achievable if a lenslet array with focal length of 150 μm and a fast detector array are used. In comparison, systems employing nonlinear optical or electro-optical materials may have slower processing time because certain material

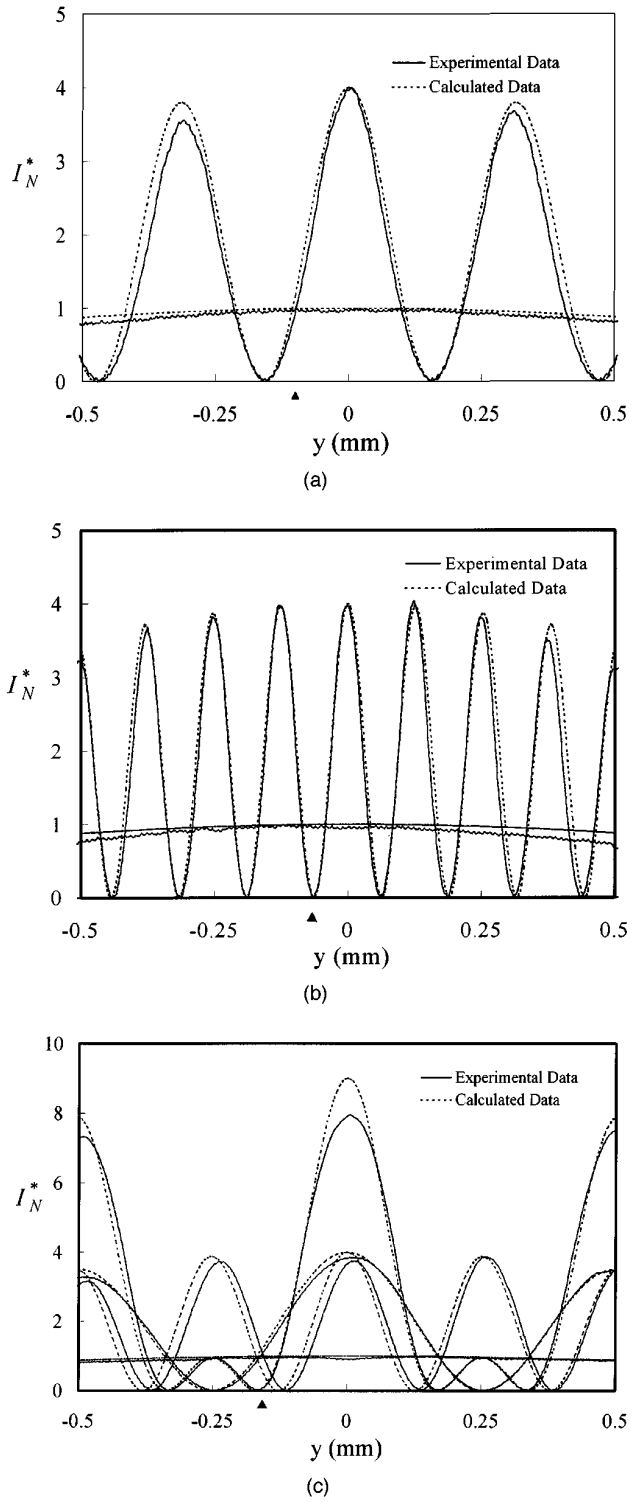
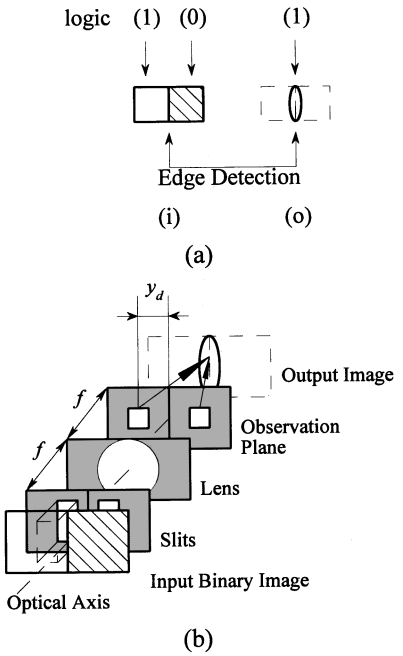


Fig. 5 Experimental and calculated results of I_N^* for (a) item I, (b) item II, (c) item III listed in Table 2.



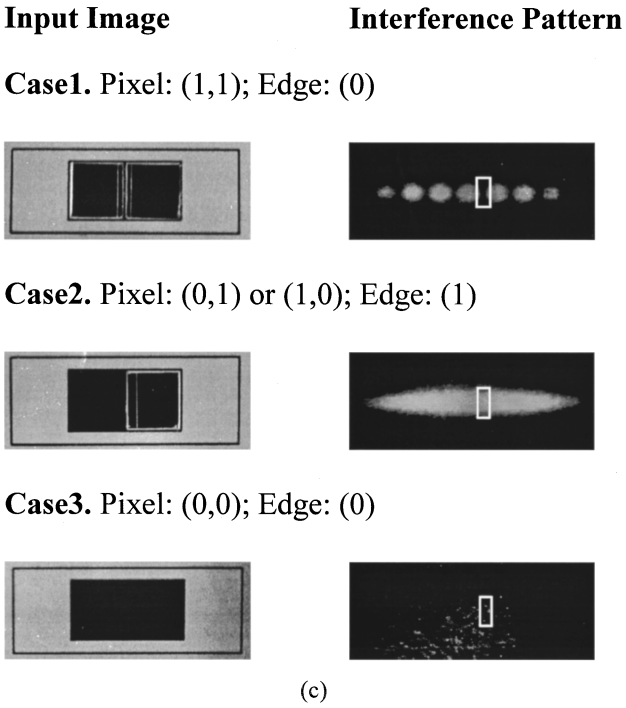


Fig. 6 (a) 1-D two-pixel edge detection (i=input, o=output), (b) 1-D edge detection system using XOR gates, (c) experimental results: left column shows input signals, right column with rectangular marks shows output signals.

response time is needed, despite the spatial transport time of light in those devices.

For more general applications other than the static conditions just described, spatial light modulators attached to the aforementioned slits with equal width and spacing in the object plane may be applied to change the slit patterns dynamically as input signals. It should be noted that this input speed would be determined by whatever input devices are used such as liquid crystal, SEED MQW structures,

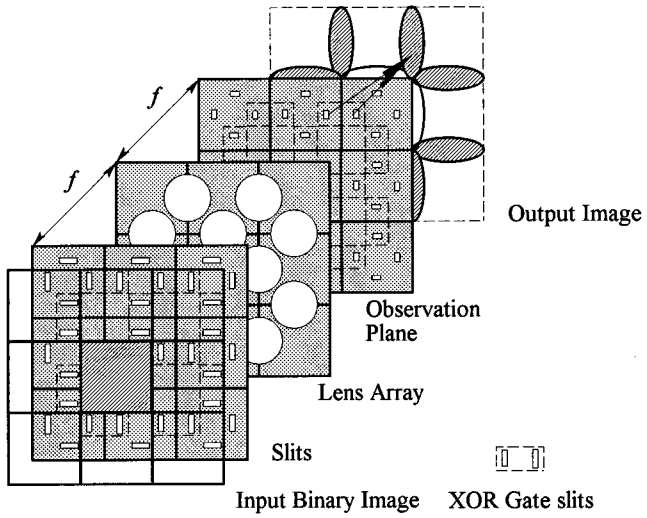


Fig. 7 Schematic setup of an optical system utilized to implement the edge detection of a 2-D nine-pixel image.

etc., and is the same for each optical computing scheme. Therefore, the overall data processing time of our method is inherently fast.

Finally, since we have successfully demonstrated edge detection by a simple two-pixel system consisting of XOR gates, detecting the edges of a 2-D nine-pixel image element can thus be inferred. Fig. 7 schematically shows how a multiple of elementary XOR gates and a lenslet array are utilized for such detection. Moreover, potential extension to a more practical application which may require, for example, 500×500 pixels can be realized by utilizing enabling technologies. Such technologies include fabrication of gratings, micro-lenses,[20,21] stack planar optics,[22] and so on to achieve the desired packaged dimension and alignment requirement. By combining both 2-D parallelism and the inherent fast switching, vast processing capability is expected.

7 Conclusion

An optical interference method for realizing all-optical logic gates has been proposed and demonstrated. The method is based on the interference patterns resulting from different numbers of equally spaced slits. We show that the dimensionless intensity resulting from one or multiple sets of the slits can be utilized to obtain any desired logic operations when detecting locations are appropriately chosen. Some design examples to implement such basic logic gates are demonstrated in Table 1. In addition, the results from the proof-of-principle experiments show good agreement with the calculated ones, a fact which verifies the feasibility of building such logic gates. In contrast to conventional all-optical logic gates, the proposed ones have a simpler configuration, and do not require any nonlinear optical materials or coding schemes. Although cascading from one stage of the optical gates to the next may require optical amplifiers to compensate for losses, these logic gates can be used in applications such as edge detection that need no more than a few successive stages.

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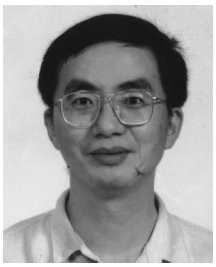

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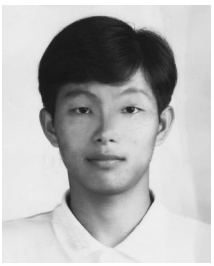

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