A High-Speed 1.5V Clocked BiCMOS Latch for BiCMOS Dynamic Pipelined Digital Logic VLSI Systems

J. B. Kuo, J. H. Lou and K. W. Su
Dept. of Electrical Eng. Rm. 338, National Taiwan University
Roosevelt Rd., Sec. 4, Taipei, Taiwan 106-17
Fax:886-2-363-6893, Telephone:886-2-363-5251 x338

Abstract

This paper presents a high-speed 1.5V clocked BiCMOS dynamic latch, which is derived from a clocked CMOS dynamic latch and a BiCMOS logic gate using BiPMOS pull-down structure, and a bootstrapped pull-up structure, for BiCMOS dynamic pipelined digital logic systems. Based on the study, for driving a load capacitance of 2pf, the 1.5V clocked BiCMOS dynamic latch provides a 2.5x improvement in switching time as compared to the clocked CMOS one.

1 Introduction

Recently, a 1.5V full-swing BiCMOS dynamic logic gate circuit as shown in Fig. 1, based on a dynamic pull-down BiPMOS configuration, suitable for high-speed VLSI using advanced low-voltage BiCMOS technology has been reported [1][2]. As for a clocked CMOS dynamic one [3], for a BiCMOS dynamic pipelined digital logic VLSI system as shown in Fig. 2, in addition to the BiCMOS dynamic logic gates, clocked BiCMOS dynamic latches are also required. Although clocked CMOS dynamic latches have been reported [3], the switching speed may be too slow as the load capacitance of the latches is large. In this paper, a clocked BiCMOS dynamic latch, which is derived from a clocked CMOS dynamic latch and a BiCMOS logic gate using BiPMOS pull-down structure, and a bootstrapped pull-up structure, for BiCMOS dynamic pipelined digital logic systems, is described.

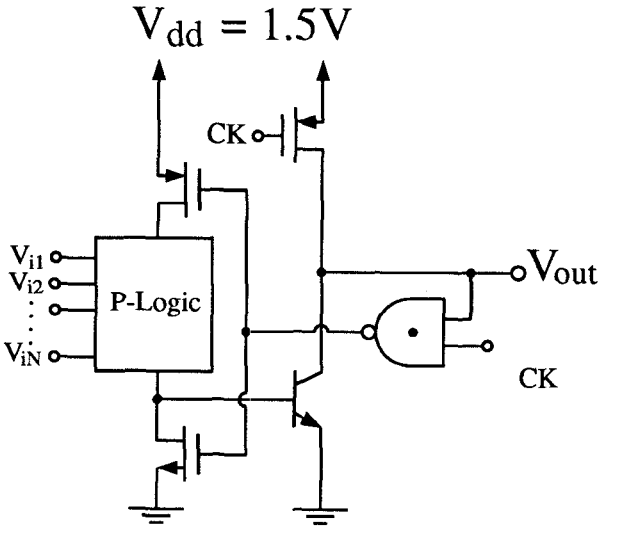


Figure 1: The 1.5V BiCMOS dynamic logic circuit based on BiPMOS pull-down structure.

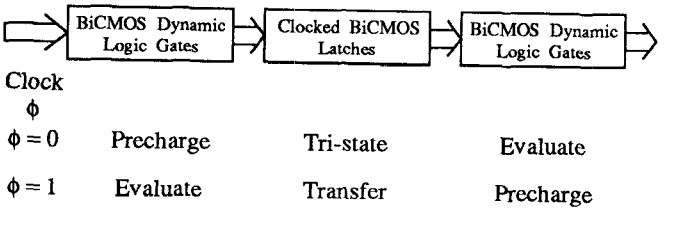


Figure 2: A BiCMOS dynamic pipelined digital logic VLSI system.

2 1.5V Clocked BiCMOS Latch

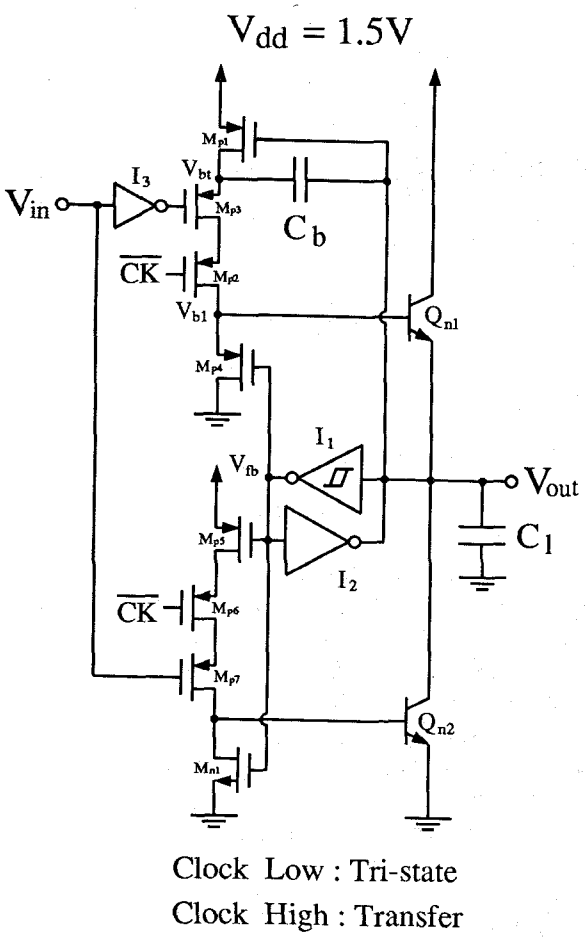
Fig. 3(a) shows the 1.5V clocked BiCMOS dynamic latch circuit, which is derived from the clocked CMOS

dynamic latch circuit as shown in Fig. 3(b). As shown in the figure, the clocked BiCMOS dynamic latch is composed of the active pull-up circuit and the active pull-down circuit. In the active pull-up circuit, a BiPMOS pull-up structure (Q_{n1}, M_{p2}, M_{p3}) is used. In the active pull-down circuit, a BiPMOS pull-down structure (Q_{n2}, M_{p6}, M_{p7}) is used. A Schmitt trigger (I_1) and a CMOS inverter (I_2) in the feeback path is used to implement dynamic operation of the circuit — the bipolar devices are only on during transient. After the transient, both bipolar devices are turned off. In addition, clock controlled devices (M_{p4}, M_{n1}) are used to implement the tristate and the logic transfer states of the latch. As clock is low ($\overline{CK}$ is high), both bipolar devices are turned off — the tri-state operation. As clock is high ($\overline{CK}$ is low), depending on the input V_{in}, only one bipolar device is on during switching.

In addition, in the active pull-up circuit, in order to increase the output swing and thus the switching time, a bootstrapped capacitor C_b is placed between the output node and the source node of M_{p3}.

3 Performance Evaluation

In order to evaluate the performance of the newly derived circuit, a clocked BiCMOS dynamic latch circuit based on $1\mu m$ BiCMOS technology has been designed. The aspect ratios of the PMOS and NMOS devices are $20\mu/1\mu m$ and $10\mu/1\mu m$, respectively. Fig. 4 shows the transient waveforms of the 1.5V clocked BiCMOS dynamic latch circuit driving an output load of $1pf$ during pull-up and pull-down. As shown in Fig. 4, before the pull-up transient, the input node (V_{in}) is low and the output node (V_{out}) is low. M_{p2} is always on. M_{p4} is off and M_{p1} is on. At this time, the bootstrapped capacitor C_b has been charged with a voltage difference of $1.5V$. During the pull-up transient, after V_{in} switches from low to high, M_{p3} turns on, consequently, the bipolar device Q_{n1} is being turned on by a base current provided by M_{p1}, M_{p2} and M_{p3}. Therefore, V_{out} slews upward. Due to the bootstrapped capacitor C_b, V_{bt} exceeds 1.5V – internal voltage overshoot. As a result, the base current increases and V_{out} slews toward 1.5V. As V_{out} turns high, V_{fb} gradually turns low, thus triggers M_{p4}. As M_{P4} turns on, the base charging current also decreases and the charge in the capacitor C_b recesses. As a result, the internal voltage overshoot reaches its peak and V_{bt} comes down. Then, the discharging base current caused by M_{p4} turns Q_{n1} off. As shown in Fig. 4, thee active pull-down procedure is similar to as de-



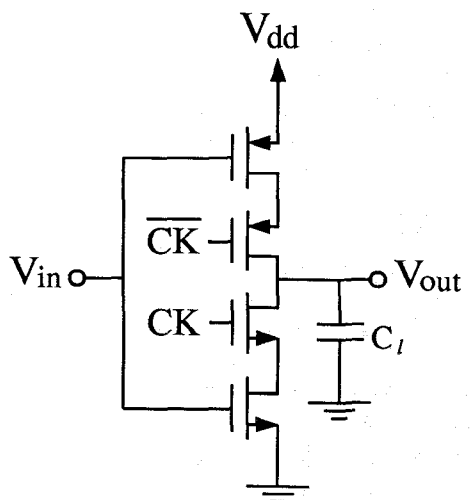


Figure 3: (a) The 1.5V clocked BiCMOS dynamic latch circuit. (b)The clocked CMOS dynamic latch circuit.

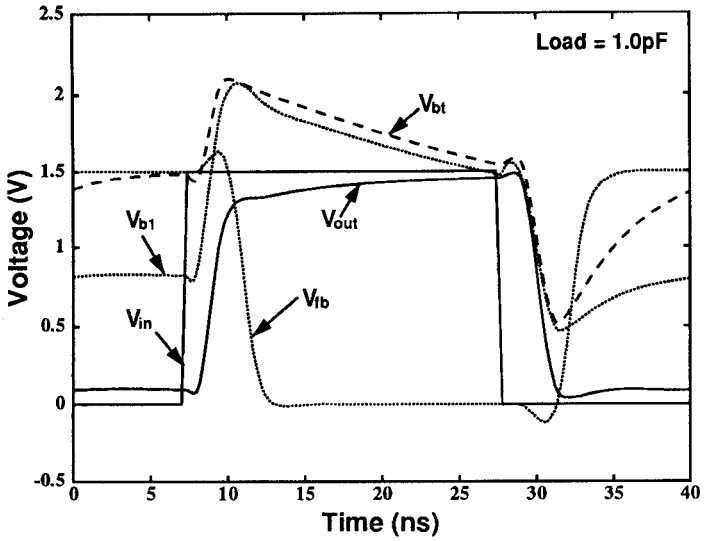


Figure 4: Transients waveforms of the 1.5V clocked BiCMOS dynamic latch circuit driving an output load of $1pf$ during pull-up and pull-down.

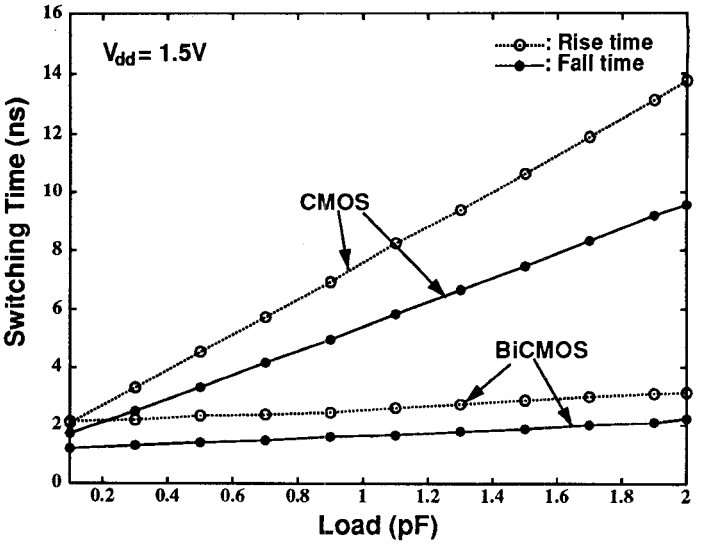


Figure 5: Rise time and fall time vs. load capacitance of the dynamic latch using 1.5V clocked BiCMOS and CMOS techniques.

scribed in [1][2].

Fig. 5 shows the rise time and fall time vs. load capacitance of the clocked BiCMOS dynamic latch. Also shown in the figure is the result for the clocked CMOS dynamic latch. As shown in the figure, the clocked BiCMOS dynamic latch provides a consistent improvement in rise time and fall time. With an output load of $2pf$, both the rise and the fall times improves 4.4x.

4 Conclusion

In this paper, a high-speed 1.5V clocked BiCMOS dynamic latch, which is derived from a clocked CMOS dynamic latch and a BiCMOS logic gate using BiPMOS pull-down structure, and a bootstrapped pull-up structure, for BiCMOS dynamic pipelined digital logic systems, has been described. Based on the study, for driving a load capacitance of 2pf, the 1.5V clocked BiCMOS dynamic latch provides a 1.9x improvement in switching time as compared to the clocked CMOS one.

Acknowledgments

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References

[1] J. B. Kuo, S. S. Chen, C. S. Chiang, K. W. Su, and J. H. Lou, "A 1.5V BiCMOS Dynamic Logic Circuit using a "BiPMOS Pull-down" Structure for VLSI Implementation of Full Adders," *IEEE TCAS*, April 1994

[2] J. B. Kuo, S. S. Chen, C. S. Chiang, K. W. Su, and J. H. Lou, "A 1.5V BiCMOS Dynamic Logic Circuit using a "BiPMOS Pull-down" Structure for VLSI Implementation of Full Adders," *IEEE JSSC*, Jan 1995

[3] N. F. Goncalves, H. J. DeMan, "NORA: A Race-free Dynamic CMOS Technique for Pipelined Logic Structures," *IEEE JSSC*, June 1983

[4] S. H. K. Embabi, A. Bellaouar, and K. Islam, "A Bootstrapped Bipolar CMOS gate for Low-Voltage Applications," *IEEE JSSC*, Jan. 1995