High-performance ZnO thin-film transistors fabricated at low temperature on glass substrates

C.C. Liu, Y.S. Chen and J.J. Huang

A high-performance enhancement-mode ZnO thin-film transistor (TFT) on a glass substrate is demonstrated. The ZnO thin film is deposited by RF magnetron sputtering with the presence of O_2 at low deposition rate and low temperature. The I_{DS} is as high as 1 mA when biased at the saturation region $V_{DS}=10$–20 V and $V_{GS}=5$ V without any post-thermal anneal. The I_{on}/I_{off} ratio is 3×10^6. The results are among the best ZnO TFTs ever obtained.

Introduction: The wide bandgap ZnO semiconductor material has attracted much attention recently for applications in transparent circuits and on flexible substrates for flat panel displays. The invisible transistors on thin-film transistor-liquid crystal displays (TFT-LCDs) have the advantage of a higher aperture ratio for the transmission of backlight. Several approaches have been used to deposit ZnO thin films, including sputtering [1], pulsed laser deposition [2], chemical vapour deposition [3] and molecular beam epitaxy [4]. Most of these methods require high temperature process during ZnO coating and contact alloy in order to obtain better crystalline quality and contact resistance. To apply ZnO to flat panel displays, especially on flexible substrates, low-temperature deposition was also proposed by sputtering, spin-coating, and chemical bath [5–7]. The device performance, depending on the process conditions and material properties such as crystalline quality (and thus the carrier mobility) in the ZnO channel, from the above approaches typically showed an I_{on}/I_{off} ratio around 10^5 to 10^6 and I_{DS} around 6 to 60 μA when biased at V_{DS} and V_{GS} around 30–40 V [6–9]. To apply ZnO TFTs to active matrix LCDs (AMLCDs), higher operating currents at lower bias voltages are required.

In this Letter, we demonstrate a high-performance enhancement-mode ZnO TFT on a glass substrate. We utilised a top-gate approach to fabricate the devices. The ZnO thin film is deposited by RF magnetron sputtering at low deposition rate and low temperature with the presence of O_2. The I_{DS}–V_{DS} curves, I_{on}/I_{off} ratio and leakage current I_{GS} are compared before and after contact alloy. We believe the results are among the best ZnO TFTs ever obtained.

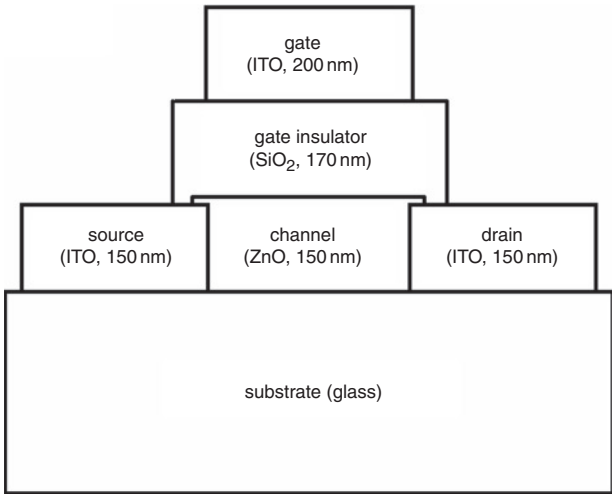

Fig. 1 *Schematic cross-sectional view of TFT structure*

Experiment: Fig. 1 schematically illustrates a top-gate-type transparent TFT device using ZnO as the active channel layer. First, a glass substrate (Corning 1737 glass) is blanket-sputtered with a highly transparent, *n*-type indium tin oxide (ITO). The ITO layer thickness is 150 nm. The ITO source and drain regions are then defined by photolithography and wet etching ($HCl:H_2O_2=1:3$). We then deposited the 150 nm-thick ZnO channel layer by RF magnetron sputtering in 10^{-2} torr of Ar/O_2 (15:1). The purpose of oxygen gas is to decrease the carrier density of the ZnO layer so that enhancement-mode TFTs can be obtained. During deposition, RF power was 100 W and the wafer holder was attached to a water running pipe to remove the generated heat. Moreover, the deposition rate was kept at around 5 nm/min to mitigate the particle bombardment to achieve better polycrystalline quality. The channel width and length were 1000 and 300 μm, respectively, yielding a width-to-length ratio 3.3. In the subsequent step, a 170 nm-thick SiO_2, layer was sputtered as the gate insulator. Again, we adapted a slow deposition rate approach (2 nm/min in this work) with 100 W RF power. Finally, the gate electrode region was coated with a 200 nm sputtered ITO layer. All ITO electrodes, including source, drain and gate contacts, were sputtered using 120 W RF power with higher deposition rate 20 nm/min.

Results and discussion: The current-voltage characteristics were measured using an Agilent 4155 C. Measurements were performed in darkness to avoid light induced photocurrents. The I_{DS}–V_{DS} curves of the ZnO TFT before contact alloy are shown in Fig. 2*a*. The I_{DS} is 1.06 mA at the bias condition $V_{DS}=5$ V and $V_{DS}=20$ V. Our enhancement-mode ZnO thin-film transistor implies that the power dissipation can be minimised when the device is normally-off, making it suitable for applications about which power consumption is a concern. Fig. 2*b* shows the transfer characteristics and gate leakage current. The I_{on}/I_{off} ratio, calculated from the drain current at its maximum and minimum value, is 3×10^6 . The gate leakage current is smaller than 3×10^{-8} A with V_{GS} less than 7 V, which is attributed to a high-quality SiO_2 gate insulting layer during device fabrication. Furthermore, the threshold voltage, determined from the $(I_{DS})^{1/2}$–V_{GS} curve, is around 1.7 V. The low threshold voltage ensures that ZnO TFT circuits are operated at low voltage and thus low power consumption can be achieved.

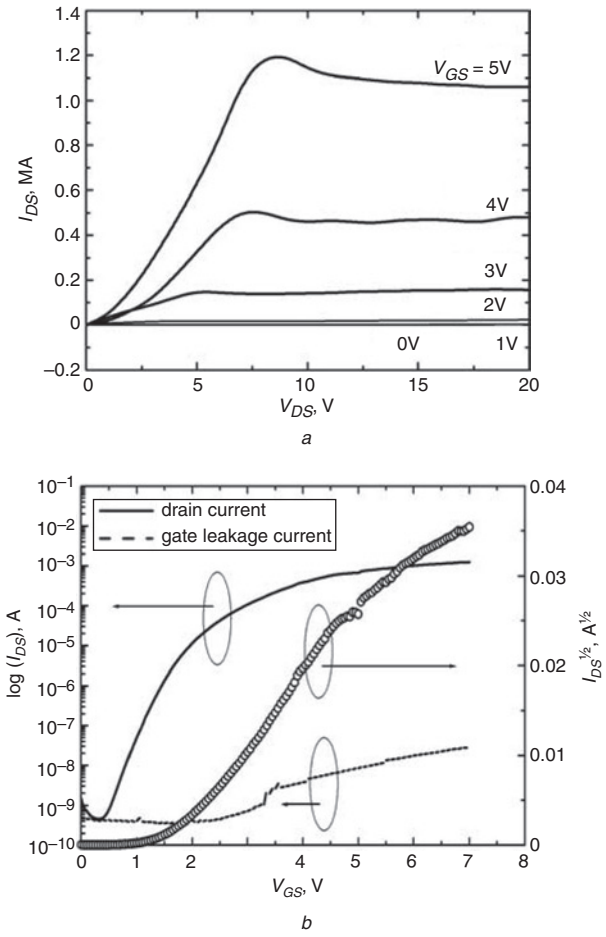

Fig. 2 *Electrical characteristics of TFT with ZnO channel and SiO_2 gate insulator before alloy*

a I_{DS}–V_{DS} curves
b Log scale I_{DS} and I_{GS} against V_{GS} at $V_{DS}=20$ V, and $(I_{DS})^{1/2}$–V_{GS} curve for determining threshold voltage

It is observed that a high contact resistance between the source/drain electrode and the ZnO channel layer in the triode region and an overshoot at the onset of saturation exist in Fig. 2*a*. The I_{DS}–V_{DS}

curves behave like a TFT device in series with a Schottky diode component. To decrease contact resistance the sample is then subject to a 200°C, 15 min rapid thermal process in N_2. The electrical characteristics are shown in Fig. 3. The currents in the saturation region in Fig. 3*a* show little change from those before alloy, indicating that the carrier mobility in the ZnO layer is not affected by the alloy condition. The slopes of I_{DS}–V_{DS} curves in the triode region are much more linear and the overshoot at the onset of the saturation region is reduced for devices after alloy. We attribute the improvement of device performance to a better contact condition between the source/drain ITO and the ZnO layer. As for the transfer characteristics, the I_{on}/I_{off} ratio becomes 3×10^4 and the gate leakage current increases to 2×10^{-7} A at $V_{GS} = 7$ V after thermal anneal.

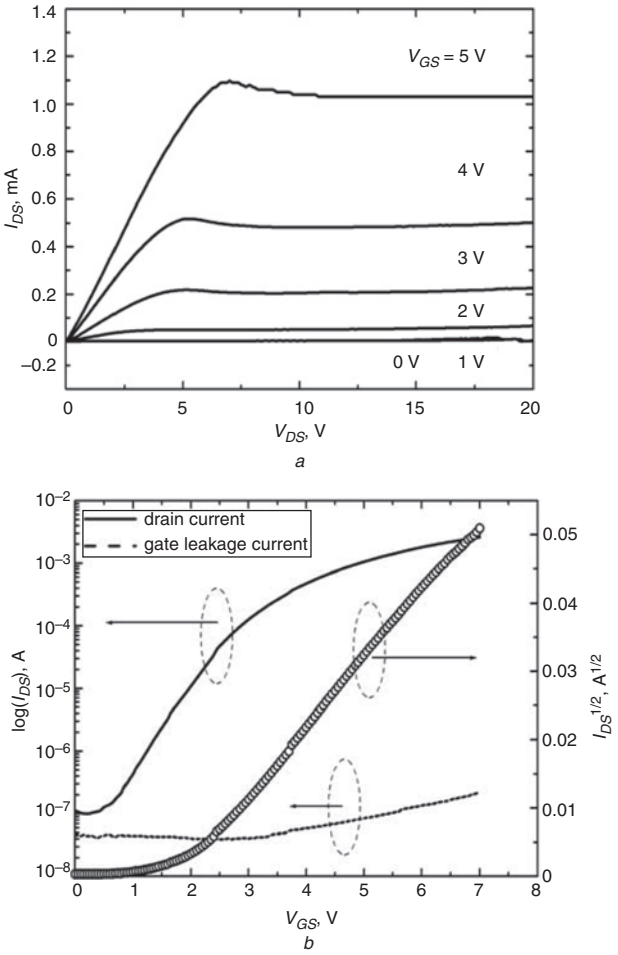

Fig. 3 *Electrical characteristics of TFTs subject to 200°C, 5 min rapid thermal process in N_2*

a I_{DS}–V_{DS} curves
b Log scale I_{DS} and I_{GS} against V_{GS} at $V_{DS} = 20$ V, and $(I_{DS})^{1/2}$–V_{GS} curve

Conclusion: We have demonstrated a high-performance enhancement-mode ZnO TFT on a glass substrate. Before contact alloy, the I_{DS} is as high as 1 mA when biased at the saturation region $V_{DS} = 10$–20 V and $V_{GS} = 5$ V. The I_{on}/I_{off} ratio is 3×10^6. The source and drain contacts are improved after 200°C, 15 min alloy. The slopes of I_{DS}–V_{DS} curves in the triode region are much more linear and the overshoot at the onset of saturation region is reduced. The fabrication steps developed and the ZnO TFT performance in this work are suitable for AMLCD applications.

16 May 2006
Electronics Letters online no: 20061518
doi: 10.1049/el:20061518

C.C. Liu, Y.S. Chen and J.J. Huang (*Graduate Institute of Electro-Optical Engineering, National Taiwan University, 1 Roosevelt Rd, Sec.4, Taipei 106, Taiwan, Republic of China*)

E-mail: jjhuang@cc.ee.ntu.edu.tw

References

1 Yao, Q.J., and Li, D.J.: 'Fabrication and property study of thin film transistor using rf sputtered ZnO as channel layer', *J. Non-Cryst. Solids*, 2005, **351**, pp. 3191–3194
2 Kim, I.-D., Choi, Y.W., and Tuller, H.L.: 'Low-voltage ZnO thin-film transistors with high-*K* $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ gate insulator for transparent and flexible electronics', *Appl. Phys. Lett.*, 2005, **87**, p. 043509
3 Minegishi, K., Koiwai, Y., Kikuchi, Y., Yano, K., Kasuga, M., and Shimizu, A.: 'Growth of *p*-type zinc oxide film by chemical vapor deposition', *J. Appl. Phys.,* Part 2, 1997, **36**, p. 1453
4 Tang, Z.K., Wong, G.K.L., Yu, P., Kawasaki, M., Ohtomo, A., Koinuma, H., and Segawa, Y.: 'Room-temperature ultraviolet laser emission from self-assembled ZnO microcrystallite thin films', *Appl. Phys. Lett.*, 1998, **72**, pp. 3270–3272
5 Fortunato, E.M.C., Barquinha, P.M.C., Pimentel, A.C.M.B.G., Conçalves, A.M.F., and Martins, R.F.P.: 'Fully tranparent ZnO thin film transistor produced at room temperature', *Adv. Mater.*, 2005, (5), pp. 590–594
6 Norris, B.J., Anderson, J., Wager, J.F., and Keszler, D.A.: 'Spin-coated zinc oxide transparent transistors', *J. Phys. D, Appl. Phys.*, 2003, **36**, pp. L105–L107
7 Cheng, H.-C., Chen, C.-F., and Lee, C.-C.: 'Thin-film transistors with active layers of zinc oxide (ZnO) fabricated by low-temperature chemical bath method', *Thin Solid Films*, 2006, **498**, pp. 142–145
8 Carcia, P.F., McLean, R.S., Reilly, M.H., and Nunes, G., Jr.,: 'Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering', *Appl. Phys. Lett.*, 2002, (7), pp. 1117–1119
9 Hoffman, R.L., Norris, B.J., and Wager, J.F.: 'ZnO-based transparent thin-film transistors', *Appl. Phys. Lett.*, 2003, **82**, (5), pp. 733–735