aspect of early vision processing. We studied the dependence of the output on the amplitude of the input in a series of simulations, which showed that the peak and the plateau values of the response are nonlinear monotonic increasing functions of J and nonlinear monotonic decreasing functions of I. Together, these results suggest that the circuit encodes the contrast rather than the absolute amplitude of the input. Fig. 3 shows that the peak and the plateau values of the response are approximately linear functions of Weber contrast on a logarithmic scale. Fig. 4 shows that the peak and the plateau values of the response are approximately linear functions of Michelson contrast on a linear scale, in particular when contrast is above 0.3.

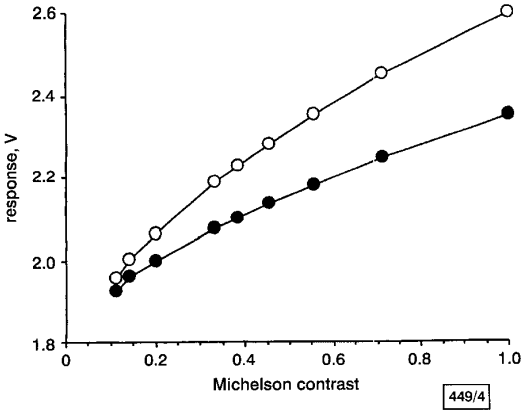


Fig. 4 *Peak and plateau values of response against Michelson contrast (defined as J/(J + 2I))*

○ peak
● plateau

Conclusion: Simulations of the proposed design have shown that the circuit exhibits non-associative learning and encodes the contrast rather than the absolute amplitude of the input. These properties result from temporal and spatial adaptation achieved through variable-gain synapses and lateral inhibition, respectively.

8 May 2001
Electronics Letters Online No: 20010631
DOI: 10.1049/el:20010631

G.B. Zhang and J. Liu (*Department of Electrical Engineering, The University of Texas at Dallas, PO Box 830688, EC33, Richardson, TX 75083-0688, USA*)

G. Bayramoglu and H. Ogmen (*Department of Electrical & Computer Engineering, University of Houston, Houston, TX 77204-4005, USA*)

E-mail: ogmen@uh.edu

References

1 INDIVERI, G., and DOUGLAS, R.: 'Neuromorphic vision sensors', *Science*, 2000, **288**, pp. 1189–1190

2 COOMBE, P.E., SRINIVASAN, M.V., and GUY, R.G.: 'Are the large monopolar cells of the insect lamina on the optomotor pathway', *J. Comp. Physiol. A*, 1989, **166**, pp. 23–35

3 OGMEN, H., and GAGNE, S.: 'Neural network architectures for motion perception and elementary motion detection in the fly visual system', *Neural Netw.*, 1990, **3**, pp. 487–505

4 OGMEN, H., and GAGNE, S.: 'Neural models for sustained and on-off units of insect lamina', *Biol. Cybernetics*, 1990, **63**, pp. 51–60

5 ARNETT, D.W.: 'Spatial and temporal integration properties of units in the first optic ganglion of dipterans', *J. Neurophysiol.*, 1972, **35**, pp. 429–444

6 JANSONIUS, N.M., and VAN HATEREN, J.H.: 'On spiking units in the first optic chiasm of the blowfly III. The sustaining unit', *J. Comp. Physiol. A*, 1993, **173**, pp. 187–192

7 CARPENTER, G.A., and GROSSBERG, S.: 'Adaptation and transmitter gating in vertebrate photoreceptors', *J. Theoretical Neurobiol.*, 1981, **1**, pp. 1–42

CMOS current-mode exponential-control variable-gain amplifier

C.-C. Chang, M.-L. Lin and S.-I. Liu

A CMOS current-mode exponential-control variable-gain amplifier is presented. It consists of a first-order current-mode pseudo-exponential circuit and a current-mode multiplier. Based on the Taylor's series expansion, the pseudo-exponential circuit can be realised by MOSFETs in saturation. The proposed circuit has been fabricated in a 0.5 μm N-well CMOS process with a gain control range of 15 dB. The experimental results confirm the feasibility of the proposed variable-gain amplifier.

Introduction: A multiplier with an input signal and an exponential input can realise a variable-gain amplifier (VGA). Traditionally, the exponential input circuit is implemented in bipolar technology due to the exponential characteristics. It could not be realised directly by MOSFETs in saturation due to square-law characteristics. Thus, several pseudo-exponential functions [1 – 6] have been explored. In this Letter, a CMOS current-mode VGA, which consists of a pseudo-exponential circuit and a current-mode multiplier, is presented. The pseudo-exponential circuit is based on the approximated Taylor's series. The proposed circuits have been fabricated in a 0.5 μm N-well CMOS process and the experimental results are given to demonstrate this proposed VGA.

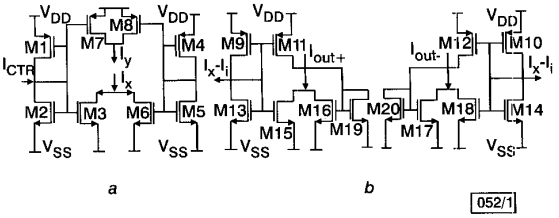


Fig. 1 *First-order pseudo-exponential circuit and current-mode multiplier*

a Exponential circuit
b Multiplier

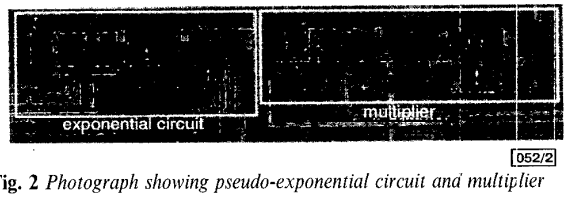


Fig. 2 *Photograph showing pseudo-exponential circuit and multiplier*

Circuit implementation: The proposed VGA consists of a current-mode multiplier and a current-mode first-order pseudo-exponential circuit. The pseudo-exponential circuit is shown in Fig. 1*a* [2, 6], the PMOS and NMOS transistors being in saturation and having the same transconductance parameters, K. The drain currents of $M1$ and $M2$ can be given as

$$I_{M1} = K\left(\frac{G}{2} - \frac{I_{CTR}}{2KG}\right)^2 \quad (1)$$

and

$$I_{M2} = K\left(\frac{G}{2} + \frac{I_{CTR}}{2KG}\right)^2 \quad (2)$$

where $G = V_{DD} - V_{SS} - |V_{Tp}| - V_{Tn}$. Furthermore, according to the approximation of the Taylor's series expansion (i.e. $2b^2 \cdot e^{(a/b)x} \cong b^2 + (b+ax)^2$ for $|(a/b)x| < 1$), the output current, I_X ($= I_{M3} + I_{M6} = I_{M2} + I_{M5}$), can be expressed as

$$I_X = K\left(\frac{G}{2} + \frac{I_{CTR}}{2KG}\right)^2 + K\left(\frac{G}{2}\right)^2 \cong K\left[2\left(\frac{G}{2}\right)^2\right] \cdot e^{\frac{I_{CTR}}{KG^2}} \quad (3)$$

The error of the pseudo-exponential function is within 5% if $-0.575 \le I_{CTR}/KG^2 \le 0.815$ and the output dynamic range can be 15 dB. Inversely, taking the output current, I_Y, from the two PMOS transistors, $M7$ and $M8$, a negative exponential factor function can be obtained as

$$I_Y = K\left(\frac{G}{2} - \frac{I_{CTR}}{2KG}\right)^2 + K\left(\frac{G}{2}\right)^2 \cong K\left[2\left(\frac{G}{2}\right)^2\right] \cdot e^{\frac{-I_{CTR}}{KG^2}} \quad (4)$$

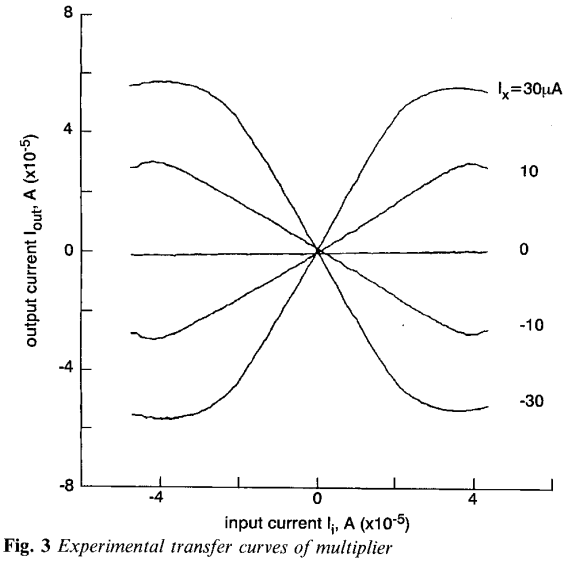
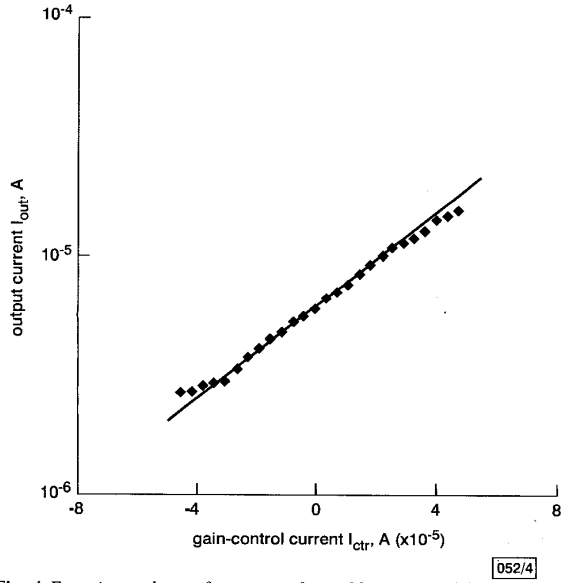


Fig. 3 *Experimental transfer curves of multiplier*



052/4

Fig. 4 *Experimental transfer curves of variable gain amplifier*

——— ideal curve
◆ experimental results

The proposed current-mode multiplier using the same building blocks is shown in Fig. 1*b*. The drain currents can be given as follows:

$$I_{M11} = I_{M15} = K\left(\frac{G}{2} + \frac{I_X + I_i}{2KG}\right)^2 \quad (5)$$

$$I_{M12} = I_{M13} = I_{M14} = I_{M16} = K\left(\frac{G}{2} - \frac{I_X + I_i}{2KG}\right)^2 \quad (6)$$

The current, I_{out+}, can then be obtained as

$$I_{out+} = I_{M15} + I_{M16} = 2K\left[\left(\frac{G}{2}\right)^2 + \left(\frac{I_X + I_i}{2KG}\right)^2\right] \quad (7)$$

Similarly, I_{out-} can be written as

$$I_{out-} = I_{M25} + I_{M26} = 2K\left[\left(\frac{G}{2}\right)^2 + \left(\frac{I_X - I_i}{2KG}\right)^2\right] \quad (8)$$

By subtracting eqn. 8 from eqn. 7, a multiplier can be realised as

$$I_{out} = I_{out+} - I_{out-} = \frac{2I_X I_i}{KG^2} \quad (9)$$

The current-mode VGA can be realised by the multiplier of Fig. 1*b* and the pseudo-exponential circuit of Fig. 1*a*. Substituting eqn. 3 in eqn. 9, the characteristic function of the proposed VGA can be

$$I_{out} \cong I_i \cdot e^{\frac{I_{CTR}}{KG^2}} \quad (10)$$

where the input current is I_i and the controlled gain is $e^{(I_{CTR}/KG^2)}$.

Experimental results: The proposed current-mode multiplier and first-order pseudo-exponential circuit have been fabricated in a 0.5μm N-well CMOS process and its die photograph is shown in Fig. 2. The power supply is single, 3V, and the aspect ratios (*W*/*L*) of the PMOS and NMOS transistors are 25μm/10μm and 10μm/10μm, respectively. The experimental transfer curves of the multiplier and VGA are shown in Figs. 3 and 4, respectively. Here, the input currents were generated by AD844 [7] and off chip 3:1 current mirrors were used to match the output current of the pseudo-exponential circuit to the input of the multiplier. The experimental results exhibited a 15dB output dynamic range when the inputs were between 46μA and −40μA.

Conclusion: The proposed circuit has been fabricated in a 0.5μm N-well CMOS process. The experimental results confirm the proposed variable gain amplifier and exhibit a 15dB output dynamic range. The wider dynamic range can be achieved by using a higher-order pseudo-exponential circuit, which can be implemented by cascading the first-order pseudo-exponential circuit with squarers.

12 April 2001
Electronics Letters Online No: 20010593
DOI: 10.1049/el:20010593

C.-C. Chang, M.-L. Lin and S.-I. Liu (*Department of Electrical Engineering and Graduate Institute of Electronic Engineering, National Taiwan University, Taipei, Taiwan 10617, Republic of China*)

E-mail: lsi@cc.ee.ntu.edu.tw

References

1 HARJANI, R.: 'A low-power CMOS VGA for 50 Mb/s disk drive read channels', *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 1995, **42**, pp. 370–376
2 MOTAMED, A., HWANG, C., and ISMAIL, M.: 'A low-voltage low-power wide-range CMOS variable gain amplifier', *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 1998, pp. 800–811
3 HUANG, P.C., CHIOU, L.Y., and WANG, C.K.: 'A 3.3-V CMOS wideband exponential control variable-gain-amplifier'. Proc. IEEE Int. Symp. Circuits and Systems, 1998, Vol. 1, pp. 285–288
4 LIN, C.H., PIMENTA, T.C., and ISMAIL, M.: 'A low-voltage CMOS exponential function circuit for AGC applications'. Proc. XI Brazilian Symp. Integrated Circuit Design, 1998, pp. 195–198
5 CHANG, C.C., and LIU, S.I.: 'Current-mode pseudo-exponential circuit with tunable input range', *Electron. Lett.*, 2000, **36**, pp. 1335–1336
6 CHANG, C.C., and LIU, S.I.: 'Pseudo-exponential function using MOSFETs in saturation', *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 2000, **47**, pp. 1318–1321
7 AD844 Data sheet of Analog Devices Inc., Norwood, 1992

Fresnel region power density levels from Earth station antennas

K.M. Keen, R.C. Heron and K. Hodson

A method for predicting power density levels near transmitting parabolic Earth station antennas is described. The Fresnel region analysis applies to circular aperture antennas with an appropriate aperture amplitude distribution, and can be used to predict power densities along the antenna boresight or at off-boresight angles.