行政院國家科學委員會補助專題研究計畫成果報告

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「毫米波電路與天線II」子計畫九：
毫米波單晶電路元件之設計與模式化技術（3/3）
※ Design and Modeling Techniques of Monolithic Millimeter-Wave Components（3/3） ※
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計畫主持人：王暉　國立臺灣大學電信所教授

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毫米波單晶電路元件之設計與模式化技術（3/3）
Design and Modeling Techniques of Monolithic Millimeter-Wave Components（3/3）

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執行期限：88 年 8 月 1 日至 89 年 7 月 31 日
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一. 中文摘要（關鍵詞：毫米波、單晶毫米波積體電路、共面波導、微帶線、收發模組。）

本計畫在於研究毫米波單晶電路元件(MMIC)之設計與模式化技術。單晶電路的製程所使用的電晶體為高速場效電晶體(HEMT)，此製程可由國外的工廠提供。所研發的元件包括低雜訊放大器、功率放大器、混波器、及振盪器。

本計畫研究項目包括：開發元件模式、MMIC 設計、晶片佈局、製作與驗證。第一年度計畫以在 35 GHz 收發模組元件的研製為主，完成了微帶線設計，同時也嘗試以共面波導進行設計，而完成設計及佈局的晶片已送往代工廠實際製作。在第二年度，晶片已製作完成，並且順利完成電路的量測。除了 35 GHz 收發模組元件的研製，更高頻率的收發元件亦相繼設計完成。

Abstract（Keywords：Millimeter-wave, MMIC, HEMT, CPW, Microstrip line, Transceiver.）

This project is aimed at the development of the design and modeling techniques of monolithic millimeter-wave (MMW) components at several major frequencies, such as 35 and 60 GHz using GaAs MMIC process technologies, which are available through foreign commercial foundries. The components include low noise amplifiers, power amplifiers, mixers and oscillators.

In this two-year project, device modeling, MMIC design, chip layout, fabrication and chip evaluation were all exercised. In the first year, this project was focused on the development of 35-GHz transceiver components. Both CPW and microstrip-line components were all designed and fabricated through foreign foundries. In the second year, all the circuits were fabricated and measured successfully. Besides, the related components of higher frequency have been designed.

二. 計畫緣由與目的

Millimeter-wave (MMW) frequency (30 - 300 GHz) transceivers will play a very import role in the next generation's wireless communication systems. There are many MMW MMIC components, including low noise amplifiers, power amplifiers, mixers and oscillators reported, in US, Japan, and European countries [1]-[4] for MMW radar, communication and radiometer applications. There have been some research and development effort devoted in microwave frequency range MMICs [5]-[7] in Taiwan, but very little in MMW frequencies. The development of monolithic MMW transceiver components at several major frequencies, such as 35 and 60 GHz, were proposed in this project. Since the GaAs MMIC process technologies (e.g. 0.15 or 0.2-micron HEMT) are available through commercial foundries, the objective of this

project is to establish the design and modeling techniques for MMW MMIC using accessible MMIC processes and to train students.

Both coplanar waveguide (CPW) and microstrip-line are commonly used in MMW MMIC designs [1]-[5]. Microstrip-line designs are more conventional but require backside process, which will increase the fabrication cost and reduce the chip yield. On the other hand, CPW design does not require backside process and line-to-line coupling can be minimized due to shielding effect of ground plane around the signal lines, which can lead to a more compact design. The drawback is that the modeling library is not well established. However, the commercial EM simulation tools can be used to serve part of this requirement.

This project provides a starting point of MMW MMIC technology in Taiwan and also establishes the infra-structure in our institute.

三. 研究結果

In this project, a complete chip set for 35-GHz transceiver was developed, including low noise amplifiers, power amplifiers, mixers and oscillators. The developments and measured results of these circuits have been published in [8], [9].

The measurement results of a 35 GHz LNA have been reported in the first year. In this year, a 35 GHz driver amplifier, a mixer and an oscillator were demonstrated. In addition, one 60 GHz LNA is also designed and fabricated. Due to measurement limitation, it was measured up to 50 GHz.

Driver Amplifier Fig. 1 shows the chip photo of the two-stage driver amplifier. Small signal measured results are shown in Fig. 2. 15-dB small signal gain is measured at 31 GHz. This medium power amplifier is a two-stage single-ended microstrip-line design with output device periphery of 360 μm [10]. Optimum load at 35 GHz was determined from the device nonlinear model using harmonic balance simulation. Two devices were combined at the second stage to provide enough power and the first stage was designed to drive the second stage. Source inductance is added at driver stage for stability concern. Odd mode clamping resistor was inserted between combined devices to suppress odd mode oscillation. Out-of-band stability was improved by the resistively loaded quarter-wave-length stubs.

VCO Fig. 3 shows the chip photo of the monolithic 35-GHz VCO, with a chip size of 2.25 x 1 mm^2. Fig. 4 shows the output power and tuning range as function of bias voltage. A four-finger with 120-μm periphery PHEMT was used for the output power consideration. The VCO is a common gate design, and the oscillation frequency is tuned by the gate voltage. A pair of coupled lines were used to couple the output power to the output port and served as a dc blocking. An 11-dBm output power is measured at 34.3 GHz. The output frequency can be tuned by using the gate bias. The tuning range is 330 MHz.

Mixer Fig. 5 shows the chip photo of 35-GHz mixer, while the chip size is 1.5 x 1 mm^2. About 10.5 dB conversion loss is achieved as shown in Fig. 6. The singly balanced diode mixer was designed using microstrip-lines. The Lange coupler was selected as 90° 3-dB hybrid for bandwidth consideration. A pair of four-finger diode with 80-μm were selected. A low pass filter was designed to achieve both Lo-to-IF and RF-to-IF isolations. The return loss of LO

and RF are both better than 20 dB and isolation are better than 10 dB and 25 dB.

In addition to 35-GHz components, higher frequency transceiver components were also developed. Fig. 7 shows the chip photo of the 45 GHz one-stage LNA, while the measurement results are shown in Fig. 8. Another two-stage CPW LNA operated at 60 GHz [11] is shown in Fig. 9. Due to limited measurement capability, the frequency response is only measured to 50 GHz, as shown in Fig. 10.

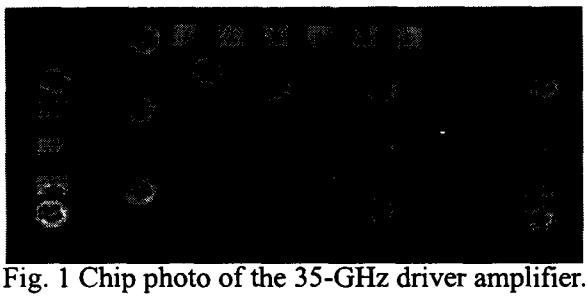

Fig. 1 Chip photo of the 35-GHz driver amplifier.

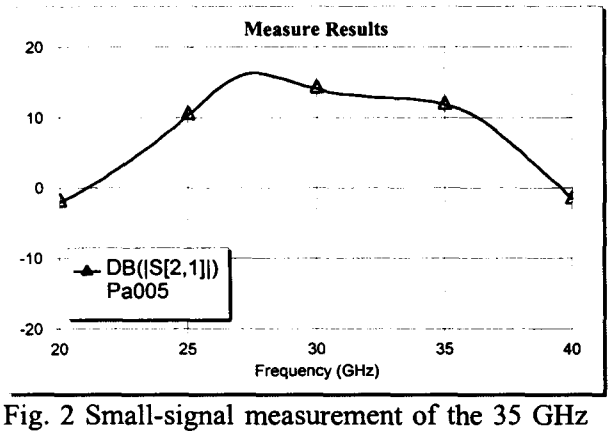

Fig. 2 Small-signal measurement of the 35 GHz driver amplifier.

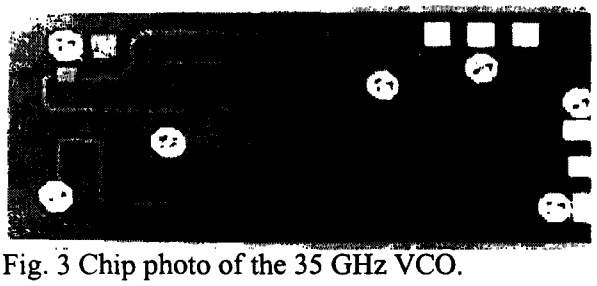

Fig. 3 Chip photo of the 35 GHz VCO.

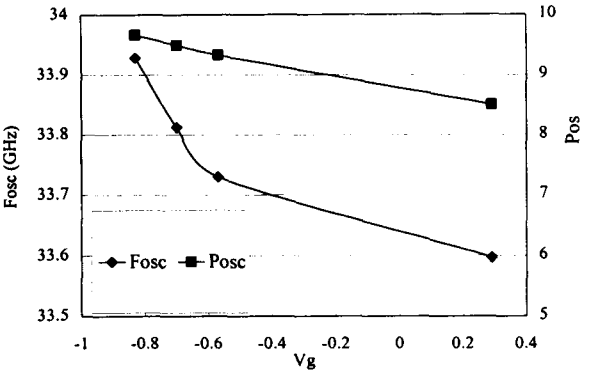

Fig. 4 Output power and tuning range as function of bias voltage of the 35-GHz VCO.

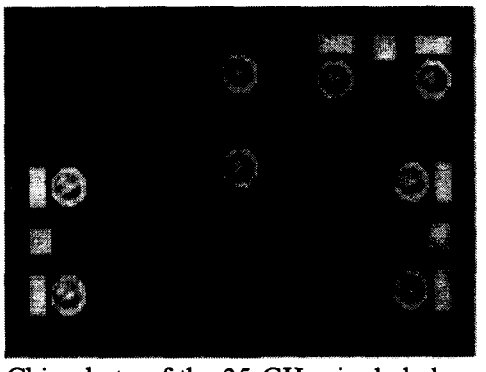

Fig. 5 Chip photo of the 35-GHz single balanced diode mixer.

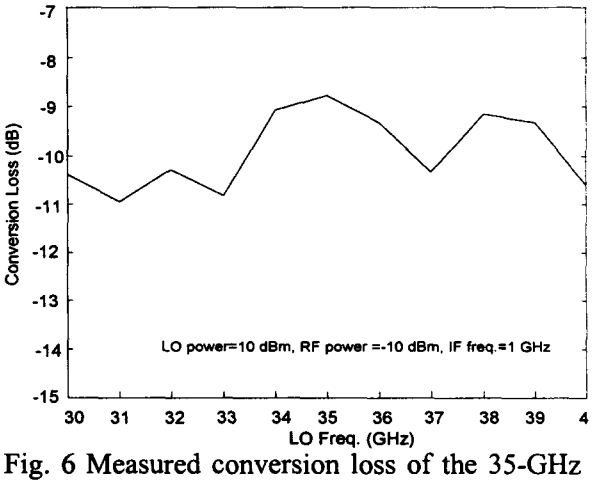

Fig. 6 Measured conversion loss of the 35-GHz mixer.

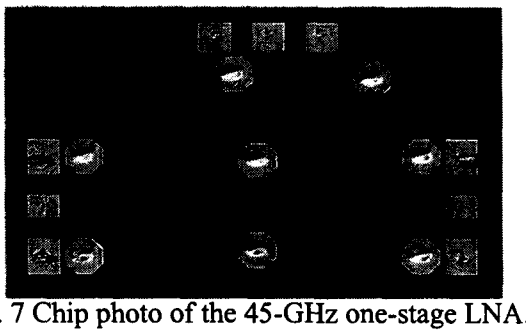

Fig. 7 Chip photo of the 45-GHz one-stage LNA.

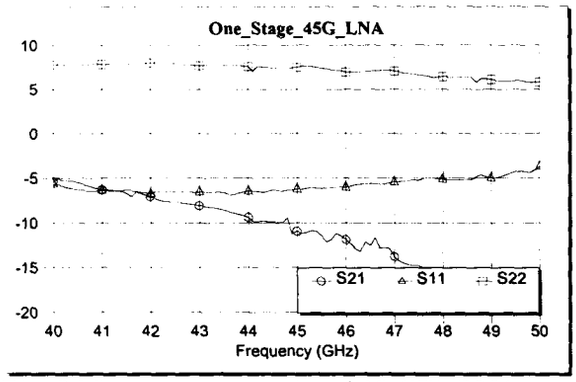

Fig. 8 Measurement results of 45-GHz LNA.

Fig. 9 Chip photo of the 60-GHz two-stage CPW LNA.

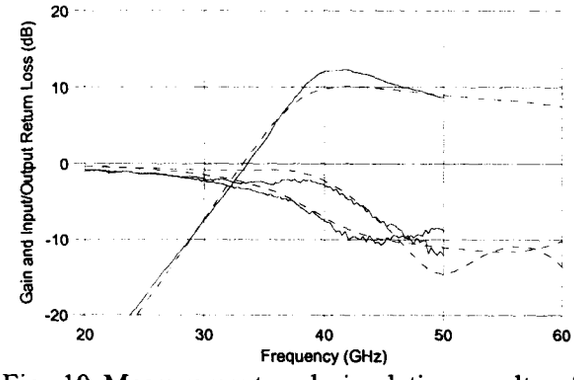

Fig. 10 Measurement and simulation results of 60-GHz LNA. (Dotted line: simulation, solid line: measurement)

四. 參考文獻

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