A New BiCMOS Increased Full Swing Converter for Low-Internal-Voltage ULSI Systems

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ABSTRACT - In this paper a new BiCMOS increased full swing inverter (IFSI) and a new BiCMOS increased full swing buffer (IFSB) for low voltage/low power ULSI (Ultra Large Scale Integration) systems are proposed. These circuits can operate at low internal voltage (V_{int}) and have low input signal swing. As long as $V_{int}>|V_t|$ (assuming $V_{tn}=-V_{tp}$), the circuits can work properly. The proposed BiCMOS IFSC circuits are suitable for high-speed operations. When the capacitor load is larger than $0.6pf$, the propagation delay and the delay power product at different internal voltages are better than previous circuits[3] under the same circuit design parameters. We also establish the relationship between the $K_r=K_n/K_p$ ratio and the circuit area. This can avoid the trial and error step in the circuit sizing operation to reduce the power consumption.

I. INTRODUCTION

Advances in the submicrometer processes make it possible to design higher density and higher speed ICs with lower supply voltages (3V or less). The trend towards low-power ULSI systems has led to new architecture considerations in [1,2]. A circuit called Increased Swing Converter (ISC) was proposed as shown in Figure 1. The detail designs of the ISC circuit as shown in Figure 1 were presented in [3] and they have zero DC current consumption at voltage ratio $V_{int}/V_{ext} < 0.4$. Figure 1(a) shows one basic design, the increased swing inverter (ISI) circuit while Figure 1(b) another design, the acc (accelerative) ISI circuit. The design in Figure 1(b) is faster than that in Figure 1(a) (about 40% faster). However, both circuits suffer two major problems. First, the voltage ratio V_{int}/V_{ext} has a lower bound ($V_{int,min}$=1.7V in [3]). Second, the propagation delay and the power consumption of the circuits increase rapidly when the V_{int} decreases.

In this paper, our new increased swing converter circuits can reduce the lower bound of V_{int}/V_{ext} to about 0.22, and still achieve higher operational speed than voltage and are faster than the circuits in [3]. Therefore, the proposed circuits are very suitable for low previous circuits with no DC current consumption. This means our circuits can be operated at lower internal voltage/low power ULSI systems.

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In the rest of this paper, we will call the increased full swing converter circuit as an "IFSC circuit" which can be implemented by the "IFSI" (increased full swing inverter) circuit or the "IFSB" (increased full swing buffer) circuit. In section 2, we will describe the impact of the K_n/K_p ratio [4,5] on a CMOS inverter of basic ISI. Based on the K_n/K_p ratios, the lower bound of the V_{int}/V_{ext} ratio and the areas of the proposeds circuits are improved. In section 3, we propose the new designs of the BiCMOS IFSC circuit. In section 4, we present the comparison results of the proposed circuits with the previous ISC by PSPICE simulation. Finally, we give our conclusions.

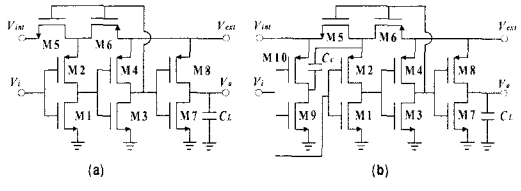

Figure 1: The implementations of ISC circuit (a) basic ISI (b) acc ISI.

II. INFLUENCE OF K_n/K_p RATIO ON BASIC ISC

The ISC circuits of Figure 1 consist of at least four stages of CMOS inverters. The first two stages(M1, M2, M3, and M4) and feedback stage(M5, M6) are the most critical stage. The goal is to design these circuits to have very low internal voltage and very low input voltage swing. Therefore, we redraw the input inverter stage and its transfer curve as shown in Figure 2.

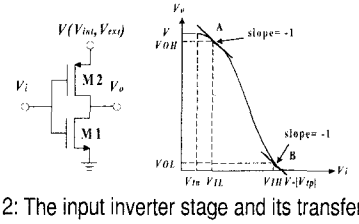

Figure 2: The input inverter stage and its transfer curve.

As we shall see, the ratio K_n/K_p is very important in the design for increased voltage swing. In Figure 2, if V_i is increased to V_{IL}, M1 is in the saturation region and M2 is in the triode region. We can determine (assume $V_{tn}=-|V_{tp}|$) as following:

$$V_{IL} = (V - V_t) - (V - 2V_t)(\frac{K_r}{K_r + 2})^{1/2} \quad (1)$$

$$V_{OH} = V_{IL}(K_r + 1) - V_t(K_r - 1) \quad (2)$$

where $K_{n,p} = \frac{\mu_{n,p}}{2} C_{OX} \frac{W_{n,p}}{L_{n,p}}$, and $K_r = \frac{K_n}{K_p}$

Similarly, if M1 is in the triode region and M2 in the saturation region, we can derive

$$V_{IH} = V_t + \frac{V - 2V_t}{(2K_r + 1)^{1/2}} \quad (3)$$

$$V_{OL} = \frac{V_{IH}(K_r + 1) - V_t(K_r - 1) - V}{K_r} \quad (4)$$

From (1) to (4), we have the relationships of the transition voltages *VIH*, *VIL*, *VOL*, and *VOH* to the ratio *Kr*. The CMOS inverter of basic ISI transition occurs at different transition points which can be estimated by (1) through (4) with first order approximation as shown in Figure 3 (assume $|V_t|$=1V, *V*=5V).

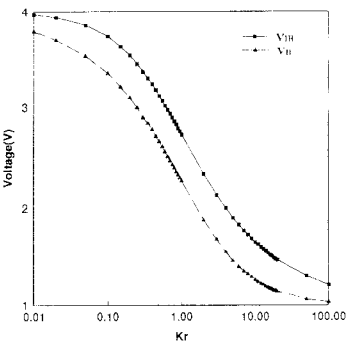

Figure 3: The relationship between *Kr* and the transition voltage.

From Figure 3 we can realize easily that the larger the *Kr*, the smaller the *VIL* and *VIH*. We can also find the transition point for different *Kr* rather easily. If we decrease the input voltage swing, we have to increase *Kr* because the increase of *Kr* will reduce the transition point voltage to assure the success of the reduced input voltage swing transition. However, there are more to be considered, otherwise the transition may not be successful because the equations (1) to (4) have restricted the range of *Kr* implicitly. We can also use the same concept to trade off the area and the input swing voltage as described above when the area is critical. In the Figure 1(a), if the voltage at the source of M2 is equal to *Vint* and *Vint* becomes smaller, we can see that the *Kr* in the second stage of Figure 1(a) must be large enough to ensure the occurrence of transition from Figure 3. However, as the *Vint* becomes smaller, the second stage will consume larger power. Besides, the lower the *Vint*, the longer the transition delay of Figure 1(a). Figure 1(b) has smaller transition delay but more power consumption. This is because the increased stage will consume more power.

III. CIRCUIT ANALYSIS AND OPERATION

A. New Implementation

To improve the circuits in Figure 1, we propose a new design as shown in Figure 4. The improvement is made by deleting one transistor (transistor M5) from the circuit in Figure 1(b). The transistor M11 acts as a capacitor. The basic operations of the two circuits are similar [3]. However, the new proposed circuit may take less area than the circuit in Figure 1(b). In the following discussion, we will focus on how and why the new circuit outperforms the previous one.

We redraw as a comparison parts of the circuits of Figure 1(b) and Figure 4 in Figure 5(a) and Figure 5(b), respectively. The voltage at B is higher than the voltage at A since M5 is connected to *Vint*. The circuit in Figure 1(b) is one conduction path more than the new implementation in Figure 4. Thus, Figure 5(a) needs more transition current and consumes more power than Figure 5(b).

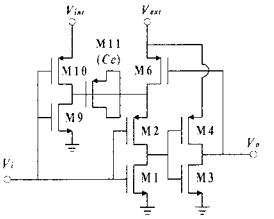

Figure 4: The new implementation.

During the transition, the voltage swing of Figure 5(b) is faster than that of Figure 5(a) because a portion of the total current is consumed by M5. The fact that the voltage at A is lower than that at B also makes the point A drive the next stage more slowly than the proposed circuit under the same *Kr* consideration as explained in the previous section. At the same time, the *Vint* of the proposed circuit can be reduced to the threshold voltage due to the existence of the coupling capacitance *CC* and still maintain the DC operation. The existence of *CC* can provide a dynamic boost to reduce the transition time and make the circuit in Figure 5(b) a high impedance path. For the circuit in Figure 5(a), if M5 is off, it is also a high impedance path. But when M5 is switched on and since it is connected in parallel to R9, R10 and *CC* as shown in Figure 5(a), the whole equivalent circuit becomes a low impedance path. Therefore, the *Vint* in Figure 5(a) must be higher than that in Figure 5(b) to ensure that the circuit can drive A to a voltage same as B during transition. Thus, with the same area, both the power consumption and the speed performance of the new implementation are better than those of the acc ISI. Especially, the power consumption of the new implementation is reduced by the transistor M5. Furthermore, this new circuit has no power consumption on the branch of *Vext* to *Vint*, which consumes much power than the branch of *Vint* to ground. This advantage will be more obvious when *Vint* becomes smaller. Thus, the new implementation can perform

faster and still reduce the power consumption.

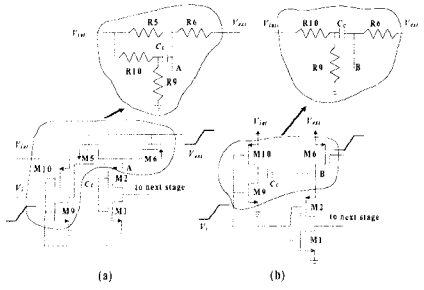

Figure 5: The feedback circuit and the input CMOS inverter stage.

B. The Proposed Circuits

For large output capacitance load, we use the concept above to propose the BiCMOS IFSI and the BiCMOS IFSB as shown in Figure 6. The activities of M1 - M11 are the same as the new implementation counterpart, and the output stage (M14 - M15, Q1, and Q2) is almost the same as the normal BiCMOS output stage to increase the output drive capacity. However, we add the transistor M12 to charge the output voltage to V_{ext} and M13 to discharge the output to ground. The full swing BiCMOS ISI and ISB have much lower propagation delay and lower delay power product than the basic ISI and acc ISI circuits under large output capacitance load.

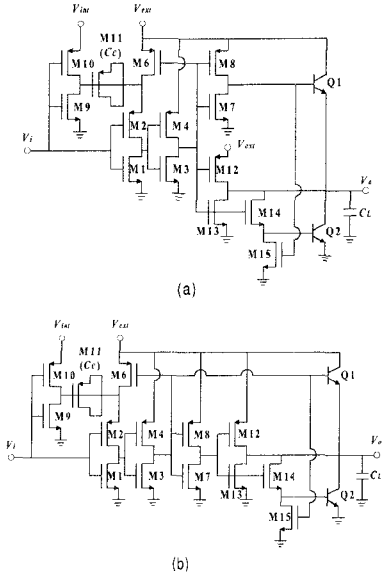

Figure 6: The full swing BiCMOS ISC (a) BiCMOS IFSI (b) BiCMOS IFSB.

IV. SIMULATION RESULTS AND COMPARISONS

We compare the two previous circuits (basic ISI and acc ISI) and the two proposed circuits by PSPICE. The parameters are shown in Table I. Table II shows the transistor sizes for equal comparison. The size of M8 in the basic ISI and the acc ISI is lager than other transistors because this transitor needs to provide larger fanout ($C_L \geq 1pf$).

Figure 7 shows the simulation results of the transmission delay versus the load capacitance (C_L) as V_i switches from 0V to 1.5V (V_{int}=1.5V). The delay times of these circuits are measured as the average of rise time and fall time from $V_I=V_{int}/2$ to $V_O=V_{ext}/2$ for square waveform at 25MHz. Increasing the load capacitance will increase the transmission delay. As shown in the circuit simulation, the proposed BiCMOS IFSI and IFSB have higher performance than the basic ISI and the acc ISI circuits for larger output load as expected.

We can see the superior drive capacity of the proposed BiCMOS version is the best of all the CMOS ISI circuits. In the proposed BiCMOS circuit, the output stage consists of two NPN BJT. However, we deliberately design these two transistors so that they will be turned on at different points of time and consequently, the short circuit current can be avoided. Therefore, the BiCMOS version has a little more power consumption than the previous CMOS version.

Table I: The PSPICE device parameters for CMOS and BiCMOS technologies.

CMOS				Voltage				Bipolar			
L	*Vtn*	*Vtp*	*tox*	*Cjp*	*Cjn*	*Vext*	*β*	*Ic*	*Cjc*	*Cje*	*Ccs*
μm	*V*	*V*	*nm*	*μF*	*μF*	*V*		*mA*	*fF*	*fF*	*fF*
0.8	0.75	-0.9	19	595	350	5	100	1.5	40	40	50

Table II: The transistor sizes of circuits.

Transistor	basic ISI	acc ISI	BiCMOS IFSI	BiCMOS IFSB
M1	8/0.8	8/0.8	8/0.8	8/0.8
M2	3.2/0.8	3.2/0.8	3.2/0.8	3.2/0.8
M3	8/0.8	8/0.8	8/0.8	8/0.8
M4	3.2/0.8	3.2/0.8	3.2/0.8	3.2/0.8
M5	8/0.8	8/0.8		
M6	3.2/0.8	3.2/0.8	3.2/0.8	3.2/0.8
M7	8/0.8	8/0.8	3.2/0.8	3.2/0.8
M8	16/0.8	16/0.8	8/0.8	8/0.8
M9		8/0.8	8/0.8	8/0.8
M10		3.2/0.8	3.2/0.8	3.2/0.8
M11		8/8	8/8	8/8
M12			3.2/0.8	3.2/0.8
M13			8/0.8	8/0.8
M14			8/0.8	8/0.8
M15			1.6/0.8	1.6/0.8

From Figure 7, we can see that the proposed BiCMOS ISFC circuit has the highest speed, but the worst power performance. However, this BiCMOS IFSC circuit has the best delay power product among all the circuits considered.

We also compare the transmission delay at different internal voltages as shown in Figure 8. Figure 8 shows that both the new BiCMOS IFSI and the new BiCMOS IFSB are faster than the acc ISI and the basic ISI.

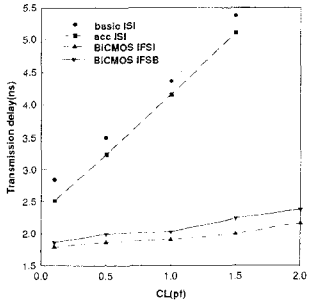

Figure 7: The transmission-delay versus the load capacitance.

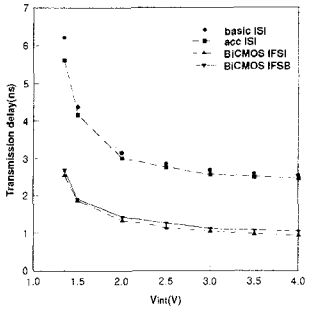

Figure 8: The transmission delay versus Vint with CL=1*pf*.

Figure 9 shows the delay power product at different internal voltages by different circuits. Although the proposed circuits consume the most power, their delay power products are the least among all the circuits.

We also compare the frequency responses between the new full swing BiCMOS ISC and the acc ISI as shown in Figure 10. The new full swing BiCMOS ISC is faster than the acc ISI at frequencies below 100 MHz. At frequencies higher than 100MHz, the proposed circuits can still work while the acc ISI can not.

V. CONCLUSIONS

In this paper we proposed a new BiCMOS IFSI and a new BiCMOS IFSB circuits. These circuits can get full swing output with low internal voltage *Vint* and low input signal swing. Even under the condition of $Vint > |Vt|$, the proposed circuits still work properly. These circuits are less constrained by the voltage ratio *Vint/Vext* than the circuits in [3] and also consume no DC current. The previous circuits in [3] can be modified to get the same *Vint/Vext* lower bound as the proposed circuit, however, they will cost a lot more area. The new proposed circuits have higher speed, lower delay power product and larger frequency response compared with the acc ISI circuit. When the capacitor load of the new BiCMOS IFSC circuit is larger than 0.6*pf*, the propagation delay and the delay power product of the proposed circuits at various internal voltages are better than those of the previous circuits[3]. Thus, the proposed circuits are very suitable for high speed and low voltage/low power applications.

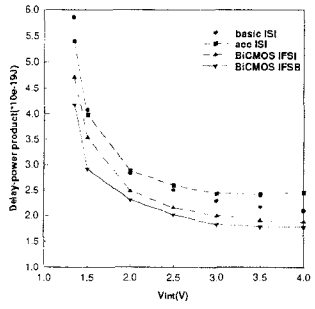

Figure 9: The delay-power product versus *Vint* with *CL*=1*pf*.

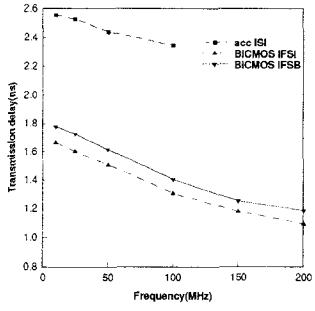

Figure 10: The transmission delay versus frequency (*Vint*=1.5V,*CL*=0.1*pf*).

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