

Reliability Improvement of Rapid Thermal Oxide Using Gas Switching

Min Hung Lee, Cheng-Ya Yu, Fon Yuan, K.-F. Chen, Chang-Chi Lai, and Chee Wee Liu, *Senior Member, IEEE*

Abstract—The instantaneous switch-off of the gas precursors during the ramp-down cycle in a spike ramp process is demonstrated to be an effective method to enhance the reliability of rapid thermal oxide. Due to the slow ramp-down rate ($60\text{ }^{\circ}\text{C/s}$ – $90\text{ }^{\circ}\text{C/s}$) of a rapid thermal process, the oxidation during the slow ramp-down cycle may produce the inferior oxide, especially for ultrathin oxide. To avoid the oxidation in the slow ramp-down cycle, the oxidation precursor (oxygen) is switched off during the ramp-down cycle. The reliability of resulting oxide without oxidation during the ramp-down cycle is enhanced as compared with the conventional oxide, which is still oxidized during the ramp-down cycle.

Index Terms—Gas switching, rapid thermal oxidation, reliability, spike ramp.

I. INTRODUCTION

THE SCALING of nano-devices reaches the gate oxide thickness 1 nm for the 45-nm technology node [1]. The precise control of the thickness and the quality of the oxide layer is a crucial factor for the performance of the MOS devices. Recently, the spike ramp process in a rapid thermal processor (RTP) is reported to effectively reduce the thermal budget as compared with the conventional furnace process [2]–[6]. The dopant out-diffusion during thermal activation annealing was minimized in shallow junction formation [3]. The ramp-up rate of a rapid thermal process is around $50\text{ }^{\circ}\text{C/s}$ – $400\text{ }^{\circ}\text{C/s}$ [6], and is controlled by the lamp power, the number of the lamps, and the reflector configuration [7]. For the cooling stage, the gas flows, chamber geometry, and physical characteristics of wafers all are important factors to determine the cooling rate. The nature and unforced ramp-down rate is about $60\text{ }^{\circ}\text{C/s}$ – $90\text{ }^{\circ}\text{C/s}$ [8]. This slow ramp-down rate increases the thermal budget and deteriorates the merit of the spike ramp process. The extra dopant diffusion in RTA and the inferior oxide formation in RTO occur during the ramp-down cycle. The additional growth of oxide during the ramp-down time for spike oxidation process becomes significant, especially for ultrathin oxide due to the fast diffusion through the ultrathin oxide. It has been reported that the spike oxidation process results in the increase of interface state density [9]. Since the interface state density increases with the decreasing oxidation temperature [10], the growth of low-temperature oxide near the Si/SiO₂ interface during the ramp-down time may be responsible for the increase of interface state density. The final formation of SiO₂ layer locates at Si/SiO₂ interface [11] and, therefore,

the final oxidation conditions are crucial for the Si/SiO₂ interface quality. To avoid oxidation in the slow ramp-down cycle, we have investigated the novel process to switch off the oxidation precursor (oxygen) during the ramp-down time and the reliability of the resulting oxide is enhanced.

II. EXPERIMENT

In the RTO system, the 4-in p-type wafer was illuminated by 12 tungsten halogen lamp tubes through a quartz window with stainless-steel chamber, was held by three quartz pins in order to reduce thermal stress and wafer slip. The wafer temperature was monitored by pyrometry with a closed-loop control. The precursor gas, which is controlled by mass flow controller (MFC), was injected horizontally across the wafer, and is exhausted by a mechanical pump. The advantages of MFC are the precise flow rate control and the abrupt switch of the gas precursor. With the size of 270 cm³ in our chamber, and oxygen flow rate of 1000 sccm at the pressure of 250 mbar, $\sim 4\text{ s}$ is more enough to replace the gas species completely. The pressure in chamber was maintained by mechanical pump and was regulated by a throttle valve. The gate oxide thickness was measured by ellipsometry. The resistivity of the wafers is 1–10 $\Omega\cdot\text{cm}$. NMOS diodes have Al gate electrodes with circular area of $5 \times 10^{-5}\text{ cm}^2$ defined by photolithography. The constant voltage stress (CVS) measurements were carried out using an HP 4156A semiconductor parameter analyzer.

Before oxidation, the wafer was cleaned by a HF dip. An *in situ* hydrogen prebake at 1000 $^{\circ}\text{C}$ for 2 min at the pressure of 250 mbar was performed before the growth of the ultrathin oxide. After the growth of ultrathin oxide, the sample was *in situ* annealed subsequently in hydrogen and in nitrogen for 10 min each at 900 $^{\circ}\text{C}$ at the pressure of 250 mbar. The ultrathin gate oxide of the NMOS diode was grown by RTO at the reduced pressure of 250 mbar with 1000 sccm nitrogen and 1000 sccm oxygen flows. The temperature ramp and oxygen flow rate profile were shown in Fig. 1. The flow rate can switch much faster than the temperature. The oxidation time is determined by gas switching. For “overall oxidation,” the oxygen continuously flows in the entire thermal cycle, as shown in Fig. 1. For “ramp-up oxidation,” the oxygen flows only during the temperature rising cycle and is switched off during the ramp-down cycle.

III. RESULTS AND DISCUSSION

The ultrathin gate oxide of the NMOS diode was grown by RTO with the spike ramp oxidation process at various peak temperatures from 800 $^{\circ}\text{C}$ to 1000 $^{\circ}\text{C}$. Fig. 2 shows the statistic

Manuscript received January 9, 2002; revised July 11, 2003.

The authors are with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. (e-mail: chee@cc.ee.ntu.edu.tw).

Digital Object Identifier 10.1109/TSM.2003.818982

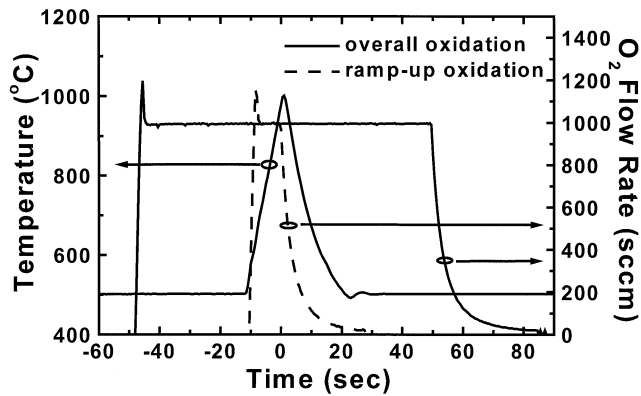


Fig. 1. The temperature and oxygen flow rate profiles of overall oxidation and ramp-up oxidation processes. The solid line indicates that the oxygen continuous to flow during overall the spike ramp oxidation process. The dash line indicates that the oxygen is switched off instantaneous at the beginning of the ramp-down cycle (ramp-up oxidation). Note that both process have the same temperature profile.

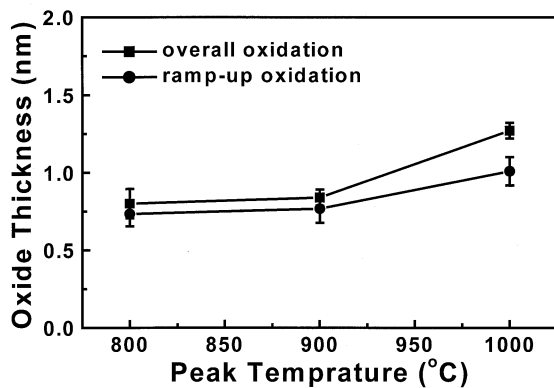


Fig. 2. The statistic average thickness of the oxide prepared by overall oxidation and ramp-up oxidation. The extra oxidation time during the ramp-down cycle leads to the thicker oxide thickness of overall oxidation as compared with ramp-up oxidation. As the peak temperature increases, the significant average thickness difference is observed due to the increasing thermal budget of the extra ramp-down cycle.

average thickness of the oxide prepared by overall oxidation and ramp-up oxidation. In the overall oxidation process, the extra oxidation time during the ramp-down cycle leads to the thicker oxide thickness as compared with the ramp-up oxidation process. As the peak temperature increases, the significant average thickness difference is observed due to the increasing thermal budget of the extra ramp-down cycle. The reliability measurement is performed by CVS, since the wear-out and breakdown are mainly controlled by the gate voltage, which determines the injected electron energy [12].

Figs. 3 and 4 show the gate current variation as a function of stress time of NMOS diodes with oxide grown at peak temperature of 1000 °C and 900 °C for both processes, respectively. Both devices are designed to have similar oxide thickness for each growth peak temperature ($T_{ox} \sim 1.2$ nm in Fig. 3 and $T_{ox} \sim 1$ nm in Fig. 4) and are stressed under the CVS at -1, -2, and -3 V for stressing time of 1000 s. We have obtained similar trend of the stress-induced leakage current (SILC) results with over 20 devices for reproducibility. There is no apparent fluctuation in gate current during the stress for both the ramp-up oxida-

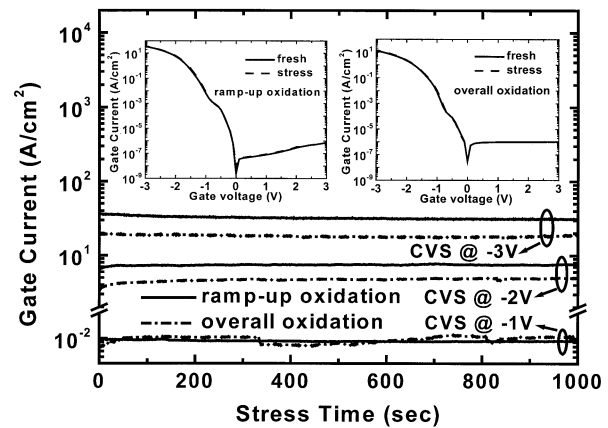


Fig. 3. The gate current versus stress time plot of the both NMOS diodes for overall oxidation and ramp-up oxidation at the peak temperature of 1000 °C, with the oxide thickness of ~ 1.2 nm under CVS at $V_g = -1, -2$, and -3 V for 1000 s. The insets are the I - V characteristics of the devices before and after stress at -1 V. (left: ramp-up oxidation; right: overall oxidation.)

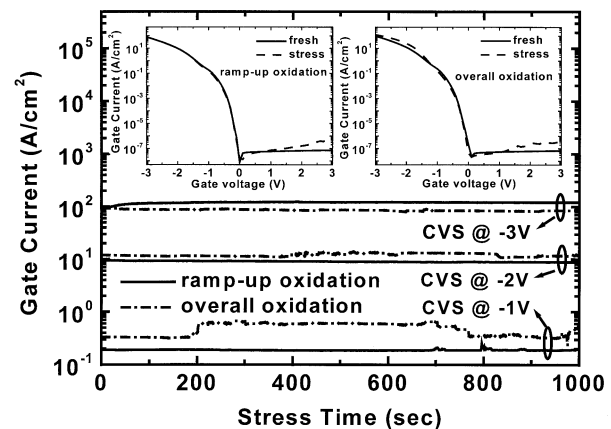


Fig. 4. The CVS measurement under $V_g = -1, -2, -3$ V for 1000 s for overall oxidation and ramp-up oxidation at the peak temperature of 900 °C grown oxide. The oxide thickness is ~ 1 nm. The insets are the I - V characteristics of the devices before and after stress at -1 V. (left: ramp-up oxidation; right: overall oxidation.)

tion and overall oxidation devices except the overall oxidation devices under CVS at -1 V in Fig. 3. This indicates that the ramp-up oxidation devices have superior oxide reliability characteristics as compared with the overall oxidation devices. It is found that the SILC at higher voltage (-3 V) for the ramp-up oxidation devices is high as compared with overall devices due to the slightly lower oxide thickness in the ramp-up oxidation process. After 1000 s CVS at -1 V, the current-voltage (I - V) curves of both devices are almost identical to the fresh one, as shown in the insets of Fig. 3. Note that there is a kink at ~ -1 V in the I - V curves of the NMOS devices, indicating the transition of two current-transport mechanisms. At the small negative gate voltage, the electrons can tunnel through the gate oxide via the interface traps at Si/SiO₂ interface [13]. At the larger negative gate bias, the electrons tunnel directly into the conduction band of Si. The overall oxidation devices grown at peak temperature of 1000 °C show inferior and degradation of interface state from Fig. 3, although it is difficult to obtain the exact value of interface state density (D_{it}) for the ultrathin oxide due to the high gate leakage current through the NMOS diodes.

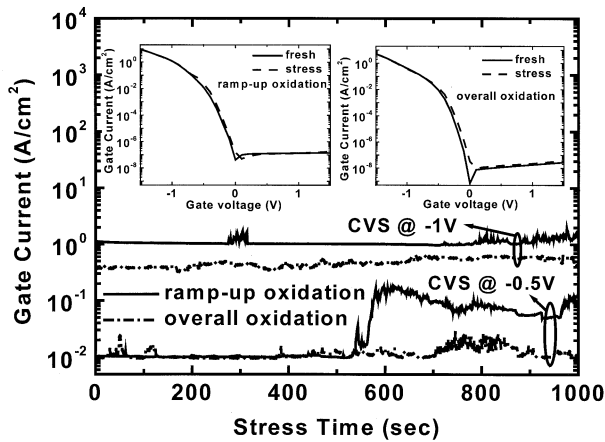


Fig. 5. The CVS measurement under $V_g = -0.5$ and -1 V for 1000 s for overall oxidation and ramp-up oxidation at peak temperature 800°C grown oxide. The oxide thickness is ~ 0.8 nm. The insets are the I - V characteristics of the devices before and after stress at -1 V. (left: ramp-up oxidation; right: overall oxidation).

For reference, the D_{it} values of the thickness oxide (~ 5.2 nm) for the without-ramp-down oxidation, and overall oxidation are 1.7×10^{11} and $2.6 \times 10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$, respectively. This implies that the overall oxidation oxide probably has higher D_{it} than the ramp-up oxidation oxide for ultrathin oxide. The large D_{it} can yield larger electron current tunneling through the oxide via interface states. This trap-assisted tunneling current may be responsible for the oxide degradation. The similar results are also obtained as the growth peak temperature of 900°C as shown in Fig. 4. Since the lower temperature oxidation (900°C) forms inferior oxide and high D_{it} [10], the ramp-up oxidation devices show gate current at about 700 s and 800 s under CVS at -1 V with a little fluctuation as compared with overall devices. There are apparent fluctuation in gate current for the overall oxidation devices with stress at -1 and -2 V, and this indicates the inferior oxide reliability and D_{it} of the overall oxidation process. The higher accumulation tunneling current of overall oxidation devices indicates the devices degradation after the 1000-s CVS at -1 V (the right inset of Fig. 4). However, this gas switching effect is not apparent for peak growth temperature of 800°C , to be discussed.

Fig. 5 shows the CVS measurements for 1000 s at $V_g = -0.5$ and -1 V of the devices with the oxide grown at peak temperature of 800°C ($T_{ox} \sim 0.8$ nm). The gas switching effect does not improve the reliability for both devices in the peak temperature of 800°C oxidation process. Since both devices show similar gate current fluctuation during the stress, and the devices are degraded after the 1000 s CVS at -1 V (the insets of Fig. 5). Besides, the gas switching effect was also studied for the thick oxide devices, which are grown by convention RTO at the temperature of 1000°C with 70-s plateaus oxidation. Fig. 6 shows the temperature ramp and oxygen flow rate profiles of overall oxidation and without-ramp-down oxidation processes. The both devices with similar oxide thickness ($T_{ox} \sim 5.2$ nm) are stressed under 200 s CVS at $V_g = -7.5$ V as shown in Fig. 7. The mid-bandgap D_{it} values are 1.7×10^{11}

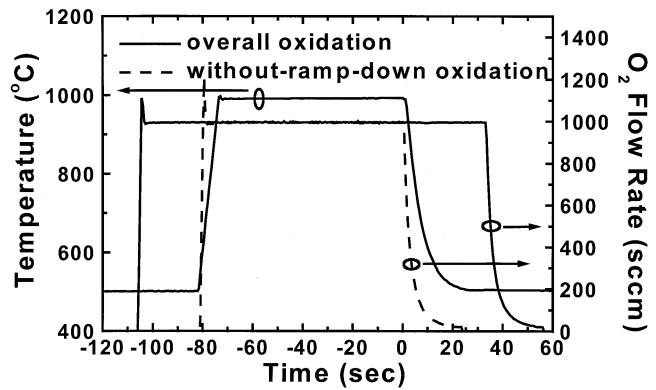


Fig. 6. The temperature and oxygen flow rate profiles of overall oxidation and without ramp-down oxidation processes. The temperature ramp profile is the conventional RTO at the temperature of 1000°C with 70-s plateaus. The solid line indicates that oxygen continuous to flow during overall oxidation process. The dash line indicates that the oxygen is switched off instantaneous at the beginning of the ramp-down cycle called "without-ramp-down oxidation."

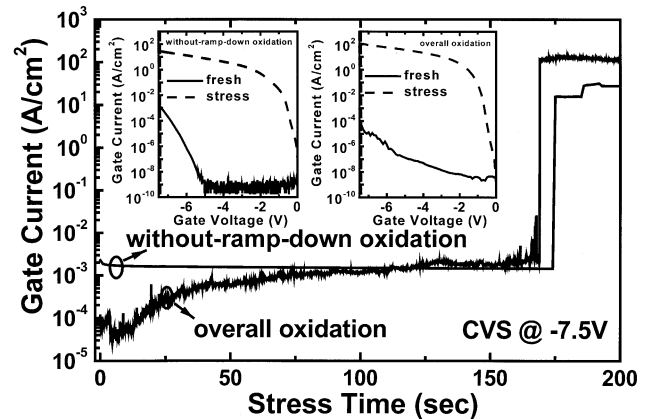


Fig. 7. The CVS measurement under $V_g = -7.5$ V for 200 s for overall oxidation and without ramp-down oxidation processes at temperature 1000°C grown oxide. The oxide thickness is 5.2 nm. The insets are the I - V characteristics of the devices before and after stress. (left: without-ramp-down oxidation; right: overall oxidation).

and $2.6 \times 10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$ for without-ramp-down oxidation and overall oxidation devices, respectively, extracted by Terman method [14]. This is corroborating with the results as discussed in Figs. 3–5. Furthermore, the I - V curve of overall oxidation before the stress (the right inset in Fig. 7) also exhibits serious leakage current, as compared with the without-ramp-down oxidation. Note that, there is apparent fluctuation in gate current before hard breakdown for the overall oxidation devices in Fig. 7. The current fluctuation is related with an oxide trap-assisted tunneling mechanism at the Fowler–Nordheim (FN) bias ($V_g = -7$ V), previously reported in [15]. The hard breakdown of oxide occurs under CVS, which is identified by an abrupt and dramatic increase of the leakage current, and the injection fluence (Q_{BD}) values are similar (about $10^{-1} \text{ coul/cm}^2$) for both devices. The value is consistent with the extrapolating of data reported in [16]. Due to no statistic data on Q_{BD} can not be concluded. However, the hard breakdown does not occur in the ultrathin oxide devices, the Q_{BD} is not important in the modern VLSI devices.

IV. CONCLUSION

We have demonstrated the reliability improvement by gas switching, which controls oxidation time in spike ramp oxidation process. The oxygen is switched off instantaneously at the beginning of the ramp-down cycle to avoid inferior oxide formation. The gas switching can enhance the oxide reliability at the spike ramp oxidation temperature of 1000 °C and 900 °C, and its effect is not apparent at 800 °C since the low-temperature oxidation (800 °C) forms inferior oxide and higher interface state density. The gas switching can also improve the oxide leakage current and reduce interface state density for thick oxide. This simple technique can easily improve oxide quality with spike ramp oxidation for reducing thermal budget.

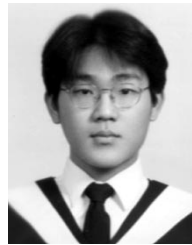
REFERENCES

- [1] "The International Technology Roadmap for Semiconductors," Semicond. Industry Assoc., 2002.
- [2] S. Shishiguchi, A. Mineji, T. Y. Matsuda, and H. Kitajima, "Shallow junction formation by low energy implant and high ramp-up rate RTA process," in *Proc. Electrochem. Soc. Symp.*, vol. 99–10, 1999, pp. 105–116.
- [3] M. Mehrotra, J. C. Hu, A. Jain, W. Shiau, S. Hattangady, V. Reddy, S. Aur, and M. Rodder, "A 1.2 V, sub-0.09 μm gate length CMOS technology," in *IEDM*, 1999, pp. 419–422.
- [4] A. Agarwal, A. T. Fiory, H. J. L. Gossmann, C. S. Rafferty, and P. Frisella, "Ultra-shallow junction formation by spike annealing in a lamp-based or hot-walled rapid thermal annealing system: Effect of ramp-up rate," in *Proc. Mater. Sci. Semiconduct.*, vol. 1, 1998, pp. 237–241.
- [5] E. J. H. Collart, G. de Cock, A. J. Murrel, and M. A. Foad, "Characterization of low energy boron implantation and fast ramp-up rapid thermal annealing," in *Proc. Mater. Res. Soc. Symp.*, vol. 525, 1998, pp. 227–235.
- [6] S. Shishiguchi, A. Mineji, T. Matsuda, and S. Saito, "Boron implanted shallow junction formation by high-temperature/short-time/high-ramping-rate (400°C/sec) RTA," in *Proc. VLSI Tech. Symp.*, 1997, pp. 89–90.
- [7] J. M. Dilhac, N. Nohier, C. Ganibal, and C. Zanchi, "Thermal modeling of a wafer in a rapid thermal processor," *IEEE Trans. Semiconduct. Manufact.*, vol. 8, pp. 432–439, Nov. 1995.
- [8] M. H. Lee and C. W. Liu, "A novel illuminator design in a rapid thermal process," *IEEE Trans. Semiconduct. Manufact.*, vol. 14, pp. 152–156, May 2001.
- [9] A. T. Fiory, "Growth of thin SiO_2 by "spike" rapid thermal oxidation," in *Proc. Mater. Res. Soc. Symp.*, vol. 567, 1999, pp. 13–19.
- [10] H. Fukuda, T. Arakawa, and S. Ohno, "Thin-gate SiO_2 films formed by *in situ* multiple rapid thermal processing," *IEEE Trans. Electron Devices*, vol. 39, pp. 127–133, Jan. 1992.
- [11] B. E. Deal and A. S. Grove, "General relationship for the thermal oxidation of silicon," *J. Appl. Phys.*, vol. 36, no. 12, pp. 3770–3778, 1965.
- [12] M. H. Lee, C.-H. Lin, and C. W. Liu, "Novel methods to incorporate deuterium in the MOS structures," *IEEE Electron Device Lett.*, vol. 22, pp. 519–521, Nov. 2001.
- [13] A. Ghetti, E. Sangiorgi, J. Bude, T. W. Sorsch, and G. Weber, "Low voltage tunneling in ultra-thin oxides: A monitor for interface states and degradation," in *IEDM*, 1999, pp. 731–734.
- [14] D. K. Schroder, *Semiconductor Material and Device Characterization*. New York: Wiley, 1990, ch. 6.
- [15] E. Miranda, J. Sune, R. Rodriguez, M. Nafria, X. Aymerich, L. Fonseca, and F. Campabadal, "Soft breakdown conduction in ultrathin (3–5 nm) gate dielectrics," *IEEE Trans. Electron Device*, vol. 47, pp. 82–89, Jan. 2000.
- [16] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge, U.K.: Cambridge Univ. Press, 1998, ch. 2.



Min Hung Lee received the B.S. degree in physics from National Chungshin University, Taichun, Taiwan, in 1996, and the M.S. degree in physics, and the Ph.D. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 1998 and 2002, respectively.

He is an Engineer with the Electronics Research & Service Organization, Industrial Technology Research Institute (ERSO/ITRI), Hsinchu, Taiwan. His current research interests include RTCVD, strained-Si, SiGe, and SiC MOSFET.

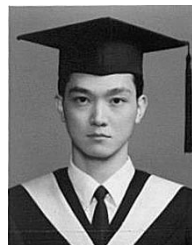


Cheng-Ya Yu received the B.S. degree in electrical engineering from National Sun Yat-sen University (NSYSU), Kaohsiung, Taiwan, in 1998. He is currently pursuing the Ph.D. degree in the Graduate Institute of Electronics Engineering, National Taiwan University (NTU), Taipei, Taiwan. His research interests include rapid thermal process, and direct wafer bonding and layer transfer technologies and their applications.



Fon Yuan received the B.S. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2001. He is currently working towards the Ph.D. degree in the Department of Electrical Engineering and Graduate Institute of Electronics Engineering, NTU.

K.-F. Chen, photograph and biography not available at the time of publication.



Chang-Chi Lai received the B.S. degree in electrical engineering from National Chen Kung University, Tainan, Taiwan, in 1999, and the M. S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2002.

He is an Integrated Circuit Design Engineer with Microelectronics Corporation, Science-Based Industrial Park, Hsinchu City, Taiwan.



Chee Wee Liu (M'99–SM'00) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1985 and 1987, respectively, and the Ph.D. degree in electrical engineering from Princeton University, Princeton, NJ, in 1994.

From 1994 to 1996, he was an Associate Professor at National Chungshin University, Taichun, Taiwan. He is currently a Professor at National Taiwan University. His current research interests include CMOS optoelectronics, optical interconnects, MOSFET devices, SiGe high-speed HBT devices, and rapid thermal process. He invented the first MOS tunneling light-emitting diode and photodetector and owns two patents on photodetectors.