K-Band Monolithic GaAs PHEMT Amplifiers

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This paper presents the designs and measurement results of several K-band monolithic microwave integrated circuits (MMIC) including 21-26 GHz amplifiers and 2-25 GHz distributed amplifiers. The MMIC chips are fabricated with a 0.2-μm gate-length pseudomorphic (PM) GaAs-based HEMT MMIC technology, carried out by commercially available foundry.

1 Introduction

Microwave amplifiers are very important components of the RF front-end for transceiver applications. As the wireless communications become more and more popular, the application frequency is moving toward higher frequency range such as K-band (18-27 GHz) or above due to the crowdness of low frequency spectrum. This paper presents the development of 21-26 GHz low noise amplifiers (LNAs), medium power amplifiers (PAs) and 2-25 GHz distributed amplifiers (DAs). Both microstrip line and grounded coplanar waveguide (GCPW) are used for the designs. These MMIC chips are fabricated using a commercial 0.2-μm pseudomorphic (PM) GaAs-based HEMT technology foundry process.

The two-stage LNA demonstrated a measured small signal gain of 16.4 dB at 24 GHz, the two-stage balanced PA has a measured small signal gain of 17 dB at 24 GHz. The DAs using microstrip line and GCPW have measured small signal gain of 11.5±2.4 dB from 2-25 GHz and 10±0.1 dB from 2-30 GHz, respectively.

2 HEMT Device Characteristic and MMIC Technology

The GaAs-based pseudormorphic HEMT (PHEMT) MMIC process foundry service is provided by Philips Microwave Limeil, France [1]. The device is a 0.2-μm gate-length low noise PHEMT with a maximum unit current gain frequency (f_T) of 53 GHz. The drain current at peak transconductance under 3-V drain bias is 208 mA/mm. The passive components include GaAs bulk resistor, MIM capacitor, and via hole through 100-μm GaAs substrate. The entire chip is also protected by silicon-nitride passivation for reliability concern.

3 Low Noise Amplifiers

Both the one- and two-stage MMIC LNAs utilize four-finger 120-μm HEMT devices. The one-stage LNA and the first stage of the two-stage LNA are matched for minimum NF, and the second stage of the two-stage LNA is matched for gain [2], [3]. The matching networks are all realized with the inductive T-transformer using high impedance microstrip lines and series capacitors. Source feedback transmission lines are utilized in the input stages for stability consideration without degrading the noise performance. A shunt resistor series with LC resonator is used in the inter-stage of the two-stage design to enhance the out-of-band stability. On the bias networks, shunt RC networks are designed for low frequency stability. The chip photos are shown in Fig. 1. The chip sizes are 1.5 mm x 1 mm for one-stage design and 2.2 mm x 1 mm for two-stage one.

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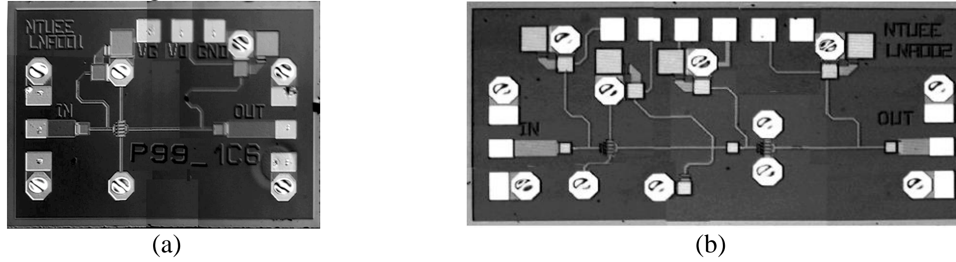
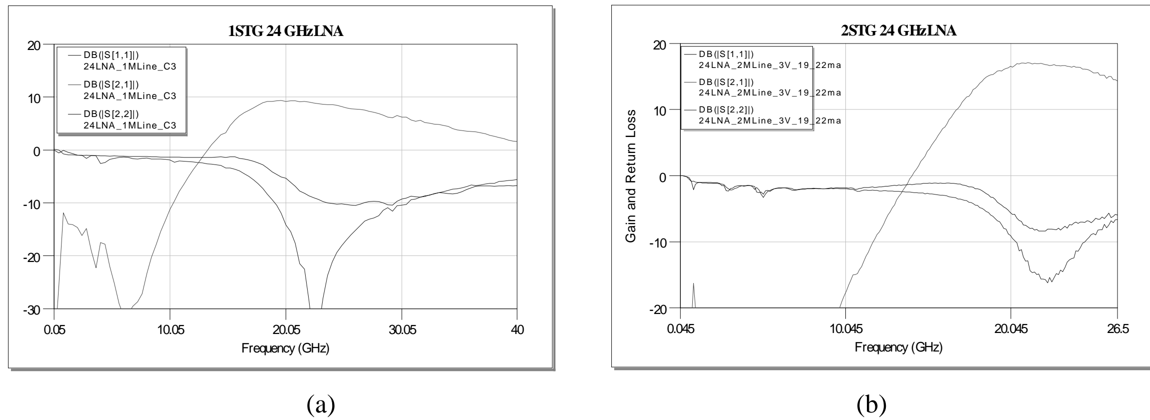
Fig. 2 shows the measured small-signal gain and return loss by on-wafer probing, the one-stage and two-stage amplifiers have small signal gain of 8.5 dB and 17 dB at 24 GHz, respectively. The one-stage chip is biased at 3-V drain voltage with 25-mA drain current, and the two-stage one is biased at 3-V drain voltage with 41-mA drain current.



(a) (b)

Fig. 1. The chip photos for the (a) one-stage, and (b) two-stage LNAs. The chip sizes are 1.5 mm x 1 mm and 2.2 mm x 1 mm, respectively.

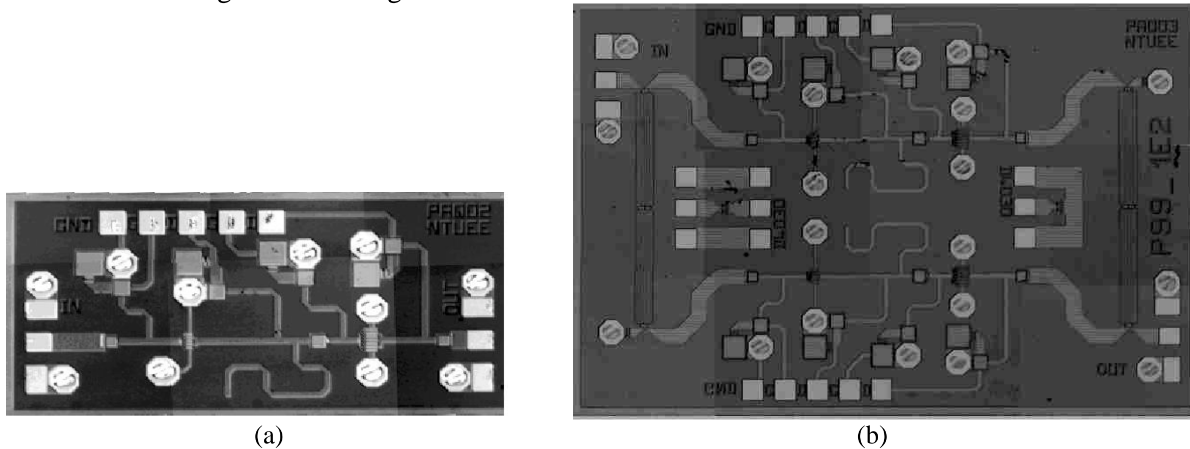


(a) (b)

Fig. 2. Measured small-signal gain and return loss for the (a) one-stage, and (b) two-stage LNAs.

4 Medium Power Amplifiers

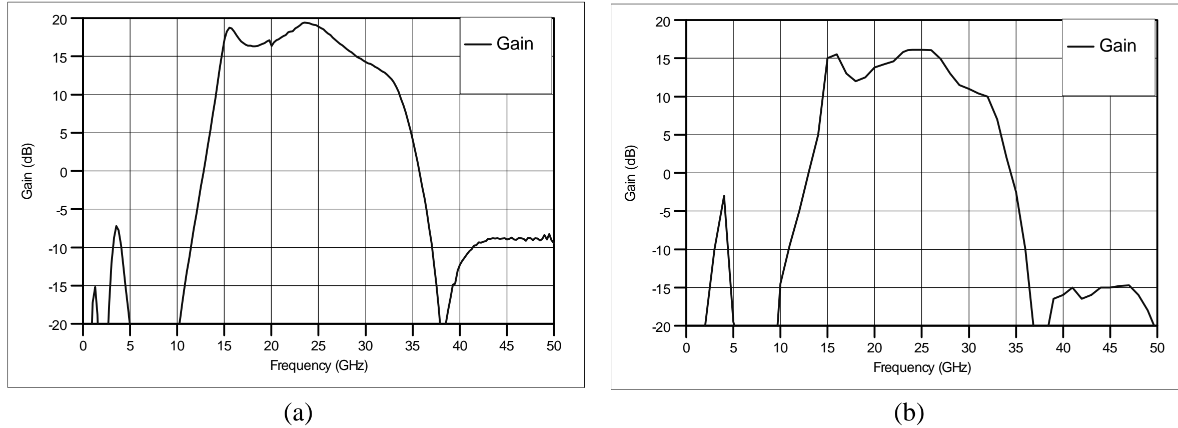
There are two medium PA chips in this paper including two-stage single-ended and balanced types [4]. In the two-stage single-ended amplifier, the 120-μm HEMT device is used to drive 300-μm HEMT device. Optimum load of output stage for maximum output power is derived from harmonic balanced simulation using commercial software Libra™ [5]. The input of output stage is matched to 50• . The driver stage is matched for gain, and source feedback transmission lines are added for stability concern. The matching networks are all realized with inductive T-transformer using high impedance microstrip lines and series capacitors. On the bias networks, shunt RC networks are designed for low frequency stability. The 90°hybrid, Lange coupler, and the single-end design are used to complete the balanced amplifier. The chip photos are shown in Fig. 3. The chip sizes are 2.2 mm x 1 mm for single-ended design and 3 mm x 2 mm for balanced one.



(a) (b)

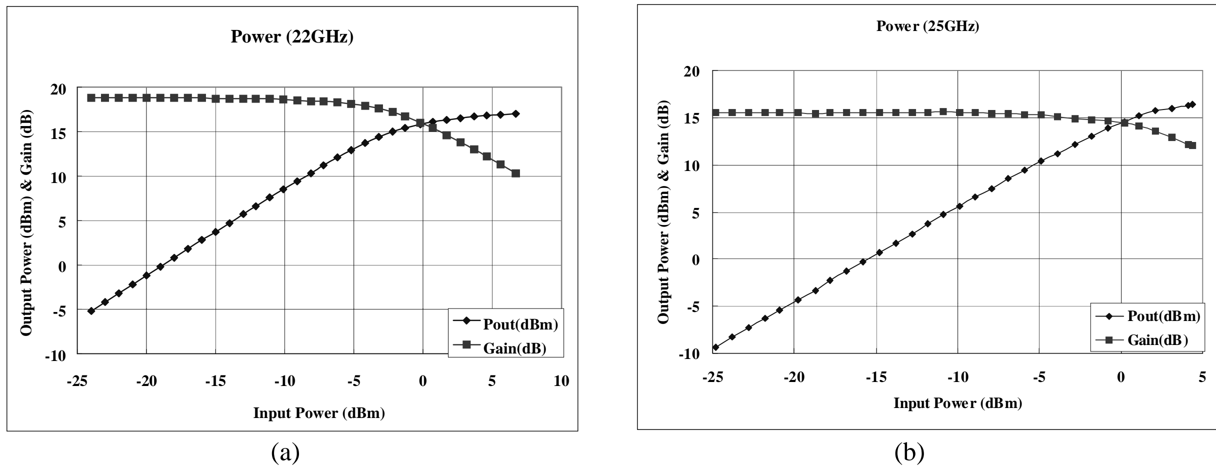
Fig. 3. The chip photos for the (a) single-ended, and (b) balanced medium PAs. The chip sizes are 2.2 mm x 1 mm and 3 mm x 2 mm, respectively.

Fig. 4 shows the measured small-signal gain by on-wafer probing, the single-end amplifier demonstrated a small signal gain of 19 dB at 24 GHz, and the balanced amplifier has a small signal gain of 17 dB. The power performance of the single-ended one is shown in Fig. 5. It has a 1-dB compressed power point (P_{1dB}) of 14.6 dBm at 22 GHz and 13.7 dBm at 25 GHz. The single-ended chip is biased at 3-V drain voltage with 62-mA drain current, and the balanced one is biased at 3-V drain voltage with 120-mA drain current.



(a) (b)

Fig. 4. Measured small-signal gain for (a) single-ended, and (b) balanced medium PAs.



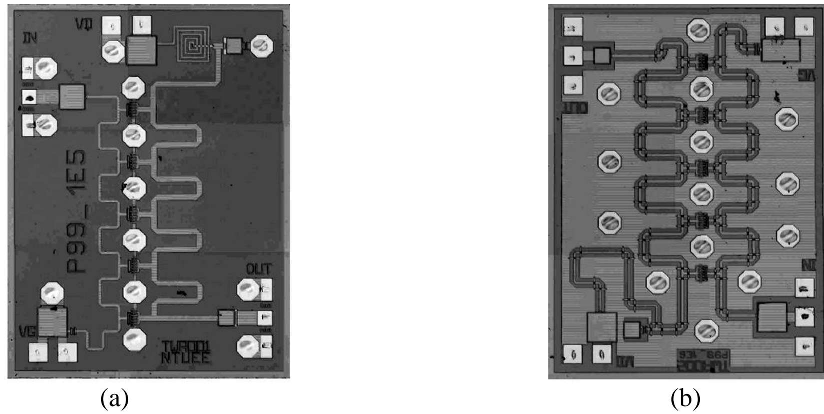
(a) (b)

Fig. 5. Measured output power versus input power for single-ended medium PA at (a) 22 GHz, and (b) 25 GHz.

5 Distributed Amplifiers

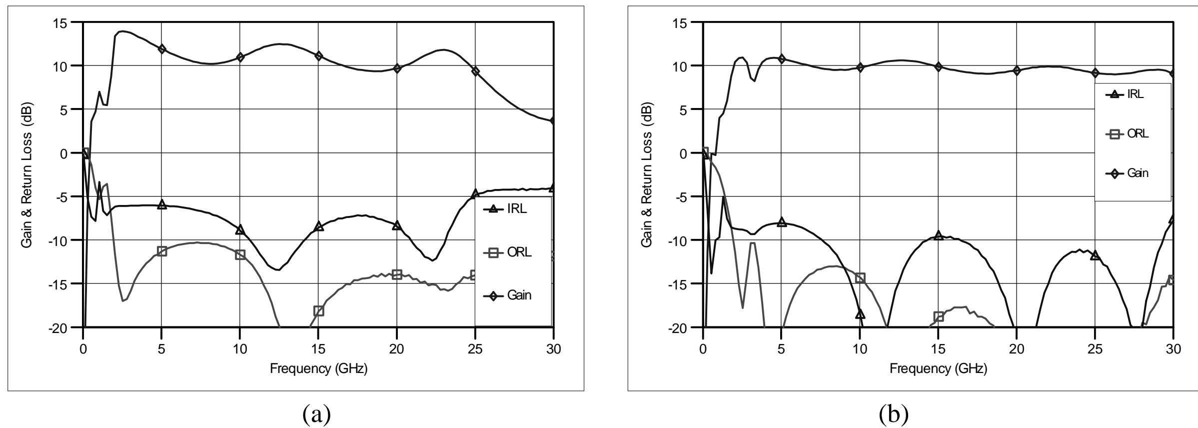
Five PHEMTs with a total gate periphery of 660 μm were used as the active devices for these amplifiers [6], [7]. Both microstrip line and GCPW are used to form the artificial gate and drain transmission lines. They are periodically loaded with the capacitive gate and drain impedance of the FET's forming lossy transmission line structures of different characteristic impedance and propagation constant. The resultant effective input and output propagation structures acted as gate and drain lines. An RF signal applied at the input end of the gate line travels down the line to the other end, where it is absorbed by the terminating impedance. The chips use capacitors, thin-film resistors and bulk resistors for biasing purposes and, the grounding is provided by means of backside via-holes. Compared with microstrip line, a GCPW design offers lower parasitic ground inductance, lower dispersion, and a GCPW design can minimize the coupling between transmission lines. The chip photos are shown in Fig. 6, and the chip sizes are both 1.5 mm x 2 mm.

Fig. 7 shows the measured small-signal gain and return loss by on-wafer probing. The microstrip-line design demonstrated a small signal gain of 12±2.5 dB, and the GCPW design has a small-signal gain of 10±0.5 dB. The microstrip-line chip is biased at 4.5-V drain voltage with 100-mA drain current, and the GCPW one is biased at 4-V drain voltage with 90-mA drain current.



(a) (b)

Fig. 6. The chip photos for (a) microstrip-line, and (b) GCPW DAs. The chip sizes are both 1.5 mm x 2 mm.



(a) (b)

Fig. 7. Measured small-signal gain and return loss for (a) microstrip-line, and (b) GCPW DAs.

6 Summary

Several K-band monolithic amplifiers including LNAs, medium PAs, and DAs were developed and measured. The MMIC chips are fabricated via commercial GaAs PHEMT foundry process and therefore have potential for mass production. Future development effort will be devoted to miniaturize the chip size to reduce the cost.

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