each of the images and the distance to the object. In the system described, an effective separation of the optical paths of ~6mm is obtained by selective use of part of the area of the single objective lens for left and right images. In the case of a typical endoscope view with objects some 30 to 100mm from the objective lens, this 6mm separation, when compared to a normal interoccular distance of 60mm, gives a similar perceived depth as objects at ~30cm to 1m.

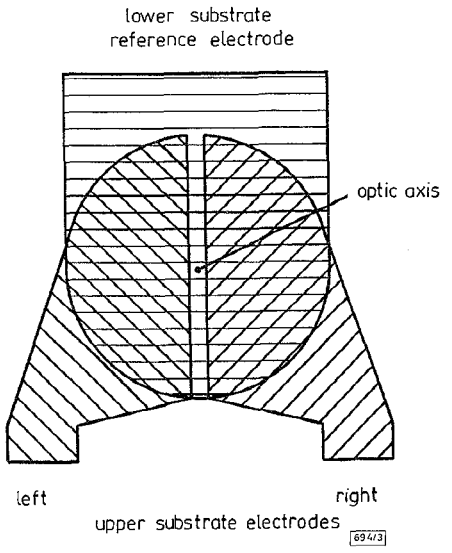

Fig. 3 *Electrode pattern for ferroelectric LCD*

Evalution and discussion: The image quality obtained using the FELC device with the 740 line CCD camera was excellent, the introduction of the liquid crystal device produced no noticeable degradation of the image. The necessary use of polarisers on the electro-optic device incurs a light loss of ~50% in addition to the light lost due to obscuring part of the optical path. This is the most serious limitation and further work is planned to investigate the trade-off between contrast ratio and stereoscopic separation.

The FELC device proved ideal for this application, as the drive signal for the shutter elements were easily derived from the camera and framestore circuits. To switch the FELC device, a charge of ~35nC must be supplied to the device during the switching period of 50 μs. This gives a modest drive requirement of < 1mA. These requirements were easily met; the two elements of the LC shutter were driven in antiphase from a signal derived from the image capture cycle of the CCD camera and framestore.

In the absence of objective evaluation procedures for stereoendoscopes, subjective initial trials were carried out with a number of different operators, and a wide variety of objects in the endoscope field of view. The camera system using the FELC shutter was compared with a system using a beamsplitter fitted with two cameras and also with an Olympus twin channel endoscope. The present system showed a significant advantage in terms of image brightness over the Olympus endoscope and gave a better perceived stereo image. The image and stereoscopic quality was judged to be as good as that using the beam splitter and dual camera system, but use of the FELC shutter allows the system to be less bulky and only half of the weight. To allow more accurate comparison between systems, standard tests are under development, the results of which will be reported in a later paper.

The endoscope camera system presented here useda monitor and shutter glasses. This arrangement has the advantage over VR types of display in that it does not obscure the surroundings. In the future, the output from the camera described here may be displayed using one of the 'glasses free' viewing systems currently under development [5].

Conclusions: A stereoscopic image capture system for use with an endoscope has been described. The use of ferroelectric liquid crystal electro-optic devices to modify the optical path at video rates, both for the camera and the 100Hz frame rate viewing system, has been successfully demonstrated. The stereo separation achieved is limited by the physical dimensions of the endoscope and the contrast ratio of the FELC device. The electro-optic switching speed and contrast of this device have been shown to be capable of giving good image separation and depth perception. The loss of image quality due to the insertion of the FELC device in the optical path has proved to be negligible with the camera in use. The ability to capture and display stereoscopic images has other applications; it could be used for enhancing the effectiveness of inspection procedures with a variety of instruments.

Acknowledgments: Thanks are due to B. Hodder and R. Sambles of Exeter University Physics Department for assistance in the manufacture of the LC devices used in this work. We also thank M. Lewis of GMMT for materials used in the LC device.

20 March 1997
Electronics Letters Online No: 19970582

G.A. Lester (*School of Engineering, University of Exeter, Exeter EX4 4QF, United Kingdom*)

J. Watts (*Liquid Vision Ltd., Old Workshops, Farringdon, Exeter, EX5 2JD, United Kingdom*)

D. Wilmington (*Mantracourt Electronics Ltd., Farringdon Park, Exeter EX5 2JB, United Kingdom*)

References

1 DURRANI, A.F., and PREMINGER, G.M.: 'Three-dimensional video imaging for endoscopic surgery', *Comput. Biol. Med.*, 1995, **25**, pp. 237–247

2 MITCHELL, T.N., ROBERTSON, J., NAGY, A.G., and LOMAX, A.: 'Three-dimensional endoscopic imaging for minimal access surgery', *J. R. Coll. Surg. Edin.*, 1993, **38**, pp. 285–292

3 STAVA, R.M.: '3-D vision technology applied to advanced minimally invasive surgery systems', *Surg. Endoscopy*, 1993, **7**, pp. 429–431

4 LESTER, G.A., COLES, H., MURAYAMA, A., and ISHIKAWA, M.: 'Electro-optic behaviour of low molar mass FELCs doped with liquid crystal polymers', *Ferroelectrics*, 1993, **148**, pp. 389–399

5 VAN BERKEL, C., FRANKLIN, A.R., and MANSELL, J.R.: 'Design and applications of multiview 3D-LCD'. Proc. 16th Int. Conf. Dsiplay Research, Birmingham, 1996, pp. 109–112

Highly accurate cyclic CMOS time-to-digital converter with extremely low power consumption

Poki Chen, Shen-Iuan Liu and Jingshown Wu

Indexing terms: CMOS integrated circuits, Instrumentation

The authors propose a new cyclic structure for a CMOS time-to-digital converter (TDC). The measured single-shot resolution is 286ps, and the measured single-shot accuracy is < 143ps. The new circuit can be shut down between measurements which makes the circuit suitable for portable applications.

Introduction: Time interval digitisation is an important element for many instrumentation circuits, such as range finders and the phasemeters [1], etc. Owing to large power consumption, conventional TDCs with subnanosecond resolution cannot easily be realised in portable systems. Recently, a novel TDC circuit, as shown in Fig. 1*a*, was proposed to obtain 780ps resolution (after averaging hundreds of measurements) with only 15mW power consumption [2]. The price is 3ns single-shot accuracy.

The degree of pulse shrinking of the delay element, in Fig. 1*b*, is controlled by V_{bias} [2]. For calibration, a stabilised reference period T_{ref} is fed into a delay line. The delay-locked loop will adjust V_{bias} to make T_{ref} reduce to zero exactly at the end, stage N, of the delay line. When a measurement is requested, the input period T_{in} will be fed through instead. Suppose that T_{in} reduces to zero at the nth stage, its width is then measured as $n \times T_{ref}/N$.

This circuit was a significant advance for low-cost, high-accuracy portable TDC systems. However, some important features still need to be improved. First, the delay line must be folded into segments, due to reasonable chip width or length limits. The inter-segment wiring is much longer than that for intra-segment wiring,

and causes a large linearity error [3]. Secondly, the mismatch among delay elements results in poor TDC linearity. Thirdly, the pulses reduce in width more rapidly at the last few stages, because they become too short to drive the next stage to toggle its state. Next, the calibration, which must be carried out continuously to make T_{ref} reduce exactly to zero at the last stage, consumes too much power [2, 3]. Finally, this TDC must double the size of its delay lines to only increase one output bit. To overcome these problems, a new TDC with a cyclic delay line is proposed.

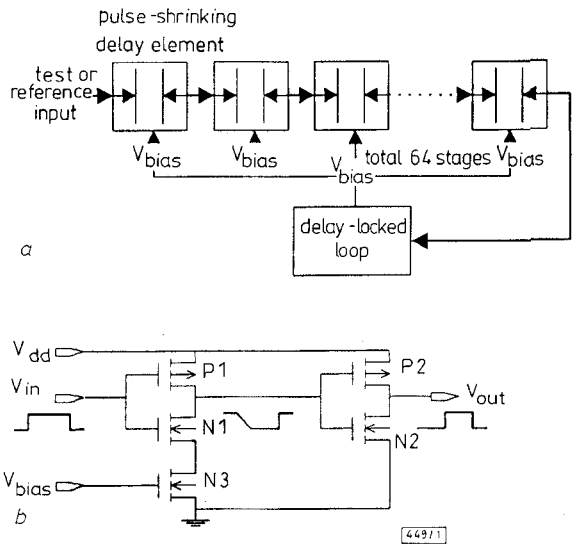

Fig. 1 *Block diagram of original CMOS TDC and pulse-shrinking delay element*

a Block diagram of original CMOS TDC
b Pulse-shrinking delay element used in Fig. 1*a*

Circuit description: As shown in Fig. 2*a*, the input pulse circulates in the proposed cyclic delay line. It reduces in width slightly each cycle until thoroughly diminished. Assume that the counter counts N for T_{ref} and n for T_{in}. T_{in} is then measured as $n \times T_{ref}/N$ theoretically. For practical implementation, the delay line is replaced by series-connected pulse-shrinking delay elements (Fig. 2*b*). We can adjust V_{bias} to make T_{ref} circulate over hundreds or thousands of cycles to obtain extremely fine resolution.

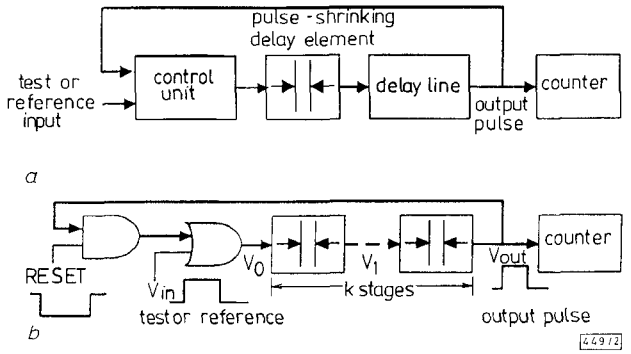

Fig. 2 *Conceptual block diagram of new TDC and realisation of cyclic TDC in Fig. 2a*

a Conceptual block diagram of new TDC
b Realisation circuit of cyclic TDC in Fig. 2*a*

The input pulse will go through the whole delay line once per cycle. The element mismatch and intra-segment wiring mismatch discussed will not cause any measurement nonlinearity from cycle to cycle. It is unnecessary to make T_{ref} just disappear at some specific cycle or stage. Sufficient resolution is obtained only if V_{bias} is properly adjusted so that T_{ref} circulates through the delay line a sufficient number of times before it vanishes. A slight variation in the output count N for T_{ref} is tolerable and continuous calibration is no longer needed. The circuit can not only be greatly simplified, but can also be shut down between measurements to save power.

The number of output bits of the new TDC is unlimited and can be increased by merely lengthening the internal counter in Fig. 2*b*, and control of V_{bias} made finer correspondingly. No averaging is needed to improve the resolution, because the single-shot resolution is accurate enough. The nonlinearity, caused by the pulse reducing in width more rapidly at the last few stages, can be treated as a constant count offset for a given V_{bias}. It can be completely calibrated out by the following technique. First, T_{ref} and $T_{ref}/2$ are fed into the TDC input and we assume that the circuit obtains N and N' counts, respectively. We have

$$T_{ref} = \alpha N + T_{offset}$$

where α = effective resolution

$$\frac{T_{ref}}{2} = \alpha N' + T_{offset} \qquad (1)$$

Then, T_{in} is fed into the TDC input, and the output count is assumed to be I. After solving α and T_{offset} from eqn. 1, we obtain

$$T_{in} = \alpha I + T_{offset} = \frac{T_{ref}(I + N - 2N')}{2(N - N')} \qquad (2)$$

T_{ref} and $T_{ref}/2$ must be re-measured for each T_{in} measurement to ensure eqn. 2 will produce enough accuracy. Only when α is above the required resolution should V_{bias} be adjusted to make α small enough again.

Measurement results: The proposed TDC has been fabricated with a 0.8μm SPDM CMOS process. It is composed of 64 delay elements in a cyclic structure with aspect ratio 3.0/0.8 (in μm/μm) for P1 and N1, 7.6/0.8 for P2, 2.3/0.8 for N2, and 1.3/0.8 for N3. The photomicrograph of the new TDC is shown in Fig. 3. The circuit size without the internal counter is reduced to 0.14 × 0.75mm only. If the counter is also included, the chip size is estimated to be 0.25 × 0.75mm. The average current consumption is calculated to be < 100nA from a 5V supply.

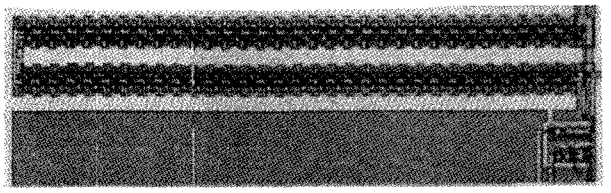

Fig. 3 *Photomicrograph of new TDC*

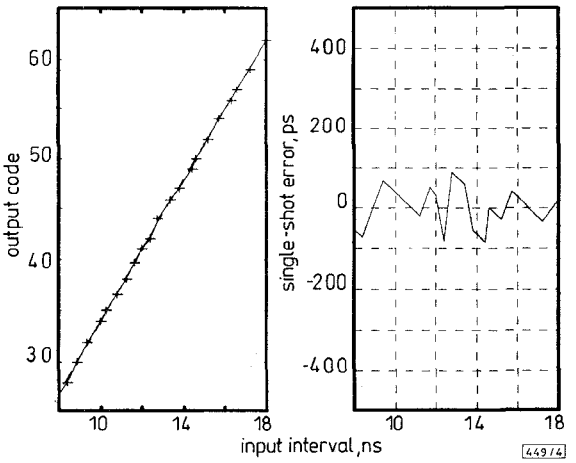

Fig. 4 *Single-shot measurements and their theoretical prediction line and measured single-shot error*

a Single-shot measurements and their theoretical prediction line
b Measured single-shot error
\+ measured
– – – – predicted

To explore the effective resolution that the new TDC can reach, a series of test pulses generated by an HP 8110A pulse generator were measured under different V_{bias}. The same pulses were also measured with a Standford Research Systems SR620 universal counter. The measurement results of single-shots for V_{bias} = 2.95V along with the theoretical prediction line are depicted in Fig. 4*a* as an example. The experimental data agrees very well with the prediction. The estimated effective resolution α is 286ps, and the measurement offset T_{offset} is 344ps. The single-shot errors are shown in Fig. 4*b* and are all < 0.5 α. This assures every output bit

is valid. Even though the overall time for each series of experiments is usually ~ tens of minutes, the bias voltage V_{bias} was never changed after initialisation during each series of experiments; therefore, the continuous calibration is unnecessary.

Conclusion: An extremely low-power, high-accuracy, and compact CMOS TDC with a cyclic delay line structure has been presented. The chip size is as small as 0.14 × 0.75mm, and the power consumption is only ~500nW. It can reach a single-shot resolution of 286ps experimentally. No averaging is needed to improve the accuracy, nor is continuous calibration. This certainly opens up a great deal of applications for the new TDC in low power and portable systems.

27 February 1997
Electronics Letters Online No: 19970594

Poki Chen, Shen-Iuan Liu and Jingshown Wu (*Department of Electrical Engineering, National Taiwan University, Taipei 10664, Taiwan, Republic of China*)

References

1 KOSTAMOVAARA, J., MÄÄTTÄ, K., KOSKINEN, M., and MYLLYLÄ, R.: 'Pulsed laser radars with high-modulation-frequency in industrial applications'. Proc. SPIE Laser Radar VII: Advanced Technol. Applicant., January 1992, Vol. 1633, pp. 114–127
2 RÄISÄNEN-RUOTSALAINEN, E.: 'A low-power CMOS time-to-digital converter', *IEEE J. Solid State Circuits*, 1995, **30**, (9), pp. 984–990
3 RAHKONEN, T.E.: 'The use of stabilized CMOS delay lines for the digitization of short time intervals', *IEEE J. Solid State Circuits*, 1993, **28**, (8), pp. 887–894

Quadratic-translinear CMOS multiplier-divider circuit

Weixin Gai, Hongyi Chen and E. Seevinck

Indexing terms: CMOS integrated circuits, Multiplying circuits

A novel current-mode analogue multiplier-divider based on the quadratic-translinear principle is presented. The input and output signals are all in current-mode. The circuit has favourable precision, wide dynamic range and is insensitive to variations in temperature and processing. It is suitable for VLSI implementation and can be used in many hardware design fields such as fuzzy logic controllers and analogue neural networks.

Introduction: Analogue multipliers are key-elements in a wide range of analogue systems, such as modulators, phase discriminators, adaptive filters, RMS-DC converters, sine/cosine synthesisers, etc. Recently, analogue multipliers have also found use in fuzzy logic controllers and artificial neural networks. Many kinds of multipliers suitable for MOS technology [1 – 4, 8] have been developed.

Based on the quadratic-translinear [5] principle, a novel current-mode analogue multiplier-divider is presented. This circuit has favourable precision, wide dynamic range and is insensitive to temperature and manufacturing variations.

Quadratic-translinear circuit principle: The term 'translinear' (TL) was suggested by Gilbert in 1975. It is a contraction of the key property: a Transconductance which is Linear with current [6]. The bipolar transistor is the main electronic device possessing this property. The original TL principle was extended to MOS technology in 1991 [7]. It is dependent on transconductance being linear with voltage. This is equivalent to a quadratic relationship between the drain saturation current and the gate-source voltage, leading to a new term 'quadratic-translinear' (QTL) [5].

We consider a loop of NMOS transistors as indicated in Fig. 1. In the loop, the gate-source voltages of these MOS transistors are connected in series, with equal numbers of transistors arranged clockwise and counterclockwise. The current sources shown are bias or signal currents. All transistors operate in saturation. According to Fig. 1, eqn. 1 can be derived [7]:

$$\sum_{cw}\left(\sqrt{\frac{I_D}{w/l}}\right)=\sum_{ccw}\left(\sqrt{\frac{I_D}{w/l}}\right) \tag{1}$$

Eqn. 1 is a statement of the QTL circuit principle. It is a simple relationship involving the drain current I_D and aspect-ratio w/l of the MOS transistors, which are insensitive to temperature and processing.

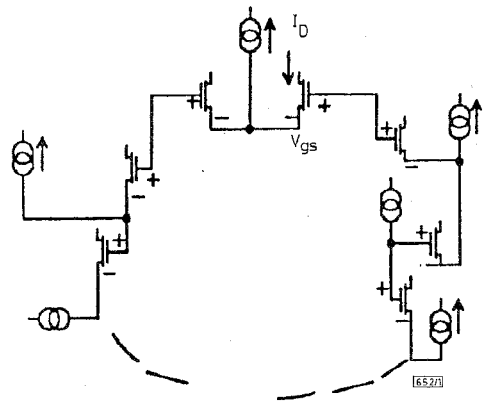

Fig. 1 *Loop of NMOS transistors*

Novel current-mode analogue multiplier-divider: Consider a multiplication-division function

$$I_z=\frac{I_xI_y}{I_w} \tag{2}$$

where I_x, I_y, I_w, I_z are all current signals.

To synthesise eqn. 2 by the use of the QTL circuit principle, we transform it as follows:

$$I_z=\frac{I_xI_y}{I_w}$$
$$I_z=((I_x+I_y)^2-I_x^2-I_y^2)/(2I_w)$$

Defining:

$$f=(I_x+I_y)^2/(4I_w)\quad g=(I_x)^2/(4I_w)\quad h=(I_y)^2/(4I_w)$$

Then

$$I_z=2f-2g-2h \tag{3}$$
$$f=(I_x+I_y)^2/(4I_w)$$
$$2\sqrt{fI_w}=I_x+I_y$$
$$f+I_w+2\sqrt{fI_w}=f+I_w+I_x+I_y$$

Taking square-roots:

$$\sqrt{f}+\sqrt{I_w}=\sqrt{f+I_w+I_x+I_y}$$
$$\sqrt{f}+\sqrt{I_w}=2\sqrt{(f+I_w+I_x+I_y)/4} \tag{4}$$

Similarly,

$$\sqrt{g}+\sqrt{I_w}=2\sqrt{(g+I_w+I_x)/4} \tag{5}$$
$$\sqrt{h}+\sqrt{I_w}=2\sqrt{(h+I_w+I_y)/4} \tag{6}$$

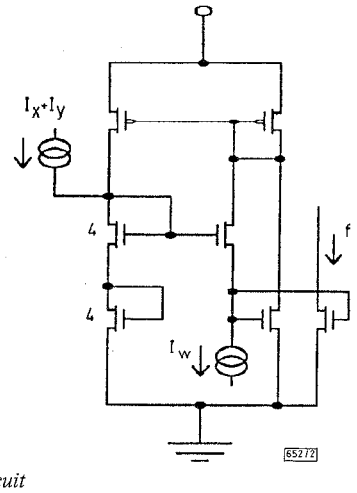

Fig. 2 *QTL circuit*