Efficient Shared Buffer Optical Stars for Bursty Traffic and Fault Tolerance in 3-Stage ATM Switches†

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ABSTRACT An efficient buffer sharing approach with fault-tolerant mechanism between the switch-units of a 3-stage shared buffer ATM switch is proposed to reduce bursty traffic cell loss ratio, the required buffer size in each switch-unit, and the number of required redundant switch-units in fault-tolerant applications. With the buffer sharing nature, the proposed structure can reduce cell loss ratio and the required buffer size of a switch unit. The buffer sharing interconnection structure is based on the passive optical star couplers employing the WDM (Wavelength Division Multiplexing) and the multi-bit parallel transmission technologies for accessing cells in the memory buffers of the switch-units, which can reduce the transmission speed requirement and the wire complexity. A practical example in B-ISDN is shown that 7 optical channels are sufficient in the passive optical stars for building a 1024 × 1024 ATM switch under a bursty-overflow traffic load of 0.2 and cell loss ratio below 10^{-6}.

1. Introduction

In recent years, much attention has been paid to a promising technique, the asynchronous transfer mode (ATM), for transferring and switching a wide range of communication services in Broadband Integrated Service Digital Network (B-ISDN) [1]. An ATM system requires a high-speed switching fabric which exchanges a large number of short and fixed-length packets (cells) according to the attached headers. A lot of switching fabrics have been proposed to implement the ATM switches [2-4]. In general, these switching fabrics need buffers due to bursty traffic and the output contention problem. [6,11,12].

In many proposed output-buffered switching fabrics, the shared output buffer architecture is one of the best techniques to reduce the required buffer size [8-10]. However, all the cells arriving at the switch inputs must be transmitted into their corresponding output ports within one cell time slot. Thus, the speed of the internal fabric has to operate N times faster than the input or output links for an $N \times N$ switch, where N is the number of input or output ports. For a large N, such a speedup is not feasible in an ATM switch. However, a 3-stage nonblocking network constructed by a number of small size shared buffer *switch-unit*, for instance 32 × 32 or 64 × 64, is most commonly used [8,9].

For a fixed buffer size switch-unit, the cell loss ratio may be increased dramatically due to bursty traffic when a large number of incoming cells are destined to the same switch-unit in a short period of time. The large number of lost cells may include routing information (call setup between switch-units, trunk/line signaling cells), OA&M messages, and loss inhibited data, *etc.* Although some of them can be re-transmitted, the quality of service (QoS) of the network may suffer a lot.

In this paper, we propose an extended buffer sharing approach which shares buffers among the switch-units to reduce cell loss due to bursty traffic. Once buffer overflow occurs in a switch-unit, the over-loaded cells are stored in one of the other switch-units through a passive optical star, and then fetched through another passive optical star. In other words, the shared buffer nature can be further enhanced, and the buffer size in each switch-unit can be reduced.

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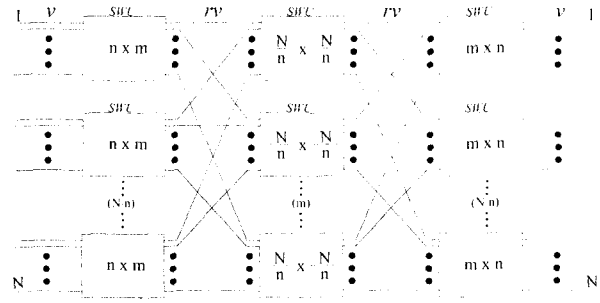
2. Optically Interconnected Structure for Shared Buffer 3-Stage ATM Switches

A 3-stage Clos network is composed of a number of identical switch-units as shown in Figure 1. A problem with such a net-



v : input/output line speed; rv : internal link speed; SWU : switch-unit.

Figure 1. *The general 3-stage nonblocking modular Clos switch architecture.*

work is that the ATM bandwidth allocation of the cell setup cannot be performed very frequently due to the internal link blocking. The network is nonblocking if and only if the number of switch-units m in the second stage is greater than or equal to $2n-1$, where n is the number of input ports of a switch-unit in the first stage [20]. The network is also nonblocking if the number of faster internal links is several times larger than that of the incoming lines [19]. To simplify the specification, we will focus on the former structure in the following discussion.

In the 3-stage Clos network, most of the cells will be queued at the 3rd stage. Thus, cell loss due to *bursty traffic*, will happen at the 3rd stage. The approach of buffer sharing among the switch-units can effectively decrease cell loss at the 3rd stage.

A. Shared Buffer Memory Switch Architecture

For a large scale ATM switch as shown in Figure 1, the *switch-unit* is implemented with a shared buffer memory switch architecture. Figure 2 shows the conceptual architecture of a shared-buffer switch. It consists of four major portions: (i) a memory pool (MEMP); (ii) a multiplexer (MUX); (iii) a routing controller (RC); and (iv) a demultiplexer (DMUX).

In each cell time slot, input cells are taken sequentially from port 1 to port g. In the meantime, the control signals of each input packet are extracted by MUX and sent to RC. A proper memory address is then given by RC to store the cell into MEMP. RC is an effective memory management controller. It keeps the order of the incoming packets in MEMP. To avoid out-of-sequence issue, two memory management methods are used in RC. The first is *link-list address scheduling* [8]. All the incoming cells are chained in a link-list form. Each cell in MEMP has a pointer to

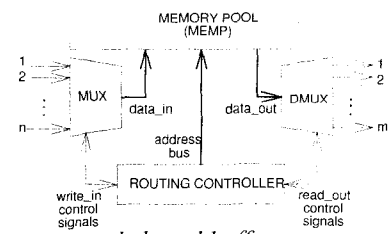


Figure 2. *The conceptual shared buffer memory switch.*

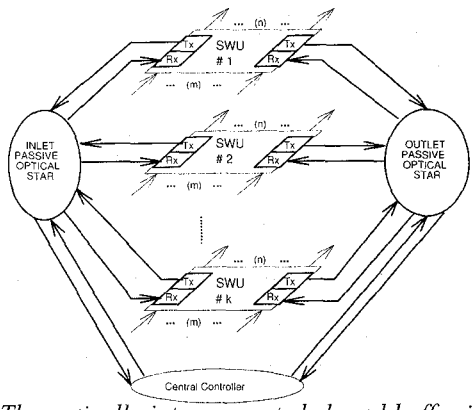


Figure 3. *The optically interconnected shared buffer in the third stage.*

indicate the next cell. Thus, RC only records a packet chain's top and end of all output ports. The second is *separated queue address scheduling* [13]. Each output port has a FIFO queue to sequentially buffer the stored packet addresses in MEMP which are destined to this output port. The former has lower hardware complexity whereas the latter has higher reliability.

B. Extended Shared Buffer Topology

The *Optically Interconnected Shared Buffer Scheme* is shown in Figure 3. When bursty traffic occurs, the buffers of this switch-unit may be overflowed and lose packets. However, in the mean-time, other switch-units may have enough buffer to store the overloaded packets to prevent packet loss. *Inlet passive optical star* and *outlet passive optical star* are used to establish the routes for storing incoming packets in other switch-units and for fetching the outgoing packets which are temporally stored in other switch-units, respectively. Each optical star has a number of optical channels with different wavelengths to support inter switch-unit memory requests. Each switch-unit has two pairs of tunable transmitter (TX) and tunable receiver (RX). When an switch-unit issues an external memory request, an optical channel with a distinct wavelength will be selected. The central controller collects the memory utilization of all switch-units. If any inter-switch-unit memory is requested, the central controller performs the channel assignment algorithms. After selected an optical channel, the central controller informs TX of the requesting switch-unit, and RX of the providing switch-unit, to tune to the selected wavelength. The cell and memory access signals are transmitted and received through this optical channel with the assigned wavelength. The control signals between all the switch-units and the central controller are communicated through a fixed optical channel with a distinct wavelength λ_c.

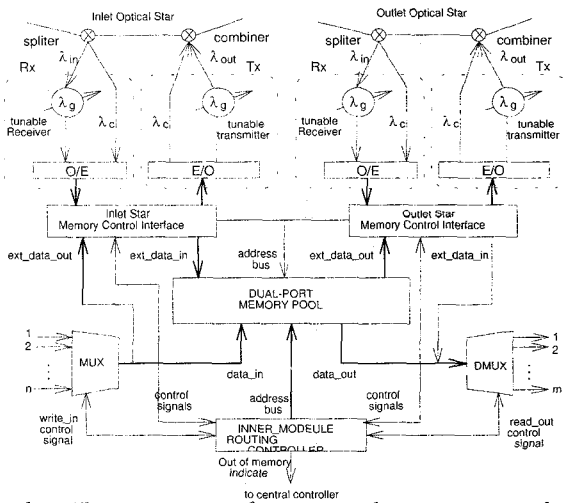


Figure 4. *The structure of an optical interconnected shared buffer switch-unit.*

Figure 4 is the extended functional architecture of a switch-unit. MEMP uses a *dual-port* memory for the internal switch-unit access and the external switch-units access. RC handles the intra-switch-unit routing control and the inter-switch-unit memory access operations. All input signals come from the optical stars which are composed of a number of 2×2 couplers [14]. An optical splitter or WDM demultiplexer separates the control signal λ_c and a tunable receiver filters the signals of external packets with the selected wavelength λ_g. After O/E conversion, λ_c is sent to RC and λ_g is fed into a memory control interface. RC then selects an address of MEMP to store the external cell or to fetch the cell which is stored in other switch-units. In contrast, the cell which wants to be stored in another switch-unit or the external cell which wants to be stored in this switch-unit will be sent by the selected wavelength.

The detail switching scheme of the extended switch-unit is shown in Figure 5. It is easy to implement with only modifying mini-time slot partition for an asymmetrical switch-unit. All the incoming cells will be served to write in the destined switch-unit or an external switch-unit in an inlet cycle, whereas all the outgoing cells will be read out from the sending MEMP or external MEMPs in an outlet cycle. These two cycles are functionally independent, and therefore they are processed concurrently.

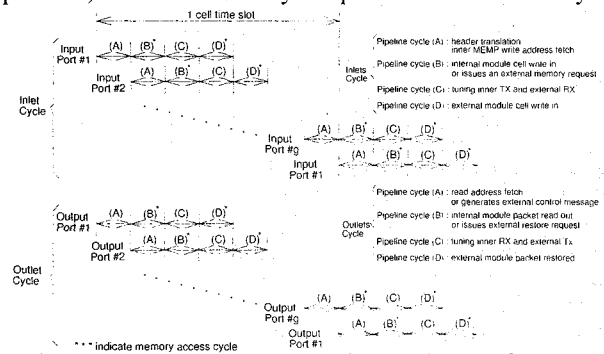


Figure 5. *The shared memory switching scheme of the optically interconnected switch-unit.*

Because a packet needs to be written into (or read out from) a switch-unit and at the same time a packet requires to be stored in (or fetched from) an external switch-unit due to buffer overflow, two pipelined parallel operations are performed. In an inlet cycle, a packet in each input port is served by a 4-stage pipelining cycle. The function of each stage is:

stage (A) Translate header and fetch MEMP address;
stage (B) Writes input cell to MEMP or issues an external request to the central controller if overflow;
stage (C) Tunes TX of the sending switch-unit and RX of the selected external switch-unit;
stage (D) Writes the input cell to the external switch-unit.

If no buffer overflow, stages (C) and (D) are idle.

In an outlet cycle, all output ports are served in a round-robin sequence. Each output port also has 4-stage pipelined operations to read out the stored cell as shown below:

stage (A) Fetch the read address for a cell stored locally or generates control message to RC if the packet is stored in an external switch-unit;
stage (B) Reads cell data if the cell is stored locally or issues an external request to the central controller if the cell is stored in another switch-unit;
stage (C) Tunes RX of the receiving switch-unit and TX of the external switch-unit where the cell is stored;
stage (D) Restores the cell data that is stored in the external switch-unit.

Similarly, stage (C) and stage (D) are idle if the cell is stored locally. At most two read/write accesses can be outstanding in each mini-time slot in both concurrent inlet and outlet cycles.

3. Optical Channel Assignment Algorithms

Two optical channel assignment algorithms in the central controller are derived for inlet and outlet passive stars.

A. Inlet Optical Channel Assignment Algorithm

The inlet optical channel assignment algorithm is depicted in Figure 6(a). Denote the buffer utilization of switch-units with $A[k]$ (k = 1, 2, ..., K). $A[k]$ indicates if the switch-unit has enough buffers or not. A barrel shifter or sorter is used to partition $A[k]$ into $B[i]$ and $C[j]$, where i = 1, 2, ..., I; j = 1, 2, ..., J; $I + J = K$. $B[i]$ denotes the switch-units which have enough buffers to provide, whereas $C[j]$ denotes the switch-units which have issued an external buffer request. That is, $B[i]=k$ if $A[k]=0$ or $C[j]=k$ if $A[k]=1$, for i=1, 2, ..., I, j=1, 2, ..., J, and k=1, 2, ..., K. By matching these two subarrays, a number of optical channels can be easily assigned with subscript number of each subset, such as λ_{g1} be assigned to switch-unit of $B[1]$ and switch-unit of $C[1]$, λ_{g2} to switch-unit of $B[2]$ and switch-unit of $C[2]$. Cell loss occurs when $j > i$, since the number of buffer-providing switch-units is less than that of buffer requesting switch-units. However, we assume that it will not happen with good traffic management.

B. Outlet Optical Channel Assignment Algorithm

The outlet optical channel assignment algorithm is proposed as depicted in Figure 6(b). Denote buffer status of switch-units by $D[k]$ (k = 1, 2, ..., K). $D[k]$ indicates the packet stored in the corresponding switch-unit. A mapping unit is used to collect the number of switch-units whose packets are stored in the same switch-unit, and push them into the corresponding queues $E[k]$ (k = 1, 2, ..., K). By matching the index of E and its entry, the optical channel can be easily assigned. For example, λ_{g1} is assigned to TX of switch-unit 2 and RX of switch-unit 3 (where top of $E[2]$ = 3), and λ_{g2} is assigned to TX of switch-unit 3 and RX of switch-unit 1 (where top of $E[3]$ = 1). If more than one switch-unit's packet are stored in the same switch-unit, only a packet in one of the switch-units can be restored and other packets will be fetched in the following cell time slots. Since the packets are all stored in the buffer, there is only cell delay and no cell loss.

4. Feasibility Studies of Optical Techniques in Switch-Units

A. Requirements of MEMP

The ATM cell length of 53 octets is not sufficient to support internal switching control, such as routing destination/multicast tags, priority indicators, and cell type identifiers. Assume an internal cell size is k octets, the input/output trunk speed s_T to/from an MEMP becomes $s_T = v \times k / 53$, where v is the speed of user network interface.

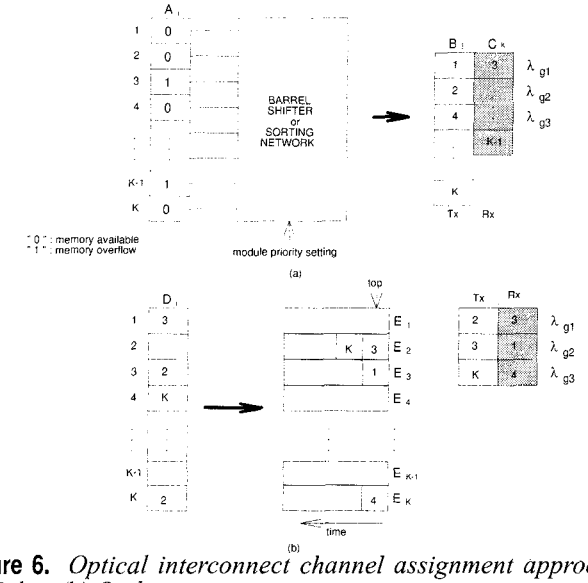


Figure 6. *Optical interconnect channel assignment approaches (a) Inlet; (b) Outlet.*

In an switch-unit, all the input cells of each input port must be served within a cell time slot. Thus, the access time t_a of MEMP shall be limited as $t_a = c_T / n$, where c_T is a cell time slot duration ($c_T = 1 / s_T$), and n is the number of input ports. Figure 7 shows the relationship of t_a vs. n for OC-3, OC-12, and OC-48. The internal cell size k is 64 octets. It is sufficient to carry more additional messages, and it is a power of 2 which is very suitable for hardware implementation. The access time of presently available RAMs is only about 10 ns.

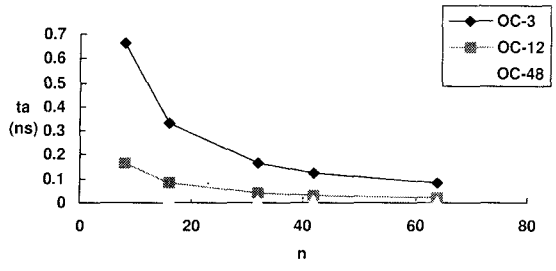


Figure 7. *The memory access time t_a vs. the number of input ports n.*

However, all of them are not sufficient to support the examples as shown in Figure 7 by bit-serial transmission. One solution uses a serial-to-parallel conversion with a p-bit parallel transmission bus. Thus, the required access time of MEMP can be changed to $t_a = p \times c_T / n$. The results of the input lines with OC-3 are shown in Figure 8. For a 32 × 32 switch-unit, the access time of MEMP would be acceptable by selecting p = 16 for OC-3.

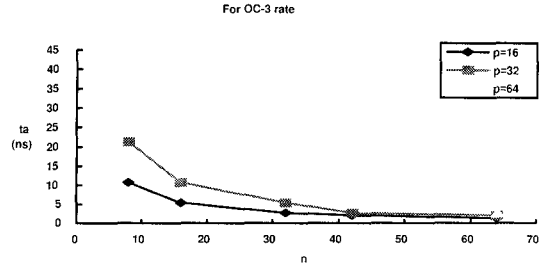


Figure 8. *The access time of different p-bit parallel transmission buses.*

B. Wavelength Encoded Multi-Channel Optical Bus (WEMCOB) Encoding Technique

Considering a 1024 × 1024 ATM switch for OC-3. If the 16-bit parallel transmission bus described in Section 4-A is adopted between the switch-units in each stage, it is difficult to implement with copper links. Even for the simplest bus interconnection topology, the high hardware cost incurred by additional 32 I/O pins is also difficult to implement in a chip or a single printed circuit board. Moreover, very high speed operations to support memory access protocols are difficult for these topologies. Thus, a parallel transmission technique with much lower hardware complexity becomes more attractive.

The wavelength encoded multi-channel optical bus (WEMCOB) [16] can be modified to implement an extended switch-unit. Data are transmitted in parallel through *a single fiber*. Data are encoded with distinct wavelengths. These wavelengths are combined with a WDM multiplexer, and then transmitted through a single-mode fiber. At the receiver end, a WDM demultiplexer separates the received signals through their wavelengths. These optical signals are then converted into electrical signals. Moreover, the scheme is based on the WDM technology in which separate low-speed control and high-speed data channels are transmitted in parallel to reduce the link speed, the power consump-

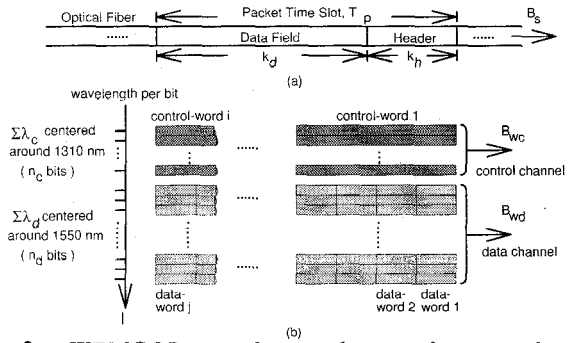


Figure 9. *WEMCOB encoding technique for a packet being transmitted.*

tion, and the wire complexity. However, the control signals and the memory access message can be encoded into the control channels, whereas the packets can be encoded in the 16-bit-wide data channels as shown in Figure 9 [16-18].

5. Performance Evaluation and Fault Tolerance Application

A. Analysis of The Number of Required Optical Channels

Only the 3rd stage is taken into consideration in the 3-stage switching network. A variable β, the offered *bursty-overflow traffic load* of each switch-unit at the 3rd stage is defined as the probability of a switch-unit with fix-size buffer being in turned into the *bursty-buffer-overflow condition* (which means the buffer of the switch-unit will be overflowed with such traffic load) in one cell time slot. β is a function of buffer size, input burst length and input traffic load. β increases as the buffer size and the grouping size decrease, or as the input traffic load increases. To simplify the analysis, we do not discuss the above factors.

Assume that cells arrive independently from different input ports and are uniformly delivered to all output ports in each switch-unit. The buffer size of each switch-unit is assumed identical. The variables are defined as follows.

m: the number of input ports in a switch-unit.
$L = (N / n)$: the total number of switch-units in the 3rd stage.
P_k: the probability of k switch-units that arrive under the bursty-allowance condition in one slot.
$(1 - \beta) / L$: the average number of switch-units under bursty-allowance in one slot.

The P_k is assumed to be the following binomial probability:

$$P_k = \binom{L}{k}\left(\frac{1-\beta}{L}\right)^k\left(1-\frac{1-\beta}{L}\right)^{L-k} \qquad k = 0,1,\ldots, L\,.$$

The average number of cells from all input ports that are destined for a switch-unit in one cell time slot is expressed as

$$\Lambda_i = \sum_{k=1}^{G}\sum_{j=1}^{m} jkP_k = \sum_{j=1}^{m} j\cdot\left(L\cdot\frac{1-\beta}{L}\right) = (1-\beta)\cdot\eta\,,$$

where $\eta = [m(m+1)]/2$.

If C is the number of optical channels, the average number of cells from all input ports that have arrived at an output port in one cell time slot is

$$\Lambda_o = \sum_{k=1}^{C}\sum_{j=1}^{m} jkP_k + \sum_{k=C+1}^{G}\sum_{j=1}^{m} jCP_k$$

$$= \sum_{k=1}^{L}\sum_{j=1}^{m} jkP_k - \sum_{k=C+1}^{L}\sum_{j=1}^{m} jkP_k + \sum_{k=C+1}^{L}\sum_{j=1}^{m} jCP_k$$

$$= \Lambda_i - \sum_{k=C+1}^{L}\sum_{j=1}^{m} j(k-C)P_k\,.$$

Since at most C cells are sent through the extended optical stars in the bursty-buffer-overflow switch-units in one cell time slot, the excess cells will be discarded and lost. The cell loss ratio is

$$P(\text{cell loss}) = \frac{\Lambda_i - \Lambda_o}{\Lambda_i} = \frac{1}{\Lambda_i}\sum_{k=C+1}^{L}\sum_{j=1}^{m} j(k-C)P_k$$

$$= \frac{1}{1-\beta}\sum_{k=C+1}^{L}(k-C)\cdot\binom{L}{k}\left(\frac{1-\beta}{L}\right)^k\left(1-\frac{1-\beta}{L}\right)^{L-k}.$$

The curves with different L and β are shown in Figure 10. It shows that only 7 and 8 optical channels are required in a 1024 × 1024 (with 64 switch-units) switch and a 2048 × 2048 (with 128 switch-units) switch under 0.2 bursty-overflow traffic load for cell loss ratio below 10^{-6}, respectively.

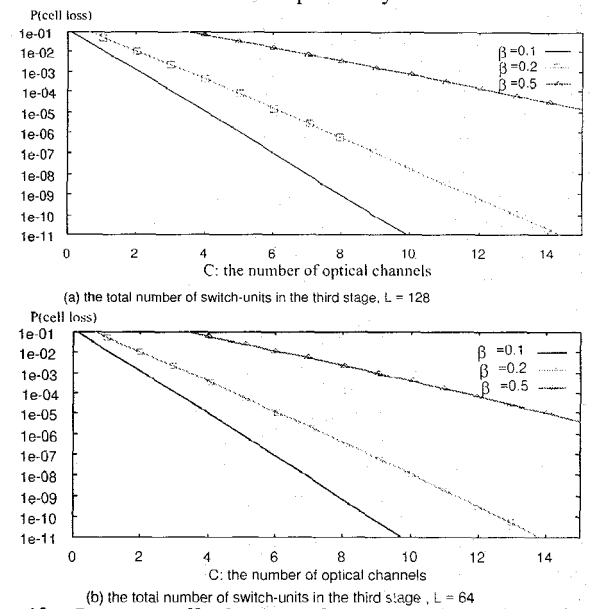


Figure 10. *Bursty traffic loss vs. the required number of optical channels.*

B. Fault-Tolerant Application

For large scale ATM switches, the fault-tolerant capability becomes very important. 1 (switch fabric) + 1 (switch fabric) redundancy with hot swap functions is one of the popular fault-tolerant schemes [21]. As shown in Figure 11, two planes of switch fabrics operates simultaneously; one is active and the other standby. When the active plane is detected fail, the standby plane takes over automatically. In normal condition, the standby plane is idle when the active plane is working well. In addition, since the standby plane operates simultaneously with the active plane, the defect probability of two or more switch elements which belongs to different planes may fail at the same time is not negligible. In this case, the off and on switchovers between the two planes will result in performance degradation and decrease the QoS and reliability dramatically.

To support the fault tolerant capability in a 3-stage shared buffer ATM switch, we briefly define the faults: the switch-unit memory fault and the interconnection link fault. The optically interconnected structure can be used with small modifications as a unique fault-tolerant structure for multi-stage large scale ATM switches to tolerate faults. As shown in Figure 12, only one re-

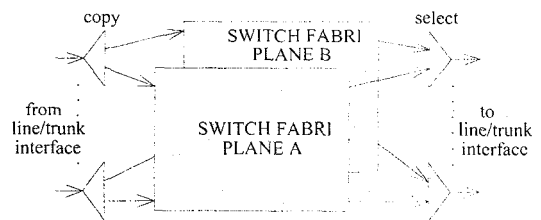


Figure 11. *The general redundancy structure of a large scale switch.*

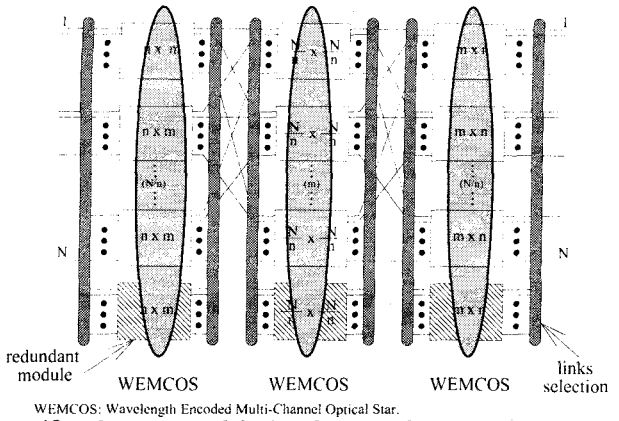


Figure 12. *The proposed fault-tolerant scheme.*

dundant switch-unit is required in each stage. All the switch-units are connected by the WEMCOB based optical star.

If a switch-unit memory fault is detected, the incoming cells are temporally accessed in other switch-units until the memory of the faulty switch-unit is replaced. The hot swap function is completed by the *links selection* circuitry to resolve the interconnection link fault. If a switch-unit is detected fail in the links, its links will be swapped to the redundant unit of the same stage by link selection circuitry. All the cells before swapping can be stored in other switch-units temporarily until the redundant one is ready. The cells will then be fetched through the star to the redundant unit and sent to the next stage or a distinct output port. However, the faulty switch-unit becomes the new redundant unit after it is repaired. Unlike the whole plane switchover in the 1 + 1 redundancy scheme, the switchover function is completed between the faulty switch-unit and the redundant unit, thus the cell loss caused by the switchover can be reduced significantly. Table 1 shows the comparison of the required number of switch-units in the proposed scheme with the traditional one.

6. Conclusions

We have presented a scalable, high-speed extended shared output buffering approach to be applied in a 3-stage ATM switch with shared buffer memory switch-units. The buffer in a switch-unit can be shared among the switch-units at the same stage when buffer overflows in some of the switch-units due to bursty traffic. Two passive optical star couplers are used to interconnect the switch-units of the 3rd stage and operate the buffer sharing functions. We proposed a buffer-sharing pipelined switching scheme in the shared-buffer switch-unit such that only a dual-port memory pool is needed. A scalable, high-speed wavelength encoded multi-channel optical bus called WEMCOB is used to meet the memory access requirements. WEMCOB reduces the link speed and the wiring complexity, and simplifies the control circuitry in the switch-units and the optical star couplers. We have also proposed optical channel assignment algorithms to resolve multiple external memory requests. We have shown that at most 7 and 8 optical channels are required in a 1024 × 1024 and a 2048 × 2048 ATM switch fabric, respectively, such that cell loss ratio due to bursty traffic can be reduced below the requirement of the entire switch. Finally, the WEMCOB based optical stars are also applied in the large scale fault-tolerant switch fabric. The required redundant switch-units can be reduced in comparison with the traditional 1 +·1 redundant switching scheme.

Table 1. *The number of required switch-units for different redundancy schemes.*

Redundancy \ Scale	512×512	1024×1024	2048×2048	4096×4096
No Redundancy	64	128	256	512
1 + 1 Redundancy Scheme	128	256	512	1024
Proposed Scheme	64 + 3	128 + 3	256 + 3	512 + 3

References

[1] CCITT Draft Recommendations for B-ISDN, 1990.

[2] H. Ahmadi and W. E. Denzel, "A survey of modern high-performance switching techniques," *IEEE J. Select. Areas Commun.*, vol. 2, pp. 1091-1103, Sep. 1989.

[3] F. A. Tobagi, "Fast packet switching architectures for broadband integrated services digital network," *Proc. IEEE*, vol. 78, pp. 133-167, Jan. 1990.

[4] Papers in "Large-scale ATM switching systems for B-ISDN," *IEEE J. Select. Areas Commun.*, vol. 9, no. 8, Oct. 1991.

[5] M. Hluchyj and M. Karol, "Queueing in high-performance packet switching," *IEEE J. Select. Areas Commun.*, vol. 6, pp. 1587-1597, Dec. 1988.

[6] M. J. Karol, M. G. Hluchyj, and S. P. Morgan, "Input versus output queueing on a space-division packet switch," *IEEE Trans., Commun.*, vol. 35, pp. 1347-1356, 1987.

[7] S. C. Liew, "Performance of Input-Buffered and Output-Buffered ATM Switches under Bursty Traffic: Simulation Study," *GLOBECOM'90*, pp. 1919-1925, 1990.

[8] T. Kozaki *et al.*, "32 × 32 Shared Buffer Type ATM Switch VLSI's for B-ISDN's," *IEEE J. Select. Areas Commun.* vol. 9, pp. 1239-1247, Oct. 1991.

[9] Y. Shobatake *et al.*, "A One-Chip Scalable 8 × 8 ATM Switch LSI Employing Shared Buffer Architecture," *IEEE J. Select. Areas Commun.* vol. 9, pp. 1248-1254, Oct. 1991.

[10] T. R. Banaiza *et al.*, "Design and Technology Aspects of VLSI's for ATM Switches," *IEEE J. Select. Areas Commun.* vol. 9, pp. 1255-1264, Oct. 1991.

[11] Y. S. Yeh, M. G. Hluchyj, and A. S. Acampora, "The Knockout Switch: A simple architecture for high-performance packet switching," *IEEE J. Select. Areas Commun.* vol. 5, pp. 1274-1283, Oct. 1987.

[12] K. Y. Eng, M. J. Karol, and Y. S. Yeh, "A growable Packet (ATM) Switch Architecture: Design Principles and Applications" *IEEE Trans. Commun.* vol. 40, pp. 423-430, Feb. 1992.

[13] M. J. Karol and C. L. I, "Performance Analysis of a Growable Architecture for Broad-Band Packet (ATM) Switching," *IEEE Trans. Commun.* vol. 40, pp. 431-439, Feb. 1992.

[14] T. Nakashima and N. Tokura, "A self-healing to correct address errors in a shared buffer memory switch," *IEICE Trans.*, vol. E.74, pp. 1593-1597, June, 1991.

[15] C. A. Brackett, "Dense Wavelength Division Multiplexing Networks: Principles and Applications," *IEEE J. Select. Areas Commun.* vol. 8, pp. 948-964, Oct. 1987.

[16] C. C. Chen, L. A. Wang and S. Y. Kuo, "A Wavelength Encoded Multi-Channel Optical Bus for Local Area Networks," *IEEE J. Lightwave Technol.*, vol. 14, no. 3, 315-323, Mar. 1996.

[17] C. C. Chen, L. A. Wang and S. Y. Kuo, "High-Speed Wavelength Encoded Multiple-Channel Optical Buses for LAN,".*GLOBECOM'94*, pp. 1533-1537, Nov. 1994.

[18] L. A. Wang and K. C. Lee, "An Opto-Electronic Virtual Bus Using WDM and VLSI technologies for Interconnection Networks," *ICC'92*, Chicago, LA, pp. 888-894, 1992.

[19] Y. Sakurai, N. Ido, S. Gohara, and N. Endo, "Large scale ATM multi-stage switching network with shared buffer memory switches," *ISS'90*, vol. 4, pp. 121-126, 1990.

[20] J. Y. Hui, *Switching and Traffic Theory for Integrated Broadband Networks,* Kluwer Academic Publishers, 1990.

[21] Refer to commercial data sheets of NEC Model 20 and NorTel Model 10.