CMOS Wideband Amplifiers Using Multiple Inductive-Series Peaking Technique

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***Abstract*—This paper presents the technique of multiple inductive-series peaking to mitigate the deteriorated parasitic capacitance in CMOS technology. Employing multiple inductive-series peaking technique, a 10-Gb/s optical transimpedance amplifier (TIA) has been implemented in a 0.18-μm CMOS process. The 10-Gb/s optical CMOS TIA, which accommodates a PD capacitor of 250 fF, achieves the gain of 61 dBΩ and 3-dB frequency of 7.2 GHz. The noise measurement shows the average noise current of 8.2 pA/$\sqrt{\text{Hz}}$ with power consumption of 70 mW.**

***Index Terms*—Inductive-series peaking, transimpedance amplifier, wideband amplifier.**

I. Introduction

With the rapid proliferation of numerous multimedia networking applications, wideband high-speed telecommunication systems, such as 10-Gb/s optical fiber-link applications, are required. These high-speed front-end circuits [1], [2] are required to be high frequency, low cost, and low power dissipation. However, CMOS devices pose difficult design challenges, such as severe parasitic capacitance, lower transconductance, and noise performance, which mandate circuit innovations to tackle with these issues.

The purpose of this paper is to introduce multiple inductive-series peaking technique to overcome the limitations of CMOS technology. This technique can significantly extend circuit bandwidth without penalty of power consumption. Meanwhile, it can have a relatively flat frequency response similar to *LC*-ladder filters. A 10-Gb/s optical transimpedance amplifier (TIA) has been implemented in 0.18-μm CMOS technology to demonstrate the technique of bandwidth extension.

The design of a TIA should meet stringent constraints, such as gain, bandwidth, noise, and dynamic range. With a typical received power of -15 dBm and a photodiode of responsibility of about 0.75 A/W, TIA must afford more than 1 kΩ (60 dBΩ) transimpedance gain to amplify the weak input current to a detectable signal level for the succeeding stage, such as limiting amplifier [3]. Besides, dynamic range has been a critical issue especially for optical fiber links applications. For low-speed optical interconnects, inverter-configuration TIA has been widely adopted [4]. Nevertheless, for high-speed optical fiber link application, such as more than 2.5 Gb/s, inverter-configuration TIA is seldom used due to its low-speed property. In this paper, the inverter-configuration TIA employing the multiple inductive-series peaking technique has been exploited up to 10–Gb/s in CMOS technology, which also possesses low-power and area-efficient features.

The paper is organized as follows. Section II introduces the proposed multiple inductive-series peaking technique. The circuit designs and schematics are also described in this section. Section III presents experimental results of the TIA. Finally, conclusions are given in Section IV.

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II. Multiple Inductive-Series Peaking Technique

The proposed wideband amplifier architecture is shown in Fig. 1(a), where on-chip inductors have been deployed between gain stages. Without employing inductors, amplifier bandwidth is mainly determined by *RC* time constants of every node. In CMOS technology, severe parasitic capacitance deteriorates bandwidth significantly. In the proposed architecture, between gain stages, deployed inductors and parasitic capacitances resemble as a third-order *LC*-ladder filter to perform an impedance transformation network [5], [6].

Considering the inter-stage small-signal model without an inductor in Fig. 1(b), the transfer function can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{-G_m R_T}{1 + sC_T R_T} \tag{1}$$

where R_T denotes $R_{f1}//R_{f2}$, and C_T represents $C_1 + C_2$. R_{f1}/R_{f2} and C_1/C_2 denote equivalent resistors and capacitors contributed by previous and next stages, respectively. The transfer function of Fig. 1(b) can be derived as shown in (2) at the bottom of the next page. Fig. 2 shows the simulated frequency responses of the first- and third-order filters with different inductances from $0.4L_T$ to $1.6L_T$, where L_T denotes the optimal inductance value, $C_1 = C_2$, and $R_{f1} = R_{f2}$. The simulation results show using smaller inductance can improve bandwidth further but also introduce larger peaking magnitude to deteriorate step response. Employing a proper inductance value L_T with an acceptable overshoot peaking, it can be found that the 3-dB bandwidth of the proposed topology is 2.5 times than that without inserting inductors. The bandwidth-extension effect of proposed technique is more apparent for cascading more stages. Fig. 3 shows the simulated 3-dB bandwidths of wideband amplifiers with different cascading stages, where 3-dB frequencies have been normalized with respect to the 3-dB frequency of first-order *RC* filter. It is shown that the 3-dB bandwidth of the proposed amplifier is 6 times than that of a conventional amplifier, which is a quite large factor. The bandwidth of conventional wideband amplifiers is significantly degraded with cascading more stages. However, that of the proposed wideband

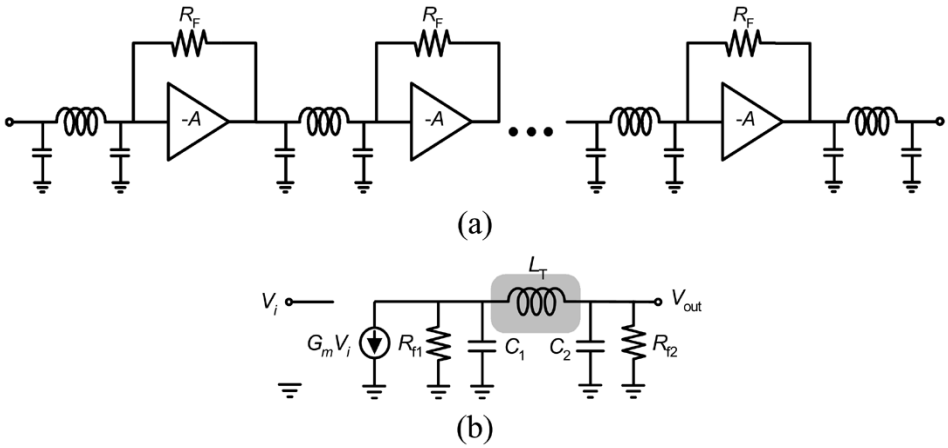


Fig. 1. (a) Proposed wideband amplifier structure. (b) Equivalent inter-stage small-signal model of the proposed amplifier.

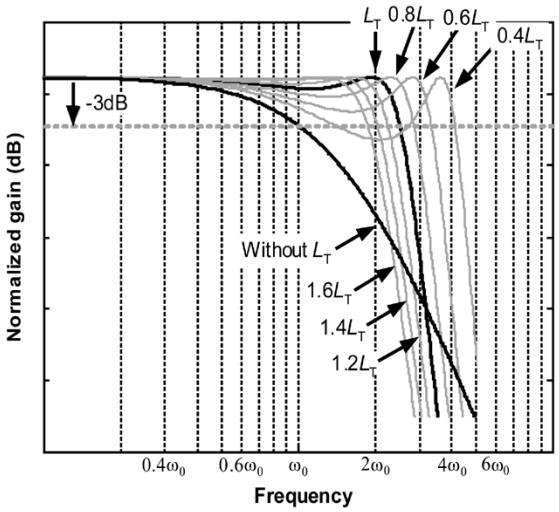


Fig. 2. Comparison between first- and third-order filters with different inductance value.

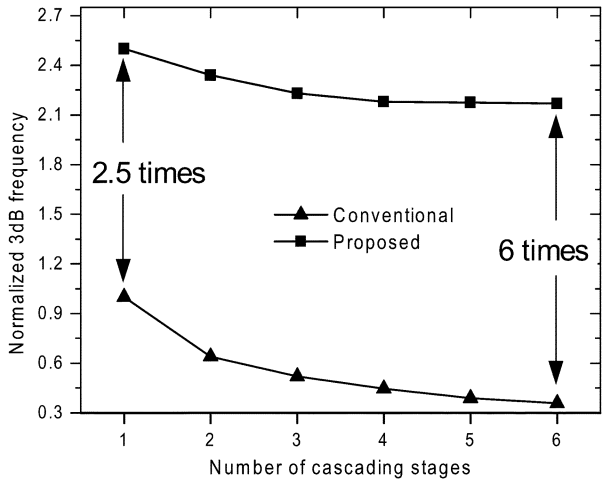


Fig. 3. Simulated 3-dB frequencies versus the number of cascading stages.

amplifier utilizing multiple inductive-series peaking technique is not obviously degraded with cascading more stage, which indicates that the gain and bandwidth trade-off can be ameliorated by the technique.

The proposed TIA is shown in Fig. 4, where on-chip inductors and *M*-derived half circuits have been employed. Photodiode capacitance, which usually performs the dominant pole, and parasitic capacitances can be absorbed as a part of impedance transformation network by utilizing the multiple inductive-series peaking technique. However, the filter structure performs considerable frequency dependence. If terminated to resistive loads directly, the mismatch will deteriorate the filter significantly. To circumvent this issue, *M*-derived half circuits, which exhibit more uniform impedance, have been utilized in input and output matching networks [7]. The circuit simulation result is depicted in Fig. 5(a), which shows the 3-dB frequency of conventional 5-stage inverter-configuration TIA is 2.4 GHz, and the 3-dB frequency of the proposed TIA is 7.4 GHz, which is 3 times larger than the conventional one. Considering trade-offs between noise and inter-symbol interference, the bandwidth is commonly determined by 0.7–0.8 times data rate, hence the simulated bandwidth is sufficient for 10-Gb/s optical fiber link application. Fig. 5(b) shows the simulated gains with different inductor series resistance. It is shown that circuit performance is

$$\frac{V_{out}}{V_{in}} = \frac{-G_m R_T}{1 + s\left[C_T R_T + \frac{L_T}{R_{f1}+R_{f2}}\right] + s^2\left[\frac{R_T L_T C_2}{R_{f1}} + \frac{R_T L_T C_1}{R_{f2}}\right] + s^3 C_1 C_2 L_T R_T} \tag{2}$$

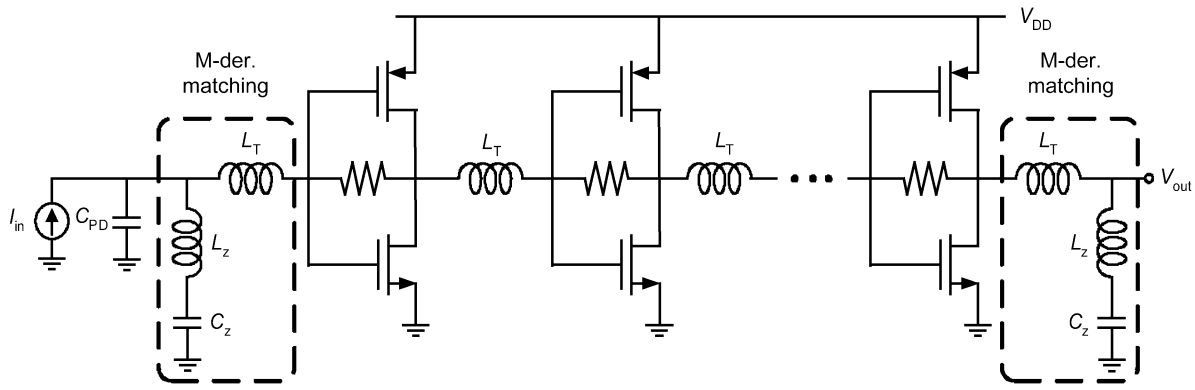
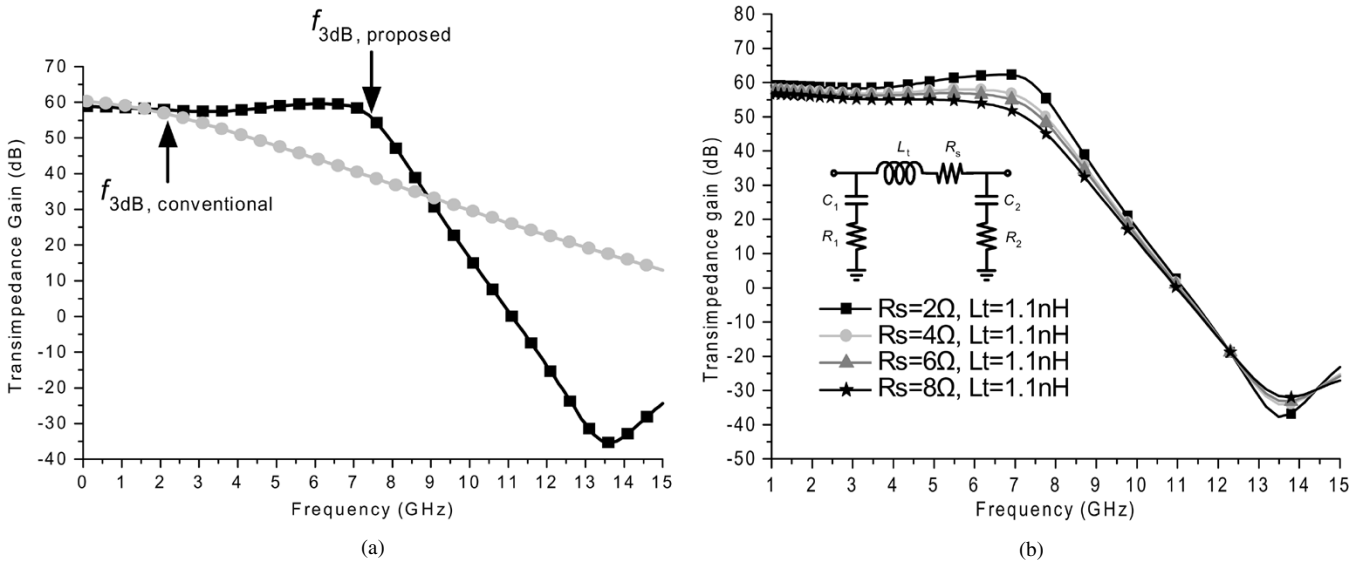


Fig. 4. A 5-stage TIA using proposed multiple inductive-series peaking technique.



(a) (b)

Fig. 5. Simulation results (a) Gains of conventional and proposed TIAs. (b) Proposed TIA's gain versus inductor's series resistance.

insensitive to inductor quality factor. With 50% reduction of inductor quality factor, the gain reduces 2 dB and bandwidth only decreases 3%. Compared to the inductive shunt-peaking technique, which is very sensitive to stray capacitance induced by spiral inductors, the proposed TIA manifests larger bandwidth enhancement and more insensitivity to on-chip inductor quality factor.

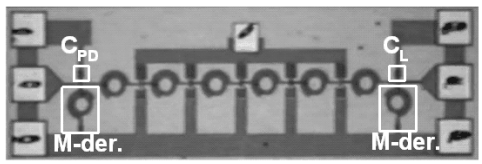


Fig. 6. Die photo of the area-efficient TIA.

III. Experimental Results

The proposed TIA has been implemented in 0.18-μm CMOS technology and measured in on-wafer testing. Fig. 6 shows the die photo. To accurately demonstrate the capability of accommodating PD capacitance and load capacitance, two 250-fF MIM capacitors have been integrated on this chip. Ascribed to be insensitive of inductor quality factors, miniature 3-D inductors have been adopted to further minimize die area [8]. The core circuit area is only 0.14 mm^2, which is almost equal to a 5-nH planar inductor.

Fig. 7 shows the measured gain and group delays. The measured gain is 61 dBΩ and 3-dB frequency is 7.2 GHz. Within 3-dB bandwidth, the average group delay is 275 ps with ripple of about 25 ps. Fig. 8 shows the measured average input equivalent noise current density of 8.2 pA/$\sqrt{\text{Hz}}$.

The measured eye diagrams with $2^{31}-1$ PRBS have been depicted in Fig. 9. The measured output eye diagram is still well open at larger input current of 3.1 mA. Compared to a resistive feedback TIA, the inverter-configuration TIA possesses superior capability to accommodate larger input current. The proposed TIA is well suitable to optical fiber link applications, which needs wide dynamic range requirement.

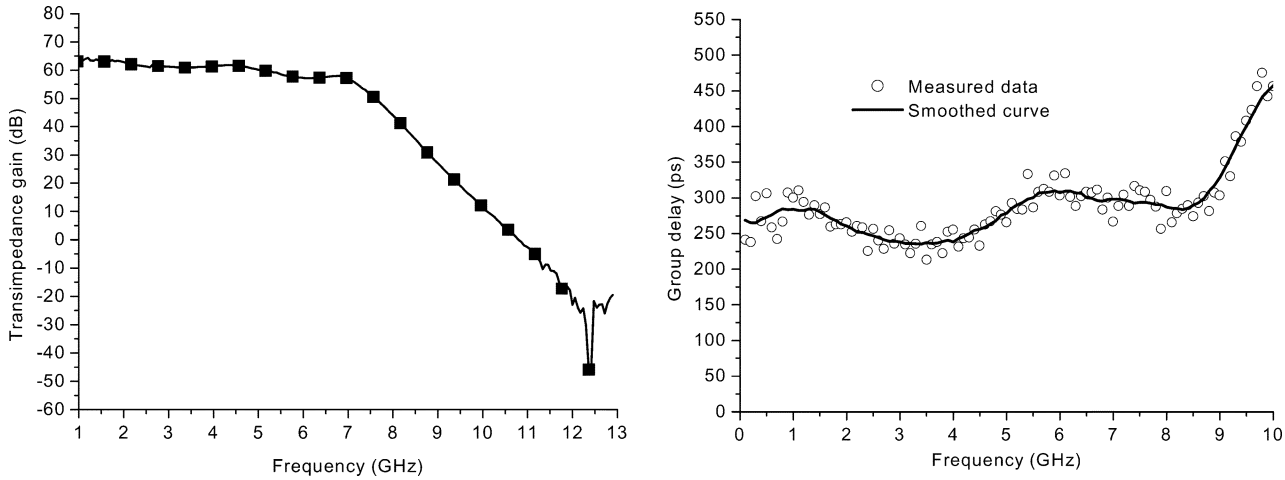


Fig. 7. Measured (a) transimpedance gain and (b) group delays.

TABLE I
SUMMARY OF MEASURED PERFORMANCE AND BRIEF COMPARISON WITH STATE-OF-THE-ART PUBLICATIONS

Reference	This Work	[9]	[10]	[11]
Process	0.18um CMOS	0.18um BiCMOS	0.18um CMOS	0.25um BiCMOS
Supply Voltage	1.8V	2.5V	1.8V	5V
Trans. Gain	1.12 kΩ 61 dBΩ	500 Ω 54 dBΩ	1.3k Ω 62.3 dBΩ	560 Ω 55 dBΩ
-3dB Bandwidth	7.2GHz	9.2GHz	9GHz	9GHz
Speed	10 Gb/s	10 Gb/s	10 Gb/s	10 Gb/s
PD Capacitance	0.25 pF	0.5 pF	0.15 pF	0.15 pF
Sensitivity	10uA (I_{in})	---	---	-17dBm (P_{in})
Input Equivalent Noise	8.2pA/√Hz	< 7pA/√Hz	N/A	9.5pA/√Hz
Power Dissipation	70.2 mW	138 mW	108 mW	140 mW
Chip Area	0.14mm^2	0.64mm^2	N/A	N/A

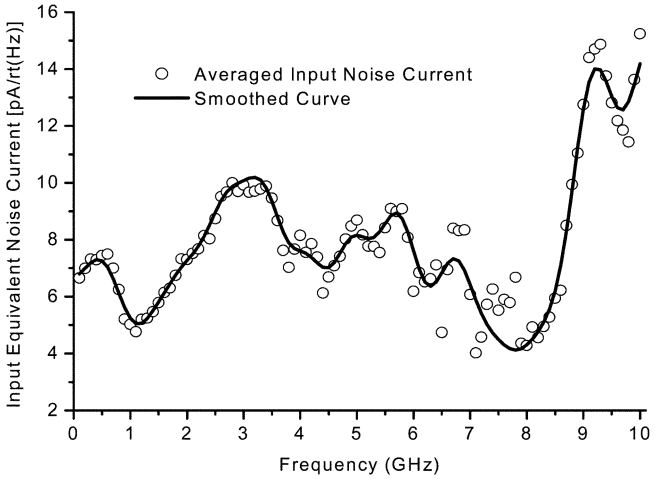
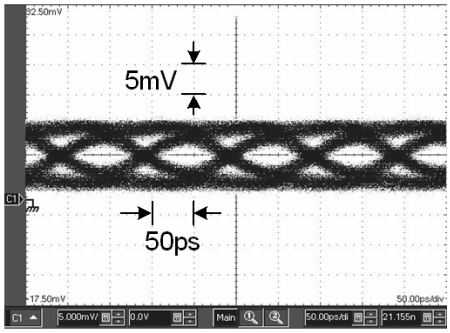


Fig. 8. Measured input equivalent noise current density.

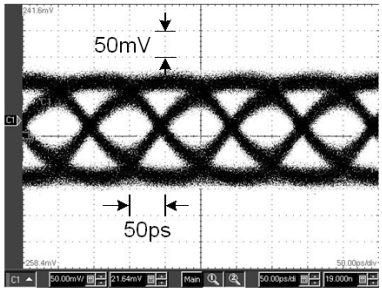
Measured results and the brief comparison with the state-of-the-art 10-Gb/s TIA publications are summarized in Table I. A low-voltage and low-power operation can be achieved by eliminating power-hungry intermediate and output buffers. This fully integrated TIA demonstrates the efficiency of chip area and power consumption, only 0.14 mm^2 and 70.2 mW with a single 1.8-V supply.

IV. CONCLUSION

A bandwidth-extension technique called multiple inductive-series peaking technique has been introduced in this paper. A 10-Gb/s CMOS TIA has been presented to demonstrate the bandwidth-extension technique. Employing the multiple inductive-series peaking technique, the CMOS TIA reported here achieves gain of 61 dBΩ with bandwidth of 7.2 GHz. The measured results demonstrate that the proposed technique of bandwidth extension can improve bandwidth performance significantly. The proposed technique of bandwidth extension is suitable for CMOS devices to achieve wideband and low-power characteristics simultaneously.



(a)



(b)

Fig. 9. Measured eye diagrams. (a) $I_{in} = 10\ \mu\mathrm{A}$. (b) $I_{in} = 0.17\ \mathrm{mA}$ with 10 Gb/s $2^{31} - 1$ PRBS.

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