PMOS Hole Mobility Enhancement Through SiGe Conductive Channel and Highly Compressive ILD-SiN_x Stressing Layer

Wen-Shiang Liao, Yue-Gie Liaw, Mao-Chyuan Tang, Kun-Ming Chen, Sheng-Yi Huang, C.-Y. Peng, and Chee Wee Liu

***Abstract*—In this letter, the SiGe-channel PMOS transistors integrated with a highly compressive contact-etching stop-layer (CESL) interlayer-dielectric-SiN_x stressing layer have been successfully fabricated. The performance improvements of devices with a gate length (L_g) of down to 40 nm were studied. For long-channel SiGe-channel PMOS, the mobility is at least +50% higher than that of the conventional bulk-Si PMOS. Moreover, compared to the conventional short-channel SiGe-channel devices, the highly compressive CESL stressor shows +32% current gain for $L_g = 40$ nm PMOS with the thinnest 9Å Si-cap. Therefore, integrating the stressed CESL technique into the SiGe-channel structure is an efficient method for improving PMOS device performance.**

***Index Terms*—Contact-etching stop layer (CESL), mobility, PMOS, SiGe channel, stressing layer.**

I. Introduction

As THE dimensions of CMOS transistors are scaled to deep submicrometer regimes, device scaling is becoming extremely difficult due to many physical and technological problems [1]. To maintain the scaling trends, new materials and device structures have to be introduced [2]. Recently, silicon–germanium ($Si_{1-x}Ge_x$) has been considered as a promising device conduction layer for submicrometer CMOS channel engineering [3], [4]. Many researches have proved that compressively strained-SiGe or strained-Ge channels could provide a significant mobility gain for long-channel PMOS devices [5]–[7]. The mobility gain under the biaxial compressive strain is attributed to the reduction of the hole effective mass as well as the splitting between the degenerated heavy hole, light hole, and spin-orbit split-off hole bands. On the other hand, various local-strain technologies have been extensively implemented in CMOS devices to improve device performance [8]–[11]. One of the most popular technologies is utilizing the contact-etching stop layer (CESL) to introduce the uniaxial strain in the channel region. For short-channel transistors, a CESL with uniaxial tensile stress improves the n-channel MOSFET performance, while a CESL with uniaxial compressive stress is beneficial for the p-channel MOSFET behavior [8], [10].

The combination of substrate-induced biaxially strained Si-channel CMOS technologies with uniaxial local tensile or compressive stressors to improve the device mobility and drive current has also been studied elsewhere [12]. The engineering challenge is to understand and optimize how the stresses originating from the various methods best interact with one another. However, only a few issues mentioned the uniaxial-strain effects on the SiGe channel [13]. In this letter, we explored the detailed effects of a highly compressive and highly tensile interlayer dielectric (ILD)-SiN_x CESL layer upon the short SiGe-channel PMOS devices for varied gate lengths down to 40 nm.

II. Device Fabrication

To fabricate the SiGe-channel MOSFET devices, 3-μm-thick epi-Si wafers were used with a traditional ultralarge-scale-integration logic 90-nm-generation technology. A shallow-trench-isolation processing and PMOS n-well and threshold implants were processed, followed by a high-temperature well rapid thermal annealing. After removing the remaining sacrificial oxide with dilute hydrofluoric acid, the wafers were sent to epi-grow a SiGe-channel structure composed of buffer-Si/$Si_{1-x}Ge_x(x = 22.5\%)$/cap-Si with an AMAT tool, and the cap-Si were fabricated with 9-, 24-, and 39-Å thickness, respectively. The cap-Si is beneficial to reduce the interface-trap states between the gate dielectric and the SiGe channel [7]. Note that the thicker cap-Si layer can also reduce the surface roughness but would lead to the formation of buried channels. A plasma-nitrided gate oxide of 14 Å (physical thickness) was then grown upon the very thin surface of cap-Si. Subsequently, a 1500-Å-thick undoped polysilicon gate electrode was deposited. To achieve a poly-Si gate length target of 40 nm, both the 193-nm scanner lithography and aggressive oxide hard-mask etching techniques were used. Moreover, heavy PMOS pocket implantations were used to avoid the punch-through of the gate length $L_g = 40$ nm. At the same time, after gate-spacer formation, the P^+ (B) source/drain ion implantation was conducted.

Manuscript received August 17, 2007; revised October 9, 2007. The review of this letter was arranged by Editor C.-P. Chang.

W.-S. Liao, M.-C. Tang, and S.-Y. Huang are with the United Microelectronic Corporation, Hsinchu 308, Taiwan, R.O.C. (e-mail: wen_shiang_liao@umc.com).

Y.-G. Liaw is with the Silicon Integrated Systems Corporation, Hsinchu 300, Taiwan, R.O.C. (e-mail: willy_liaw@sis.com).

K.-M. Chen is with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C. (kmchen@mail.ndl.org.tw).

C.-Y. Peng and C. W. Liu are with the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 10617, Taiwan, R.O.C.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2007.910794

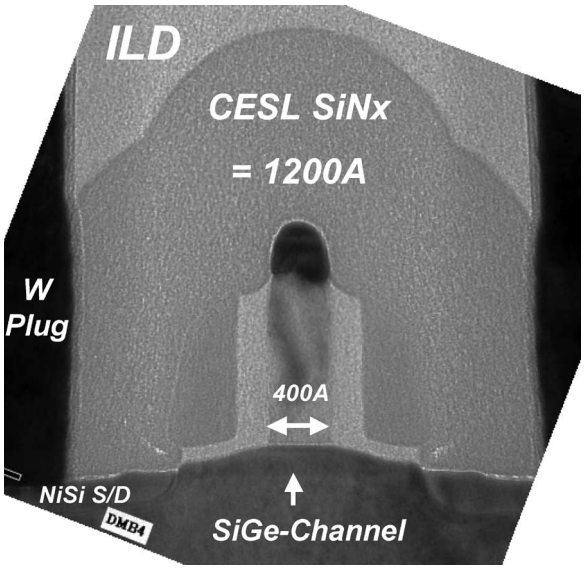

Fig. 1. X-TEM of a SiGe-channel MOSFET with a compressive CESL ILD-SiN_x stressing layer.

To enhance the electrical conductivity of the source/drain integrated with the SiGe-channel layer, a nickel-salicidation process was used, followed by a recipe-varied plasma-enhanced chemical-vapor-deposition 1200-Å-thick ILD-SiN_x CESL layers as a highly compressive (-2.0 GPa) stressing layer and a highly tensile ($+1.41$ Gpa) stressing layer, respectively. For the control devices, the conventional lowly tensile (ILD-SiN_x = 380 Å) CESL layer was used. After ILD-oxide deposition, chemical–mechanical planarization, contact patterning, etching, and W-plug formation, a standard copper-metal interconnection process was processed. Finally, a passivation layer was followed by the formation of aluminum-bonding pads. The X-TEM picture of a fabricated 100-Å-thick $Si_{1-x}Ge_x(x = 22.5\%)$ channel MOSFET with its gate length of 40 nm and a highly compressive 1200-Å-thick ILD-SiN_x stressing layer is shown in Fig. 1.

III. Results and Discussion

Fig. 2 shows the effective hole mobility ($\mu_{\rm eff}$) as a function of the effective vertical electric field ($E_{\rm eff}$) for long-channel ($L_g = 10$ μm) PMOS devices with the thinnest Si-cap thickness of 9 Å. The gate width (W) of the test devices is 10 μm. As shown in Fig. 2, the high-field-mobility performance of the conventional bulk-Si channel PMOS is similar to the universal curve. Under conventional lowly tensile (ILD-SiN_x = 380 Å) CESL layer, a long-channel SiGe-channel PMOS device has a significant mobility gain of 50% as compared to the conventional bulk-Si channel PMOS. This exhibits the great mobility-enhancement ability of the $Si_{1-x}Ge_x(x = 22.5\%)$ conductive layer. The mobility enhancement in SiGe-channel device is due to the lower effective mass of holes in SiGe, and probably, the existence of biaxial compressive strain in the channel which splits the heavy- and light-hole subbands [14]. Fig. 2 also roughly depicts the CESL stressing effect on the mobility. The highly compressive (-2.0 GPa) SiGe-channel exhibits an even

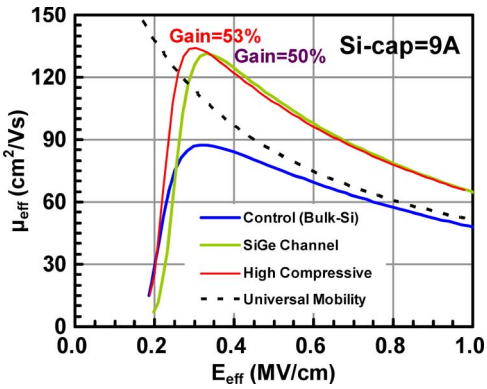

Fig. 2. Mobility comparison of long SiGe channel ($W/L = 10/10$ μm) PMOS devices with the thinnest Si-cap thickness of 9 Å.

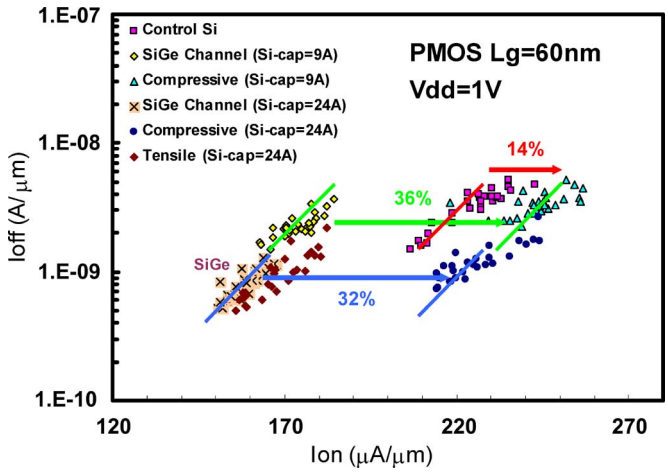

Fig. 3. Universal comparison of a $L_g = 60$ nm SiGe-channel PMOS, with and without the compressive ILD-SiN_x CESL layer.

higher mobility gain of $+53\%$ as compared to the conventional bulk-Si channel PMOS. The insignificant improvement (from $+50\%$ to $+53\%$) may be due to the measurement-error bar and the lesser sensitivity of the long-channel device to the change of the stress in the CESL layer. It only intuitively indicates that the substrate-induced and CESL-induced stresses are additive.

As the gate length is scaled down, the enhancements of hole mobility and drive current for PMOS devices with highly compressive CESL layer will be increased due to the increase of the strain level in the device channel [9]. Fig. 3 shows the $I_{\rm ON}-I_{\rm OFF}$ (at Vdd = 1 V) universal characteristics curves for the SiGe-channel PMOS devices with the gate length of 60 nm. In comparison to the lowly tensile SiGe-channel devices, the $I_{\rm ON}$ improvements of the devices with highly compressive CESL layer are significantly enhanced by $+36\%$ and $+32\%$ for that integrated with 9 and 24 Å Si-cap, respectively. The $I_{\rm ON}$ also shows a 14% enhancement for the 9-Å Si-cap SiGe channel with highly compressive CESL layer as compared to the conventional lowly tensile bulk PMOS. The large $I_{\rm ON}$ improvements for the SiGe channel are mainly attributed to the highly compressive stress induced by the CESL on the

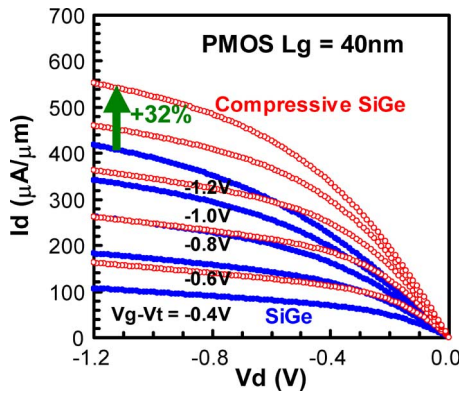

Fig. 4. I_d–V_d characteristic curve of a $L_g = 40$ nm SiGe-channel PMOS, with and without the compressive CESL ILD-SiN_x.

channel of the device. To explain it in detail, the drive-current enhancement depends both on the hole-population distribution across the Si-cap/SiGe-channel layers during inversion and hole mobility in the SiGe channel. The thinner Si-cap thickness (9 Å) results in the higher fraction of the hole-population distribution in the SiGe-channel and leads to the larger $I_{\rm ON}$ as compared to the thicker Si-capped SiGe-channel (24 Å). Furthermore, owing to the higher sensitivity to the hole-mobility enhancement of relaxed Ge than of relaxed Si under the same strain level [7], the 9-Å Si-capped SiGe-channel thus has the larger $I_{\rm ON}$ enhancement (+36%) than the 24-Å Si-capped SiGe-channel (+32%) after capping the highly compressive (−2.0 GPa) stressing layer. Moreover, the thicker Si-cap thickness (24 Å) will further reduce the vertical electrical field in the smaller bandgap SiGe channel, and thus, the lower leakage current $I_{\rm OFF}$ (coming mainly from the band-to-band tunneling current) can be obtained as compared to the thinner Si-cap (9 Å) SiGe channel devices [7]. On the other hand, $I_{\rm ON}$ of the devices with highly tensile CESL layer shows a 5% enhancement for that integrated with 24 Å. Since uniaxial tensile stress is beneficial for the holes in the tensile Si-cap while undesirable for the holes in the compressive SiGe channel, the carrier-population effect may lead to the abnormal enhancement of $I_{\rm ON}$ under highly tensile CESL layer.

Furthermore, the output-characteristic (I_d–V_d) curves in Fig. 4 express good device performance for $L_g = 40$ nm SiGe-channel (Si-cap thickness = 9 Å) PMOS device and a drastic current enhancement of 32% as compared to that of the conventional SiGe-channel PMOS fabricated with lowly tensile 380-Å ILD-SiN_x CESL layer. Excellent on/off ratio (4×10^7) has been obtained (not shown) due to the aid of optimized Si-cap thickness (Si-cap thickness = 9 Å) to reduce the leakage current as compared to the study in [7]. Additionally, the PMOS also displays good subthreshold swing (SS = 100 mv/dec) and drain-induced barrier lowering (DIBL = 0.116 V/V) performed by the highly compressive SiGe-channel (−2.0 GPa).

IV. Conclusion

A SiGe-channel PMOS with a gate length down to 40 nm has been successfully integrated with a nitrided gate oxide of 14 Å, as well as a 1200 Å highly compressive CESL ILD-SiN_x stressing layer. For long SiGe-channel PMOS, the mobility is at least +50% higher than that of the conventional PMOS. Moreover, as compared to the conventional short-channel SiGe-channel devices, the highly compressive CESL stressor shows +32% current gain for $L_x = 40$ nm PMOS with the thinnest 9-Å Si-cap. Therefore, an effective short SiGe-channel mobility engineering is demonstrated for the PMOS device while integrating with the uniaxially highly compressive (beneficial for PMOS) CESL layer and the biaxially substrate-strained SiGe channel.

References

[1] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–288, Mar. 2001.

[2] T. Skotnicki, J. A. Hutchby, T. J. King, H.-S. P. Wong, and F. Boeuf, "The end of CMOS scaling: Toward the introduction of new materials and structural changes to improve MOSFET performance," *IEEE Circuits Devices Mag.*, vol. 21, no. 1, pp. 16–26, Jan./Feb. 2005.

[3] Y. C. Yeo, V. Subramanian, J. Kedzierski, P. Xuan, T. J. King, J. Bokor, and C. Hu, "Design and fabrication of 50-nm thin-body p-MOSFETs with a SiGe heterostructure channel," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 279–286, Feb. 2002.

[4] Y. C. Yeo, Q. Lu, T. J. King, C. Hu, T. Kawashima, M. Oishi, S. Mashiro, and J. Sakai, "Enhanced performance in sub-100 nm CMOSFETs using strained epitaxial silicon–germanium," in *IEDM Tech. Dig.*, Dec. 2000, pp. 753–756.

[5] G. Höck, E. Kohn, C. Rosenblad, H. von Känel, H.-J. Herzog, and U. Königet, "High hole mobility in $Si_{0.17}Ge_{0.83}$ channel metal–oxide–semiconductor field-effect transistors grown by plasma-enhanced chemical vapor deposition," *Appl. Phys. Lett.*, vol. 76, no. 26, pp. 3920–3922, Jun. 2000.

[6] C. Jungermann, S. Keith, and B. Meinerzhagen, "Full-band Monte Carlo simulation of a 0.12 μm-Si-PMOSFET with and without a strained SiGe-channel," in *IEDM Tech. Dig.*, Dec. 1998, pp. 897–900.

[7] T. Krishnamohan, Z. Krivokapic, K. Uchida, Y. Nishi, and K. C. Saraswat, "High-mobility ultrathin strained Ge MOSFETs on bulk and SOI with low band-to-band tunneling leakage: Experiments," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 990–999, May 2006.

[8] L. Washington *et al.*, "pMOSFET with 200% mobility enhancement induced by multiple stressors," *IEEE Electron Device Lett.*, vol. 27, no. 6, pp. 511–513, Jun. 2006.

[9] S. Pidin, T. Mori, K. Inoue, S. Fukuta, N. Itoh, E. Mutoh, K. Ohkoshi, R. Nakamura, K. Kobayashi, K. Kawamura, T. Saiki, S. Fukuyama, S. Satoh, M. Kase, and K. Hashimoto, "A novel strain enhanced CMOS architecture using selectively deposited high tensile and high compressive silicon nitride films," in *IEDM Tech. Dig.*, Dec. 2004, pp. 213–216.

[10] C. T. Lin, Y. K. Fang, W. K. Yeh, C. M. Lai, C. H. Hsu, L. W. Cheng, and G. H. Ma, "Impacts of notched-gate structure on contact etch stop layer (CESL) stressed 90-nm nMOSFET," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 376–378, May 2007.

[11] R. A. Bianchi, G. Bouche, and O. Roux-dit-Buisson, "Accurate modeling of trench isolation induced mechanical stress effects on MOSFET electrical performance," in *IEDM Tech. Dig.*, Dec. 2002, pp. 117–120.

[12] A. V.-Y. Thean, L. Prabhu, V. Vartanian, M. Ramon, B.-Y. Nguyen, T. White, H. Collard, Q.-H. Xie, S. Murphy, J. Cheek, S. Venkatesan, J. Mogab, C. H. Chang, Y. H. Chiu, H. C. Tuan, Y. C. See, M. S. Liang, and Y. C. Sun, "Uniaxial-biaxial stress hybridization for super-critical strained-Si directly on insulator (SC-SSOI) PMOS with different channel orientations," in *IEDM Tech. Dig.*, Dec. 2005, pp. 509–512.

[13] S. Jakschik, T. Hoffman, H.-J. Cho, A. Veloso, R. Loo, S. Hyun, H. Sorada, A. Inoue, M. D. Potter, G. Eneman, S. Severi, P. Absil, and S. Biesemans, "A 50 nm high-k poly silicon gate stack with a buried SiGe channel," in *Proc. VLSI-TSA*, 2007, p. 30.

[14] D. K. Nayak, J. C. S. Woo, J. S. Park, K. L. Wang, and K. P. MacWilliams, "Enhancement-mode quantum-well Ge_xSi_{1-x} PMOS," *IEEE Electron Device Lett.*, vol. 12, no. 4, pp. 154–156, Apr. 1991.