A 2.17-dB NF 5-GHz-Band Monolithic CMOS LNA With 10-mW DC Power Consumption

Hung-Wei Chiu, Shey-Shi Lu, *Senior Member, IEEE*, and Yo-Sheng Lin, *Member, IEEE*

***Abstract*—Design principles of CMOS low-noise amplifiers (LNAs) for simultaneous input impedance and noise matching by tailoring device size for $R_{\rm opt} = 50\ \Omega$ are introduced. It is found that $R_{\rm opt}$ close to 50 Ω can be obtained by using small devices (110 μm) and small currents (5 mA). Based on the proposed approach, CMOS LNAs with on-chip input and output matching networks on thin ($\sim$ 20 μm) and normal (750 μm) substrates are implemented. It is found that the noise figure (NF) (3.0 dB) of the CMOS LNA at 5.2 GHz with 10-mW power consumption on the normal (750 μm) substrate can be reduced to 2.17 dB after the substrate is thinned down to $\sim$ 20 μm. The reduction of NF is attributed to the suppression of substrate loss of the on-chip inductors. The input return loss (S_{11}) is smaller than −22 dB across the entire band of interest (5.15–5.35 GHz). An input 1-dB compression point ($P_{1\ \rm dB}$) of −8.3 dBm and an input third-order intercept point of 0.8 dBm were also obtained for the LNA on the thin substrate.**

***Index Terms*—Low-noise amplifier (LNA), MOSFET amplifier, noise figure (NF), thin substrate.**

I. Introduction

HIGH data-rate (up to 50 Mb/s) wireless local area networks (LANs), which exploit the 300-MHz bandwidth in the 5-GHz frequency band (5.15–5.35/ 5.725–5.825 GHz) released by the Federal Communications Commission (FCC) for the unlicensed national information infrastructure (UNII) have become increasingly popular and important for mobile computing devices such as notebook computers. The allocated frequencies overlap the European standard for the high-performance radio local area network (HIPERLAN), which also operates in the 5-GHz band (5.15–5.35/5.47–5.725 GHz). Recently, many C-band low-noise amplifiers (LNAs) have been implemented in various technologies for these LAN systems with excellent noise performance [1]–[14]. However, some of the LNAs with extremely low noise figures (NFs) were achieved at the expense of very high dc power consumption, and others suffered from high input/output return losses (> -10 dB), insufficient dynamic range ($P_{1\ \rm dB} < -20$ dBm), or low linearity [input third-order intercept point (input IP3)]. Ultra-low NF is generally not necessary in short-range wireless applications, while low power dissipation to extend the battery life is strongly demanded for portable wireless data applications [5]. Table I is a summary of recent reports on C-band LNAs with low dc power consumption (< 15 mW). From Table I, it is clear that CMOS integrated circuits, which are receiving much attention due to their potential for low cost and the prospect of system-level integration [15], must equal to or surpass the low power consumption (~ 10 mW) and low NF (< 3.0 dB) of the bipolar and GaAs circuits in order to compete with them. Besides, as previously mentioned, good input/output match, sufficient linearity, and high dynamic range are required as well. In commercial and consumer applications, the cost must also be kept low. One solution to this is the use of a foundry process with proven yield and reliability to fabricate the circuits with on-chip input/output matching networks.

Therefore, there is a need to implement an LNA, which can simultaneously balance all of the following constraints:

1) low NF (< 3.0 dB);
2) low dc power consumption (< 15 mW);
3) low input/output return losses (< -10 dB);
4) sufficient input $P_{1\rm dB}$ (> -20 dBm);
5) high input IP3 (> -10 dBm);
6) low cost.

In this paper, we describe 5-GHz-band CMOS LNAs on both thin (~ 20 μm) and normal (750 μm) substrates, which meet all the above requirements. The purpose of silicon substrate thinning of the LNA is to study the effect of silicon substrate thickness on the NF performance. The emphasis of this study is to reduce the power consumption of the CMOS LNA while still retaining acceptable noise performance, good input/ output match, sufficient linearity, and a high dynamic range. A single-stage cascode amplifier topology with inductive degeneration at the source was used. In the course of developing such an LNA, a formula of the NF for a field-effect transistor (FET) with source and gate inductors was derived to facilitate circuit design. Based on the derived formula and the careful selection of the device size and bias, the gate inductor and source inductor, a CMOS on-chip matched LNA with a normal (750 μm) substrate for 802.11a and HIPERLAN2 receivers exhibiting NFs of 2.7, 3.0, and 3.3 dB, input return losses of −27, −30, and −29 dB, output return losses of −15, −15, and −16 dB, $P_{1\ \rm dB}$ of −8.36, −8.3, and −8.33 dBm, input IP3 of 0.3, 0.3, and 0.4 dBm with power consumptions of 12, 10 and 3.6 mW, respectively, were demonstrated experimentally (see Table I). In addition, it was found that the NF (2.17 dB) of the LNA with power consumption of 10 mW on a thin substrate (20 μm) was better than that (3 dB)

Manuscript received March 16, 2004; revised May 11, 2004. This work was supported under Grant NSC92-2212E002-091, Grant 91EC17A05-S10017, and Grant NSC93-2752-E002-002-PAE and by the United Microelectronics Company (UMC) under the UMC University Program.

H.-W. Chiu was with the Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. He is now with the Mixed-Mode and RF Library Division, Taiwan Semiconductor Manufacturing Company, Taiwan, R.O.C.

S.-S. Lu is with the Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. (e-mail: sslu@ntu.edu.tw).

Y.-S. Lin is with the Department of Electrical Engineering, National Chi-Nan University, Puli, Taiwan, R.O.C. (e-mail: stephenlin@ncnu.edu.tw).

Digital Object Identifier 10.1109/TMTT.2004.842510

TABLE I
SUMMARY OF THE STATE-OF-THE-ART C-BAND LNAs

References	f_c	NF	Gate Length	P_{DC}	Gain	input return loss	output return loss	IIP3	P_{1dB} (input)
	(GHz)	(dB)	(μm)	(mW)	(dB)	(dB)	(dB)	(dBm)	(dBm)
This Work (CMOS, Before Thinning Down)	5.2	3.3	0.25	3.6	8.0	-29	-16	0.4	-8.33
	5.2	3.0	0.25	10	10	-30	-15	0.3	-8.3
	5.2	2.7	0.25	12	11.5	-27	-15	0.3	-8.36
This Work (CMOS, After Thinning Down)	5.2	2.17	0.25	10	11	-45	-15	0.3	-8.3
MESFET[4]	5.5	3.5	0.7	9.9	14.85	na	na	na	-21
MESFET[5]	5	1.9	0.6	13.2	10.9	-21	-10	5	na
MESFET[6]	5	1.8	0.6	6	16.5	-16	-4	-6	-16
SiGe HBT[7]	5.8	2.1*	0.5×10 (emitter)	13	13	-6	-4	-10.5	-21
CMOS[8]	5	4.8	0.24	7.2	18+	-12	na	na	na
CMOS[9]	5.25	5.3	0.25	6	6.8	-10.4	-11.6	-3.5	3.3
	5.25	3.5	0.25	12	11.6	-10.9	-12.4	-1.5	-8.7
	5.25	2.5	0.25	48++	16	-12.3	-11.9	-1.5	-11.7
CMOS[10]	5.2	2.1	0.25	9	17	-10	na	na	na
CMOS[11]	5.25	4.5	0.35	10	15.5+	-15	na	5.6	-1.5
CMOS[12]	5.75	1.8**	0.18	21.6++	14.1	-11	-11	4.2	0
CMOS[13]	5.2	2.45	0.35	26.4++	19.3	na	na	-6.1	na

*: input off-chip matching; **: input off-chip matching & dual-gate layout
+: voltage gain; ++: $P_{DC} > 15$ mW

of the LNA on a normal substrate (750 μm) [16]. The reduction of the NF of an LNA with a thin substrate is mainly due to reduction of the substrate loss of the inductors in the LNA.

II. PRINCIPLES OF CIRCUIT DESIGN

The schematic of the popular source–inductor–feedback amplifier with the gate inductor for input impedance matching is shown in Fig. 1(a). Fig. 1(b) shows an equivalent circuit of Fig. 1(a) for noise calculation. The source inductor L_S is used to achieve simultaneous input and noise matching [15]–[18] and to provide the desired input resistance (50 Ω) [19]. To thoroughly understand the effect of source inductance on the NF of an FET quantitatively, a formula of the NF for an FET with source and gate inductors was derived and is detailed as follows.

A. NF of an FET With Source and Gate Inductors

By extending the noise theory for an FET *without* a source inductor published by Pucel *et al.* [20] and referring to Fig. 1(b), we have derived the NF F for an FET *with* source and gate inductors as follows:

$$F = 1 + \frac{1}{R_S}\left\{ R_g + R_{\ell g} + R_{\ell f} + R_f + |Z_t|^2 \frac{\overline{|i_g^2|}}{4kT\Delta f} + \left|\frac{1 + j\omega C_{\rm gs} Z_t}{g_m}\right|^2 \cdot \frac{\overline{|i_d^2|}}{4kT\Delta f} - 2{\rm Re}\left[Z_t \left(\frac{1 + j\omega C_{\rm gs} Z_t}{g_m}\right)^* \frac{\overline{i_g^* i_d}}{4kT\Delta f}\right]\right\} \quad (1)$$

where R_S is the signal source resistance (usually 50 Ω), R_g and R_f represent gate and source parasitic resistances of the FET,

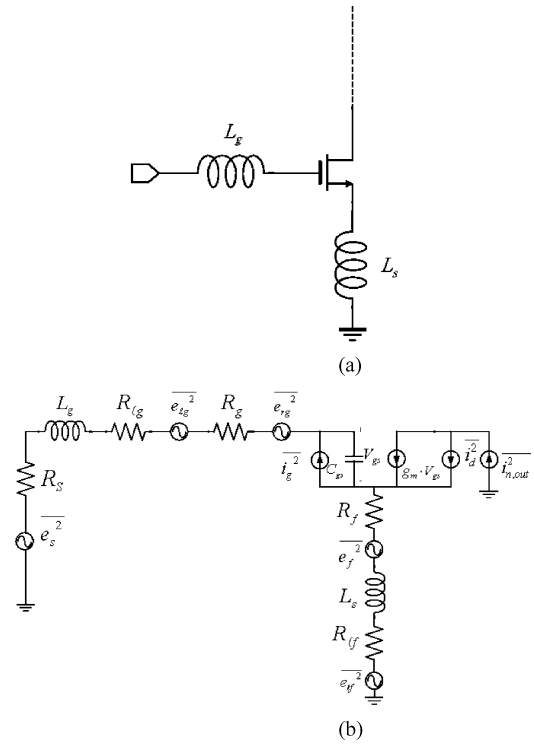

Fig. 1. (a) Schematic of the popular source–inductor–feedback amplifier with an input matching gate inductor. (b) Equivalent circuit of Fig. 1(a) for noise calculation.

respectively, $R_{\ell g}$ and $R_{\ell f}$ stand for the series resistance of the inductors L_g and L_S, respectively, $Z_t = Z_S + R_g + R_f + R_{\ell g} + R_{\ell f} + j\omega(L_g + L_S)$, Z_S is the source impedance of the signal source, g_m is the transconductance of the FET, $C_{\rm gs}$ is

the gate-to-source capacitance of the FET, k is the Boltzmann constant, T is absolute temperature, f is frequency, i_g is the induced gate noise current, and i_d is the drain noise current. Re denotes "the real part of."

i_g and i_d can be written as

$$\overline{|i_g^2|} = R\frac{\omega^2 C_{\rm gs}^2}{g_m} 4kT\Delta f \tag{2}$$

$$\overline{|i_d^2|} = P g_m 4kT\Delta f \tag{3}$$

where R and P are the coefficients of gate and drain noise, respectively, and are equal to $(\delta\cdot\alpha)/5$ and γ/α if the symbols in [21] and [22] are used, where δ is the coefficient of gate noise, γ is the coefficient of drain noise, and α is the ratio of device transconductance to zero-bias drain conductance.

In fact, the expression for F can be put in the following useful form by inserting (2) and (3) into (1):

$$F = 1 + \frac{R_u + G_n\left|Z_S + Z_C\right|^2}{R_S} \tag{4}$$

where R_u, G_n, and Z_C are defined as follows:

$$R_u \equiv R_g + R_{\ell g} + R_{\ell f} + R_f + \frac{K_r}{g_m} \tag{5}$$

$$G_n \equiv K_g\frac{\omega^2 C_{\rm gs}^2}{g_m} \tag{6}$$

$$\begin{aligned} Z_C &\equiv R_C + jX_C \\ &= R_g + R_{\ell g} + R_{\ell f} + R_f + \frac{K_C}{j\omega C_{\rm gs}} + j\omega(L_g + L_S). \end{aligned} \tag{7}$$

Comparing (5)–(7) with (35)–(37) derived in the Appendix, it can be seen that K_g, K_c, and K_r are the functions of P, R, and C as follows:

$$K_g = P\left[\left(1 - C\sqrt{\frac{R}{P}}\right)^2 + \frac{(1-C^2)R}{P}\right] \tag{8}$$

$$K_c = \frac{1 - C\sqrt{\dfrac{R}{P}}}{\left(1 - C\sqrt{\dfrac{R}{P}}\right)^2 + \dfrac{(1-C^2)R}{P}} \tag{9}$$

$$K_r = \frac{\dfrac{(1-C^2)R}{P}}{\left(1 - C\sqrt{\dfrac{R}{P}}\right)^2 + \dfrac{(1-C^2)R}{P}}. \tag{10}$$

C is the correlation coefficient of i_g and i_d defined by

$$jC = \frac{\overline{i_g^* i_d}}{\sqrt{\overline{|i_g^2|}}\cdot\sqrt{\overline{|i_d^2|}}}. \tag{11}$$

Theoretically, the value of C is 0.395 for a long channel device [21]. Since R and P are difficult to extract from the measured results, we shall consider these K functions as our fundamental noise coefficients, which can be estimated from the measured noise parameters ($R_{\rm opt}$, $X_{\rm opt}$, $F_{\rm min}$, and R_n), as will be described shortly. The expression of NF F in (4) is usually written in terms of minimum NF $F_{\rm min}$, and the optimal source impedance $Z_{\rm opt} = R_{\rm opt} + jX_{\rm opt}$ or source admittance $Y_{\rm opt} = G_{\rm opt} + jB_{\rm opt}$ as follows:

$$F = F_{\rm min} + \frac{G_n}{R_S}\left|Z_S - Z_{\rm opt}\right|^2 \tag{12}$$

$$= F_{\rm min} + \frac{G_n}{R_S}\left|Z_S - R_{\rm opt} - jX_{\rm opt}\right|^2 \tag{13}$$

$$= F_{\rm min} + \frac{R_n}{G_S}\left|Y_S - G_{\rm opt} - jB_{\rm opt}\right|^2 \tag{14}$$

where $R_{\rm opt}$, $X_{\rm opt}$, $F_{\rm min}$, and R_n are given by (15)–(19), shown at the bottom of this page. Now, several observations are described in order here. For the time being, let us suppose that $L_g = 0$. From (18), we know that the introduction of L_S, to a first-order approximation, does not affect $F_{\rm min}$, which is consistent with the experimental results [23]. According to (15) and (17), it is also interesting to note that $R_{\rm opt}$ is independent of L_S, while $X_{\rm opt}$ is reduced when L_S is introduced; i.e., $Z_{\rm opt}$ in the Smith chart should follow a constant resistance ($R_{\rm opt}$) circle with decreasing reactance ($X_{\rm opt}$) when L_S increases, as shown in Fig. 2(a), which, to a first-order approximation, agrees

---

$$R_{\rm opt} = \sqrt{R_C^2 + \frac{R_u}{G_n}} \tag{15}$$

$$= \sqrt{(R_g + R_{\ell g} + R_{fg} + R_f)^2 + \frac{(R_g + R_{\ell g} + R_{fg} + R_f)g_m}{K_g\omega^2 C_{\rm gs}^2} + \frac{K_r}{K_g\omega^2 C_{\rm gs}^2}}$$

$$= \sqrt{(R_g + R_{\ell g} + R_{fg} + R_f)^2 + \frac{(R_g + R_{\ell g} + R_{fg} + R_f)\omega_T^2}{K_g g_m} + \frac{K_r\omega_T^2}{K_g g_m^2}} \tag{16}$$

$$\begin{aligned} X_{\rm opt} &= -X_C \\ &= \frac{K_C}{\omega C_{\rm gs}} - \omega(L_g + L_S) \end{aligned} \tag{17}$$

$$F_{\rm min} = 1 + 2G_n\left(R_C + R_{\rm opt}\right) \tag{18}$$

$$\begin{aligned} R_n &= R_u + G_n\left|Z_C\right|^2 \\ &= G_n\left(R_{\rm opt}^2 + X_{\rm opt}^2\right) \end{aligned} \tag{19}$$

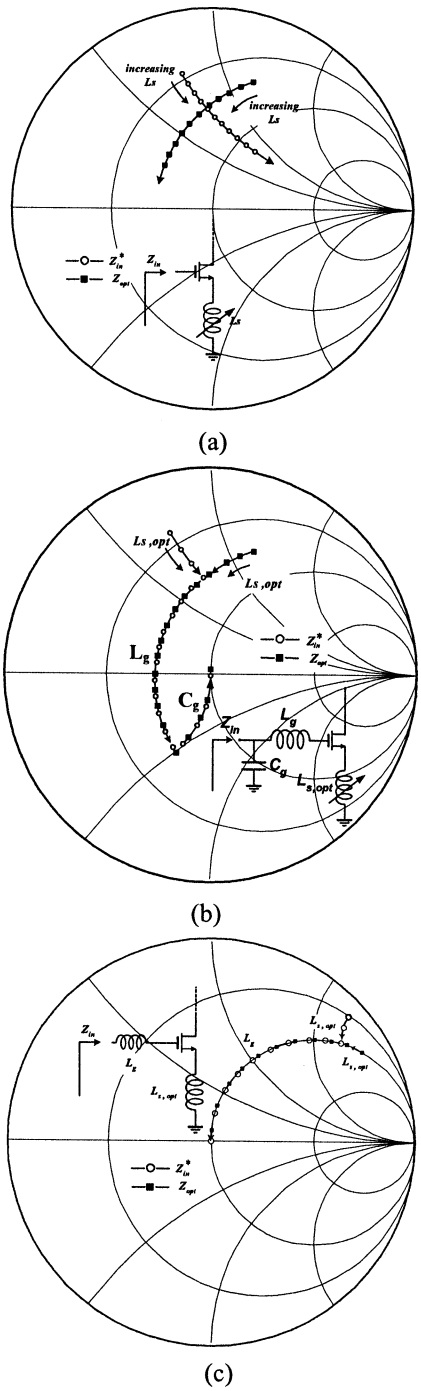

Fig. 2. Loci of $Z_{\rm opt}$ and $Z_{\rm in}^*$ in the Smith chart with increasing L_g and L_s. (a) To a first-order approximation, $Z_{\rm opt}$ follows a constant resistance circle with decreasing reactance ($X_{\rm opt}$) when L_g and L_s are increased and the loci of $Z_{\rm opt}$ and $Z_{\rm in}^*$ intercept at some point. (b) The loci of $Z_{\rm opt}$ and $Z_{\rm in}^*$ in the Smith chart with L_g, C_g, and L_s. (c) The loci of $Z_{\rm opt}$ and $Z_{\rm in}^*$ in the Smith chart with L_g and L_s when $R_{\rm opt} = 50\ \Omega$ is required.

with the published experimental data [17]. On the other hand, the input impedance $Z_{\rm in}$ of the LNA is given by

$$Z_{\rm in} = R_g + R_{\ell g} + R_{\ell f} + R_f + \frac{g_m L_S}{C_{\rm gs}} + \frac{1 + g_m R_f}{j\omega C_{\rm gs}} + j\omega\left(L_g + L_S\right) \quad (20)$$

if gate-to-drain capacitance ($C_{\rm gd}$) and output resistance (R_o) of the FET are neglected (and, correspondingly, the termination condition applied to the drain is immaterial). The locus of the complex conjugate of the input impedance $Z_{\rm in}^*$ with increasing L_S is also shown in Fig. 2(a). The two loci intercept at some point, which stands for the simultaneous impedance and noise matching if $K_c = 1$ and if a suitable source inductor $L_{S,\rm opt}$ is chosen. Note that, if $K_c \neq 1$, *it is impossible to achieve impedance matching and noise matching simultaneously*. Therefore, it is important for a circuit designer to check whether the K_c of the CMOS process that will be used is close to 1 or not before the source inductor feedback technique can be used for simultaneous input and noise matching. We will discuss the value of K_c later. For the time being, if we assume $K_c = 1$, then a matching network consisting of L_g and C_g can be used to transform the signal source impedance (usually 50 Ω) into this intercept point, as shown in Fig. 2(b). For the ease of matching, one may even eliminate the need of C_g if $Z_{\rm opt} = R_{\rm opt} + jX_{\rm opt}$ is chosen to be $50\ \Omega + j0\ \Omega$. According to (15), it is doable to modify $R_{\rm opt}$ by a careful selection of transistor size ($C_{\rm gs}$) and transconductance (g_m) or bias. $L_{S,\rm opt}$ is then selected so that $\mathrm{Re}(Z_{\rm in})$ ($\sim g_m L_{S,\rm opt}/C_{\rm gs}$) is also 50 Ω and $Z_{\rm opt}$ and $Z_{\rm in}^*$ are coincident at a point on the constant 50-Ω circle in the Smith chart. Nevertheless, from (17), it is, in general, not possible to reduce $X_{\rm opt}$ to zero by merely changing transistor parameters or by the use of $L_{S,\rm opt}$. Hence, a gate inductor L_g must be added to reduce $X_{\rm opt}$ to zero in order to achieve the minimum NF condition ($Z_{\rm opt} = 50\ \Omega + j0\ \Omega$). The loci of $Z_{\rm in}^*$ and $Z_{\rm opt}$ corresponding to this situation are shown in Fig. 2(c). Also note that when $X_{\rm opt}$ ($= -X_c$) is reduced, R_n is reduced as well according to (19). However, one must be cautious that $L_g + L_S$ should not be too large or $X_{\rm opt}$ may become negative, and both the NF and R_n will increase accordingly.

B. Design Procedure of the Source-Inductor-Feedback LNA

Suppose that an LNA in an RF receiver is preceded by a high-frequency bandpass filter whose output resistance is 50 Ω, then $Z_S = 50\ \Omega + j0\ \Omega$. As previously mentioned, $R_{\rm opt}$ has to be 50 Ω and $X_{\rm opt}$ has to be zero in order to achieve the minimum NF $F_{\rm min}$ if we want to avoid additional input matching components other than L_g. According to (15), $R_{\rm opt}$ can be set to 50 Ω by choosing suitable g_m and $C_{\rm gs}$ if K_g and K_r are known. Similarly, $X_{\rm opt}$ can be reduced to zero by choosing suitable $L_g + L_S$ if K_c is given. K_g, K_c, and K_r can be estimated from the measured R_n, $R_{\rm opt}$, and $X_{\rm opt}$ of an FET *without* source and gate inductors (i.e., $L_g = L_S = R_{\ell g} = R_{\ell f} = 0$) based on the following proposed steps. First of all, G_n can be determined by (19). Second, K_g can be determined by (6). Third, K_r can be determined by (16). Finally, K_c can be determined by (17). K_g, K_c, and K_r were estimated from a test device before the design of the LNAs studied in this paper. It is found that K_g, K_c, and K_r are weak functions of frequency [see Fig. 3(a)]. In addition, K_c is 1 within an experimental uncertainty. Therefore, at least for the current CMOS process, impedance matching and noise matching can be achieved simultaneously. Besides, as shown in Fig. 3(b)–(d), the agreements between the predicted and experimental values of $R_{\rm opt}$, $X_{\rm opt}$, and $F_{\rm min}$ are quite satisfactory for the design of LNAs.

As mentioned before, in an average modern CMOS process, whether K_c is always close to 1 or not is crucial. From (9), K_c is

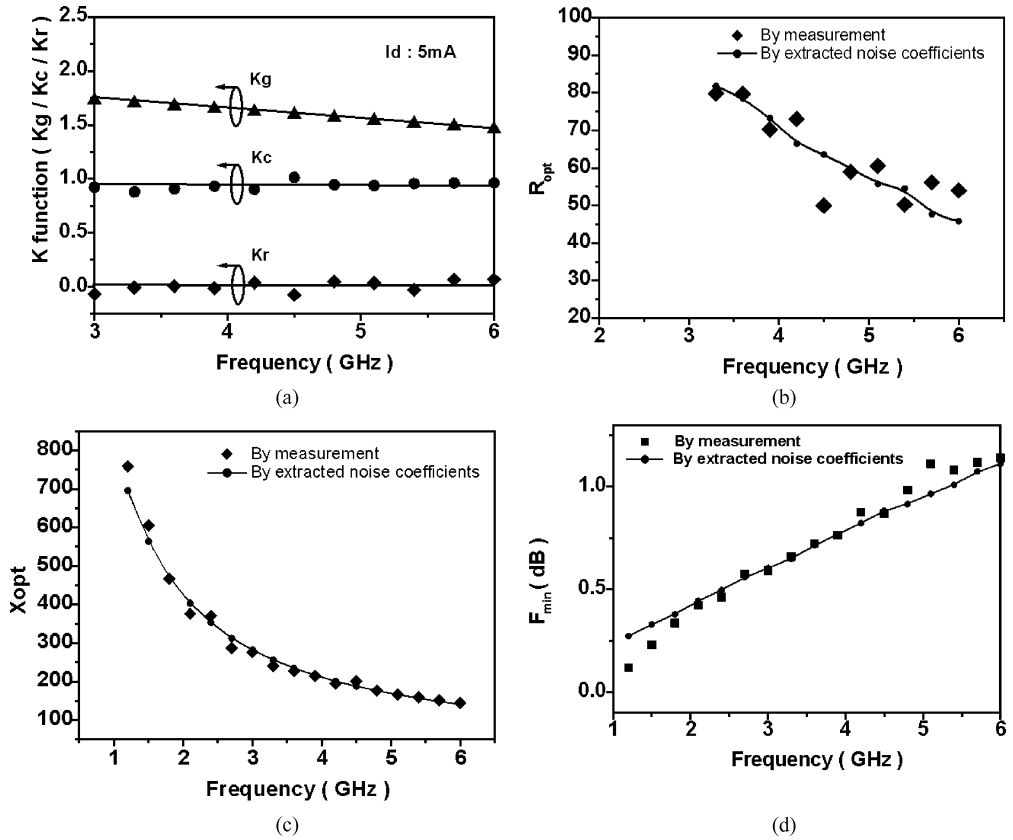

Fig. 3. (a) Extracted K_g, K_c, and K_r versus frequency characteristics of a MOSFET *without* source and gate inductors (i.e., $L_g = L_S = R_{\ell g} = R_{\ell f} = 0$). (b) Comparison between predicted and experimental $R_{\rm opt}$. (c) Comparison between predicted and experimental $X_{\rm opt}$. (d) Comparison between predicted and experimental $F_{\rm min}$.

a function of the ratio R/P, and C. Since C in the short-channel regime is not currently known, we have assumed C to be equal to its long channel value (i.e., 0.395), as was done in [22]. The values of K_c versus R/P based on (9) are plotted in Fig. 4. From this figure, it is clear that when R/P is beyond 0.042, K_c is a monotonically decreasing function of R/P. Since the ratio R/P can be interpreted physically as the relative contribution of gate noise and drain noise to the total noise, we may say that K_c deviates from 1 substantially if the gate noise plays an important role in a device. Some specific values of R/P ($= 0.2 \cdot (\delta/\gamma)^2 \cdot \alpha^2$) may be given to get a feeling of the values of K_c. For a long-channel FET, $\gamma = 2/3$ and $\delta = 4/3$ (twice γ) [21]. For a short-channel device, the assumptions made in [22] are adopted, i.e., δ continues to be approximately twice as large as γ and, hence, although γ and δ are taken as 1–2 and 2–4, respectively, the ratio δ/γ is still a constant 2. Now K_c is only a function of α. If $\alpha = 1$ and $\alpha = 0.85$ were used for long- and short-channel devices [22], respectively, then the calculated ratio R/P can be summarized as

$$\frac{R}{P} = \frac{1}{5} \cdot \left(\frac{\delta}{\gamma}\right) \cdot \alpha^2 = 0.4 \cdot \alpha^2 = \begin{cases} 0.4 & \text{(long channel)} \\ 0.289 & \text{(short channel).} \end{cases} \tag{21}$$

From (21) and Fig. 4, the corresponding K_c is 0.833 and 0.911 for long- and short-channel devices, respectively. Therefore, for an average modern CMOS process, K_c should be close to 1. In addition, K_g, K_c, and K_r are functions of R/P and C from (8)–(10). If C is assumed to be equal to its long channel value

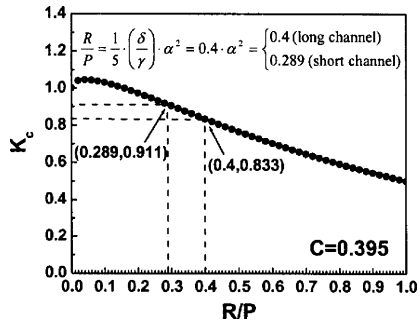

Fig. 4. Calculated K_c versus R/P characteristics of modern CMOS technologies.

(i.e., 0.395), then α (the indication of the gate length) is the only parameter that most strongly affect the values of the three K-parameters, i.e., process parameters highly related to gate length (L_g) will most strongly affect the values of the three K-parameters.

The complete schematic of our LNA is shown in Fig. 5. A single-stage topology is chosen to minimize the power dissipation and to improve input 1-dB compression point ($P_{1\ \rm dB}$) and input IP3 [15]. A cascode configuration is used to improve stability and to reduce the Miller effect. The source inductor L_S is used for simultaneous input and noise matching, while inductors L_1 and L_2 and capacitor $C_{\rm out}$ are used for output matching.

Fig. 6 presents a flowchart of the design procedures for finding the size and bias of the transistor. First, the current density J_C [or gate overdrive voltage ($V_{\rm GS}$-V_T)] and current

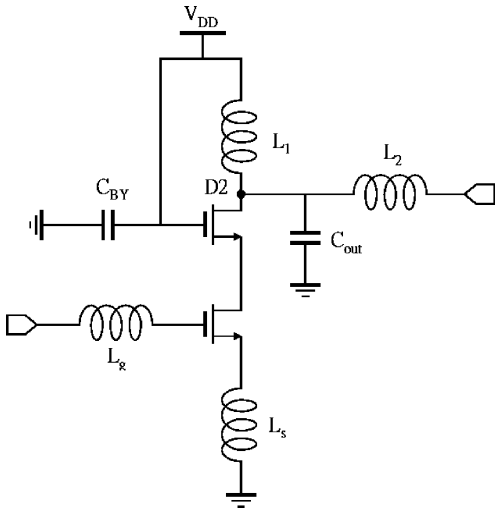

Fig. 5. Complete schematic of the LNA.

gain cutoff frequency f_T of the transistor are set to the values corresponding to the minimum $F_{\min}$ of the test device. As shown in Fig. 7, J_C and f_T corresponding to the minimum $F_{\min}$ (1.0 dB) of the test device are 49 μA/μm and 26 GHz, respectively. Second, check if S_{21} meets the specification, which is set to 10 dB. If yes, go to the next step. If no, return to the first step, i.e., sacrifice $F_{\min}$ in order to make S_{21} meet the specification. It can be shown that S_{21} of the LNA is given by

$$S_{21} = \frac{\omega_T}{\omega_O}\sqrt{\frac{R_P}{R_S}} \tag{22}$$

where $\omega_O = 1/\sqrt{(L_g + L_S)C_{gs}}$ is the resonant frequency of the input/output matching networks and R_P is the resistance seen at point D2 at the resonant frequency. Since R_P is not known *a priori*, a conservative and worse case value of 50 Ω is chosen for the initial estimate of S_{21}. Third, for noise matching, R_{opt} is set to 50 Ω and, from (16), the required g_m can be decided. Fourth, the required W is decided by g_m and f_T. Fifth, the driving current I_C is decided by J_C and W. Finally, if the power consumption and linearity meet the specification, then the finding of the size and bias of the transistor is completed. Otherwise, go back to step 1 and use lower current density.

After deciding the size and bias of the transistor, the other components of the LNA can be determined as follows. The input resistance R_{in} of the LNA is known to be $R_{\text{in}} = \omega_T L_S$ [19] and, thus, L_S is determined when R_{in} is set to 50 Ω. L_g is calculated by setting (17), i.e., X_{opt} to zero. L_1, L_2, and capacitor C_{out} are determined by the standard matching technique. The calculated result shows that the best condition is $W = 110$ μm and $I_C = 5$ mA for $R_{\text{opt}} = 50\ \Omega$. The measured result shows that $R_{\text{opt}} = 44\ \Omega$ is achieved when $W = 110$ μm and $I_C = 5$ mA, which not only agree with the calculated results, but also experimentally demonstrate that R_{opt} close to 50 Ω can be obtained by using small device and small current and, therefore, the power constraint method [19], [22] is not always necessary.

III. Circuit Implementation and Measurement Results

The LNA under study was fabricated with a standard 0.25-μm mixed-signal/RF CMOS technology on a p-type substrate with substrate resistivity $R_{\text{sub}} \sim 20\ \Omega \cdot$ cm provided by the commercial foundry United Microelectronics Corporation (UMC), Hsinchu, Taiwan, R.O.C. The main features of the backend processes are as follows. There are five metal layers. Metal-4 (M4) and Metal-5 (M5) were used as the underpass metal layer and the top metal layer of the inductors, respectively. The top metal thickness and underpass metal thickness were 2 and 0.6 μm, respectively. The oxide thickness between top metal and underpass metal, and the oxide thickness between underpass metal and silicon substrate were 1 and 6.2 μm, respectively. No patterned ground shield was implemented below the inductors. Normal substrate thickness was approximately 750 μm. Low-k dielectric material was used

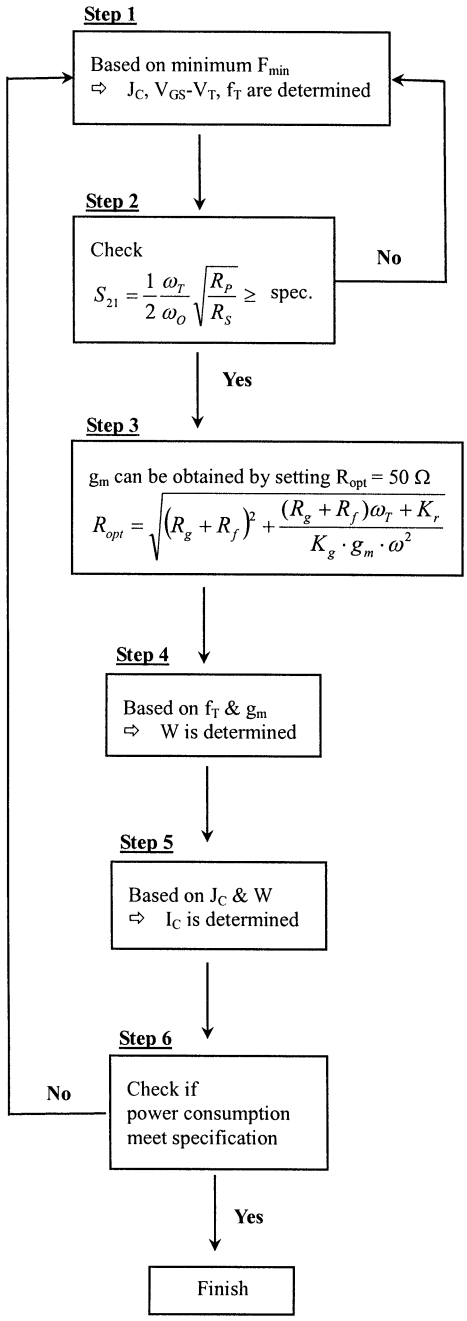

Fig. 6. Flowchart of the design procedures for finding optimized transistor's size and bias.

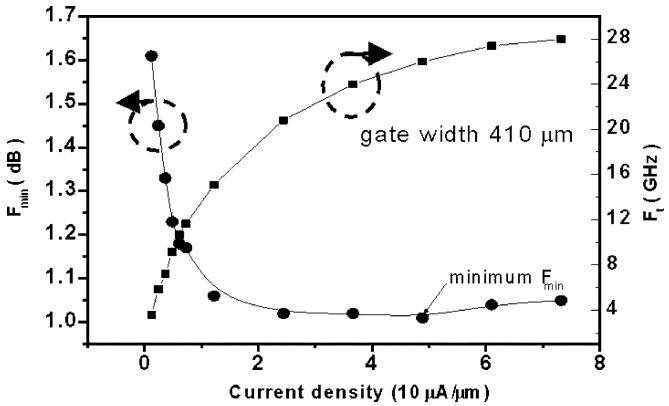

Fig. 7. $F_{\min}$ and f_T versus current density J_C of a test device with gatewidth 410 μm.

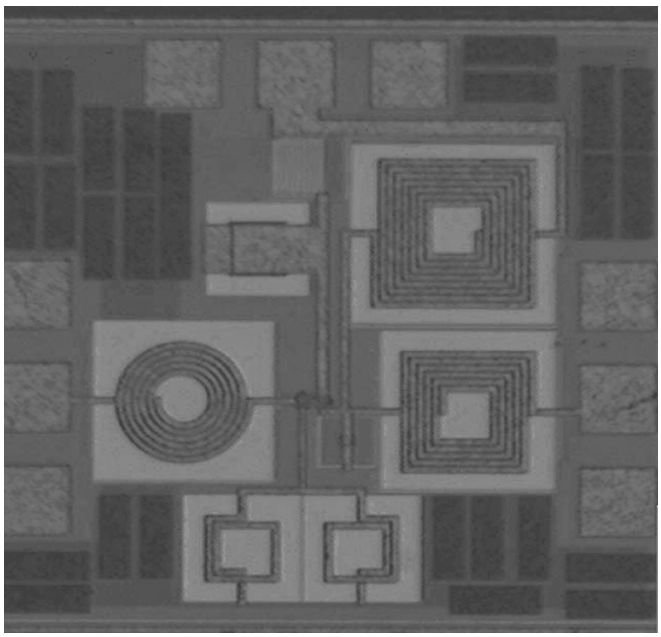

Fig. 8. Die photograph of the LNA.

as the inter-metal-dielectric (IMD) layers for high-performance mixed-signal/RF-CMOS applications.

Fig. 8 presents a die photograph of the LNA. This circuit, which occupies an area of 500×795 μm^2, is operated with $V_{DD} = 2$ V. The substrate of the LNA was thinned down to approximately 20 μm for the purpose of studying the effect of silicon substrate thickness on the NF performance of the LNA. Fig. 9 shows the detailed process flow to thin down the substrate of the LNA. First, stick the front side (the side with the LNA) of the chip (5 mm $\times$ 5 mm) to the glass substrate with wax. Second, polish the back of the chip mechanically to the target thickness, i.e., 20 μm, by holding the glass substrate facing down onto a rotating pad with a diamond sand paper. Third, apply photosensitive epoxy to the back of the chips and stick another glass substrate to it, followed by a 3-s UV exposure for epoxy curing and activation. Viscosity is enhanced as the exposure time increases. Fourth, soften the wax by heating so that the glass substrate on the front side of the chip can be removed. Finally, clean the chip by acetone. The thickness of the overall die plus photosensitive epoxy is approximately 40 μm. Since a glass substrate has

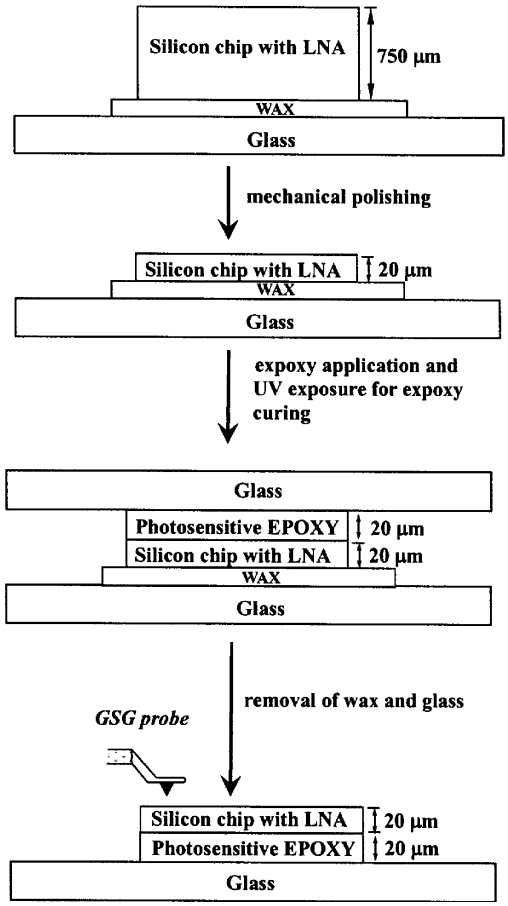

Fig. 9. Detailed process flows of silicon substrate thinning.

been attached to the backside of the chip, it is easy to handle the chip. For the current small 5 mm $\times$ 5 mm chip, it is found that the yield is 100% in the laboratory. It is not clear to us that if this process will be a low-cost and high-yield process in the industry. However, as technology advances, we believe that the yield of this process should also be high even for large diameter wafers used in the industry.

The noise and scattering parameters were measured on wafer using an automated NP5 measurement system from ATN Microwave Inc., Palo Alto, CA. The measured characteristics of NFs versus frequency for the LNA on a normal substrate with different power consumptions are shown in Fig. 10(a). Minimum NFs of 2.7, 2.9. and 3.3 dB were obtained at the frequency 5.2 GHz with power consumptions of 12, 7.6, and 3.6 mW, respectively. The frequency (5.2 GHz) where minimum NF happens is denoted by ω_{On}. Fig. 10(b) compares the measured characteristics of NFs versus frequency for the LNA on both normal and thin substrates with power consumption of 10 mW. Minimum NFs of 2.17 and 3.0 dB are obtained around the frequency $\omega_{On} = 5.2$ GHz for the LNAs on the thin and normal substrates, respectively. Our results unequivocally demonstrate that low NFs and low power consumptions can be achieved simultaneously with on-chip input and output matching networks in CMOS technology at 5-GHz band. In fact, the difference between minimum and 50-Ω NF is only 0.2 dB at 5.2 GHz, indicating an approximation to optimum noise matching due to the design of $R_{\rm opt}$ to the desired value of 50 Ω ($= Z_s$). From our

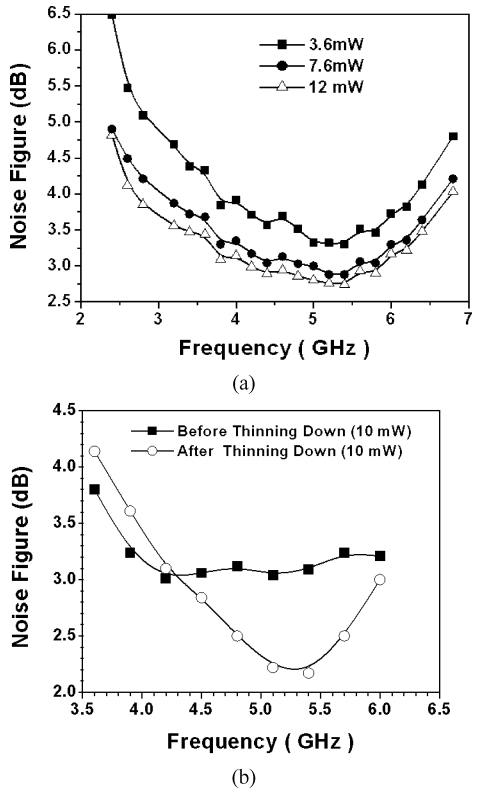

Fig. 10. (a) Measured characteristics of NFs versus frequency for the LNA on a normal substrate (750 μm) with different power consumptions. (b) Measured characteristics of NFs versus frequency for the LNA on both normal (750 μm) and thin (20 μm) substrates with 10-mW power consumption.

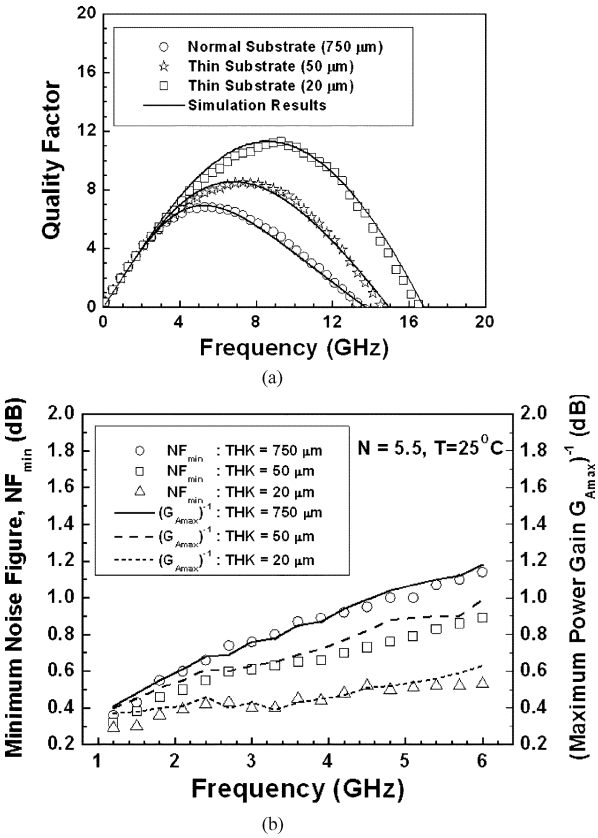

Fig. 11. (a) Measured and simulated quality factors versus frequency characteristics. (b) Measured minimum NFs and the inverse of maximum available power gains versus frequency characteristics of a 5.5-turn testing inductor fabricated at the same time with the LNAs on both normal (750 μm) and thin (50 and 20 μm) substrates.

experimental data, we conclude that setting $R_{\rm opt} = 50\,\Omega$ does not necessarily require large $C_{\rm gs}$ (device size) or large current, at least for the CMOS process we used.

Fig. 11(a) shows the measured and simulated quality factors versus frequency characteristics of a 5.5-turn testing inductor fabricated at the same time with the LNAs on both normal (750 μm) and thin substrates (50 and 20 μm). The track width and gap between tracks of this inductor were 8 and 2 μm, respectively. The inner dimension inside the inner coil was 60 μm$\times$ 60 μm. As can be seen, the measured maximum quality factors ($Q_{\rm max}$) were 6.9, 8.5, and 11.3, respectively, for silicon substrate thicknesses of 750, 50, and 20 μm. The measured self-resonance frequencies ($f_{\rm SR}$) were 13.5, 14.7, and 16.7, respectively, for silicon substrate thicknesses of 750, 50, and 20 μm, i.e., 63.8% (from 6.9 to 11.3) and 23.7% (from 13.5 to 16.7) performance improvements of $Q_{\rm max}$ and $f_{\rm SR}$, respectively, are achieved if the silicon substrate is thinned down from 750 to 20 μm. This means the silicon substrate thinning is effective in improving both the quality factor and resonant frequency of the inductors due to the reduction of silicon substrate loss. It is interesting to note that silicon substrate thinning can largely improve both the $Q_{\rm max}$ and $f_{\rm SR}$ of an inductor, while metal or polysilicon pattern-ground-shield (PGS) can only improve $Q_{\rm max}$, but deteriorate $f_{\rm SR}$ of an inductor [26]. Taking the inductor with the best performance (i.e., with polysilicon PGS on a silicon substrate with resistivity $R_{\rm sub} \sim 11\,\Omega\cdot$cm) in [26], for example, the improvement in $Q_{\rm max}$ is only 33% (from 5.08 to 6.76), but the deterioration in $f_{\rm SR}$ is up to -47.1% (from 6.8 to 3.6).

The measured $\rm NF_{min}$ of a 5.5-turn testing gate inductor was compared to the calculated $10\log(1/G_{A\,\rm max})$ obtained from the measured S-parameters at various silicon substrate thicknesses (750, 50, and 20 μm), as shown in Fig. 11(b). As can be seen, the measured $\rm NF_{min}$ conformed well to the calculated $10\log(1/G_{A\,\rm max})$ [24]. In addition, the measured $\rm NF_{min}$ at 5.4 GHz was 1.07, 0.83, and 0.52 dB, respectively, for silicon substrate thicknesses of 750, 50, and 20 μm. This means the silicon substrate thinning is effective in improving $\rm NF_{min}$ of the inductors due to the reduction of silicon substrate loss. Besides, the measured S-parameters of a testing MOSFET with gate length of 0.25 μm fabricated at the same time with the LNAs on both normal (750 μm) and thin substrates (50 and 20 μm) are nearly the same, i.e., silicon substrate thinning shows no effects on the performance of MOSFETs. Based on the above results, the reason why silicon substrate thinning can improve the NF of an LNA can be explained as follows. Since the thickness of the thin substrate ($\sim$ 20 μm) is much smaller than the diameter of the inductor (on the order of 100 μm) [26], [27] and much larger than the gate length of the MOSFETs (0.25 μm), the reduction of the NF of an LNA with a thin substrate should be mainly due to the reduction of substrate loss of the inductors in the LNA. The measurement of the NFs on the 5.5-turn testing inductor shows a 0.55-dB reduction of NF

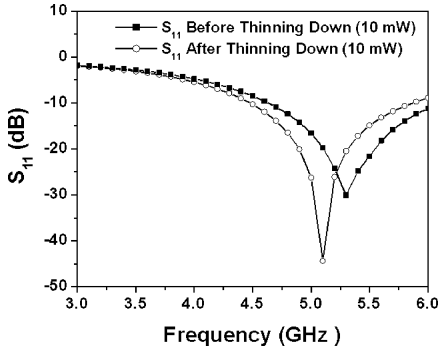

Fig. 12. Measured characteristics of input return loss (S_{11}) versus frequency for the LNA on both normal (750 μm and thin (20 μm) substrates with 10-mW power consumption.

(from 1.07 to 0.52 dB) after substrate thinning to 20 μm [see Fig. 11(b)]. This result demonstrates the 0.83-dB reduction of the NF of the LNA (from 3.0 to 2.17 dB) is reasonable.

Fig. 12 shows the measured characteristics of S_{11} versus frequency for the LNAs on both normal and thin substrates with power consumption of 10 mW. Minimum return losses of -45 dB at ω_O of 5.1 GHz (thin substrate) and -30 dB at ω_O of 5.3 GHz (normal substrate) were achieved as a result of the right choice of L_S. The in-band (5.15 $\sim$ 5.35 GHz) return losses were below -18 dB and -22 dB for normal and thin substrates, respectively, indicating a very good match even over the band. Note that ω_O is very close to ω_{On}. This is important for simultaneous input matching and noise matching. In fact, it can be shown from (4) that the frequency ω_{On} is given by

$$\omega_{On} = \omega_O\sqrt{K_C}\sqrt{1-\frac{\omega_O^2 C_{\rm gs}^2\left(R_S+R_g+R_{\ell g}+R_{fg}+R_f\right)^2}{2K_C}} \approx \omega_O\sqrt{K_C}\sqrt{1-\frac{1}{2Q_S^2K_C}}. \quad (23)$$

If $Q_S^2 \gg 1$ and K_C is not far from unity, (23) reduces to

$$\left(\frac{\omega_{On}}{\omega_O}\right)^2 = K_C. \quad (24)$$

Take, for example, the experimental values of the LNA on a normal substrate at power consumption of 10 mW, i.e., $\omega_{On} = 5.2$ GHz and $\omega_O = 5.3$ GHz, as shown in Figs. 10(b) and 12, respectively. A value of $K_c = 0.96$ was determined, which is close to 1. The fact that K_c approximates 1 explains why ω_O and ω_{On} are so close to each other. Thus, K_c can be interpreted physically as a measure of the separation between ω_O and ω_{On}. In other words, if a CMOS process does not result in a K_c close to 1, it is almost hopeless for circuit designers to design a circuit with simultaneous input impedance matching and noise matching over the narrow band of interest.

The measured transducer gain (S_{21}) for the LNA on a normal substrate with different power consumptions is shown in Fig. 13(a). The bandpass nature of this amplifier is evident from the plot. Under the bias condition of 12 mW, the gain has

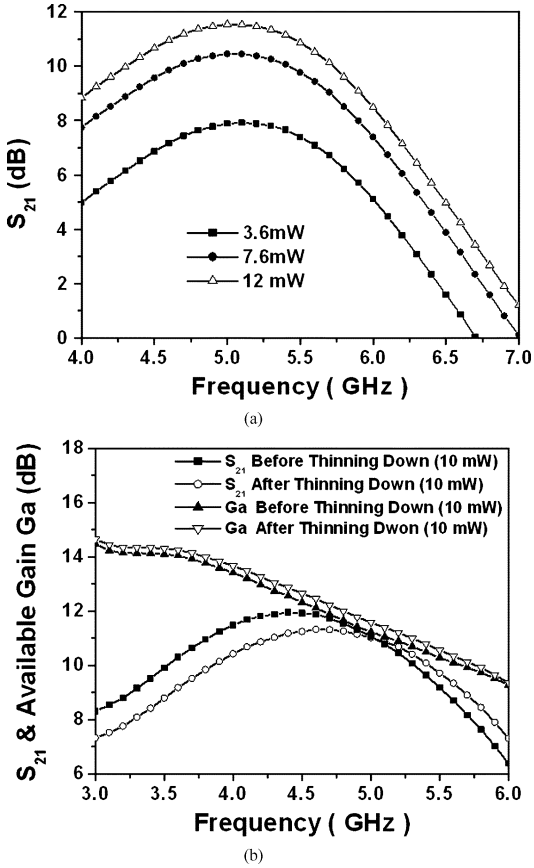

Fig. 13. Measured transducer gain (S_{21}) versus frequency of the LNA: (a) on a normal substrate (750 μm) with different power consumptions and (b) on both normal (750 μm) and thin (20 μm) substrates with 10-mW power consumption.

a peak value of 11.5 dB. For a direction conversion receiver, the load resistance is not necessarily 50 Ω and a higher gain can be expected. For lower power consumptions, the characteristics are similar, but with lower gains of 10.4 dB at 7.6 mW and 8 dB at 3.6 mW. One figure-of-merit is the ratio of gain to dc power consumption [2]. The values of gain to dc power consumption attained by this CMOS LNA were 0.95, 1.4, and 2.2 dB/mW at three different power consumptions of 12, 7.6 and 3.6 mW, respectively. The measured S_{21} and available gain for the LNA on both normal and thin substrates with power consumption of 10 mW are shown in Fig. 13(b). The available gain has peak values of 10.9 and 11.2 dB for normal and thin substrates, respectively. The values of gain to dc power consumption attained are 1.12 (thin substrate) and 1.09 (normal substrate) dB/mW. As can be seen clearly in Table I, the obtained ratios of gain to dc power consumption are comparable to the other state-of-the-art C-band LNAs shown in Table I.

Microwave power performances were measured by a load–pull ATN system with automatic tuners. The measured $P_{1\,\rm dB}$ and input IP3 data for the LNA on a thin (20 μm) substrate under power consumption of 10 mW are shown in Fig. 14. As can be seen, an input $P_{1\,\rm dB}$ of -8.3 dBm and an input IP3 of 0.3 dBm were obtained. Other measured $P_{1\,\rm dB}$ and input IP3 data are summarized in Table I. A summary of the measured amplifier characteristics at different bias conditions is also included in Table I.

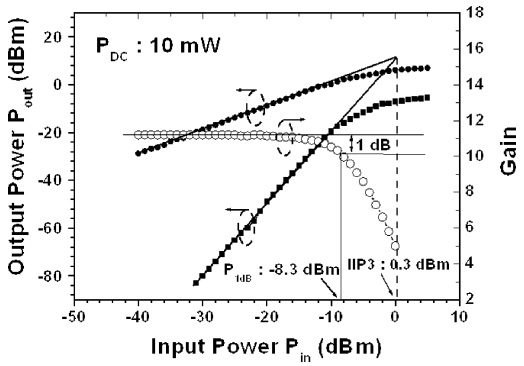

Fig. 14. Measured input $P_{1\ \mathrm{dB}}$ and input IP3 for the LNA on a thin substrate (20 μm) with 10-mW power consumption.

IV. Conclusions

A method of designing R_{opt} to a desired value by the selection of transistor device size and transconductance or bias is proposed. By setting $R_{\mathrm{opt}} \sim 50\ \Omega$, NFs of 2.17 and 3.0 dB, and input return losses of -45 and -30 dB at the 5-GHz band from a monolithic CMOS LNA with 10-mW dissipation on both thin ($\sim$ 20 μm) and normal (750 μm) substrates are demonstrated with a standard 0.25-μm CMOS process provided by a commercial foundry. The fact that K_c is close to 1 in the CMOS process we used can achieve low NF and low input return loss simultaneously in the narrow band of interest. In addition, substrate thinning is effective in reducing the NF. The result also unequivocally demonstrates that low NFs and low power consumption can be achieved simultaneously with on-chip input and output matching networks in CMOS technology at the 5-GHz band. From both a performance and a cost perspective, these experimental results show that CMOS is very competitive with silicon bipolar and GaAs technologies.

Appendix
Derivation of the NF for an FET With Gate and Source Inductors

A noise analysis of the circuit shown in Fig. 1(b) quantifies the effects of the gate and source inductors. An equivalent circuit for noise calculation is depicted in Fig. 1(b). By definition the NF, F can be expressed in the form

$$F = \frac{\overline{i_{n,\mathrm{out}}^2}}{\overline{i_{s,o}^2}} = 1 + \frac{\overline{|i_{rgo} + i_{\mathrm{lg}\,o} + i_{go} + t_{rfo} + i_{lfo} + i_{do}|^2}}{\overline{i_{s,o}^2}} \tag{25}$$

where $i_{n,\mathrm{out}}$ stands for the total noise current in the short-circuited drain–source path originated from the noise current components i_{rgo}, $i_{\ell go}$, i_{go}, i_{rfo}, $i_{\ell fo}$, i_{do}, and i_{so} produced by the noise generators from transistor gate resistance noise e_{rg}, series resistance of gate inductor $e_{\ell g}$, induced gate noise current i_g, transistor source resistance noise e_{rf}, series resistance of source inductor $e_{\ell f}$, drain noise current i_d, and signal source resistance noise e_s. The noise generators representing the extrinsic thermal sources are given by their mean square values $\overline{|e_{rg}^2|} = 4kTR_g\Delta f$, $\overline{|e_{\ell g}^2|} = 4kTR_{\ell g}\Delta f$, $\overline{|e_{rf}^2|} = 4kTR_f\Delta f$, $\overline{|e_{\ell f}^2|} = 4kTR_{\ell f}\Delta f$, and $\overline{|e_s^2|} = 4kTR_S\Delta f$. A careful analysis yields the following equations:

$$i_{rgo} = e_{rg}\frac{\frac{g_m}{j\omega C_{\mathrm{gs}}}}{\frac{1}{j\omega C_{\mathrm{gs}}} + \frac{g_m L_s}{C_{\mathrm{gs}}} + Z_t} \tag{26}$$

$$i_{\ell go} = e_{\ell g}\frac{\frac{g_m}{j\omega C_{\mathrm{gs}}}}{\frac{1}{j\omega C_{\mathrm{gs}}} + \frac{g_m L_s}{C_{\mathrm{gs}}} + Z_t} \tag{27}$$

$$i_{rfo} = e_{rf}\frac{\frac{g_m}{j\omega C_{\mathrm{gs}}}}{\frac{1}{j\omega C_{\mathrm{gs}}} + \frac{g_m L_s}{C_{\mathrm{gs}}} + Z_t} \tag{28}$$

$$i_{\ell fo} = e_{\ell f}\frac{\frac{g_m}{j\omega C_{\mathrm{gs}}}}{\frac{1}{j\omega C_{\mathrm{gs}}} + \frac{g_m L_s}{C_{\mathrm{gs}}} + Z_t} \tag{29}$$

$$i_{so} = e_s\frac{\frac{g_m}{j\omega C_{\mathrm{gs}}}}{\frac{1}{j\omega C_{\mathrm{gs}}} + \frac{g_m L_s}{C_{\mathrm{gs}}} + Z_t} \tag{30}$$

$$i_{go} = i_g\frac{\frac{g_m}{j\omega C_{\mathrm{gs}}}Z_t}{\frac{1}{j\omega C_{\mathrm{gs}}} + \frac{g_m L_s}{C_{\mathrm{gs}}} + Z_t} \tag{31}$$

$$i_{do} = i_d\frac{Z_t + \frac{1}{j\omega C_{\mathrm{gs}}}}{\frac{1}{j\omega C_{\mathrm{gs}}} + \frac{g_m L_s}{C_{\mathrm{gs}}} + Z_t}. \tag{32}$$

Inserting (26)–(32) into (25) yields

$$F = 1 + \frac{R_g + R_{\ell g} + R_{\ell f} + R_f}{R_S} + \frac{1}{4kTR_S\Delta f}\overline{\left|Z_t i_g + \frac{1 + j\omega C_{\mathrm{gs}} Z_t}{g_m} i_d\right|^2}. \tag{33}$$

Substituting $Z_t = Z_S + R_g + R_f + R_{\ell g} + R_{\ell f} + j\omega(L_g + L_S)$ into (33), we get (34), shown at the bottom of this page. By

$$F = 1 + \frac{R_g + R_{\ell g} + R_{\ell f} + R_f}{R_S} + \frac{1}{4kTR_S\Delta f}\frac{\overline{\left|i_g + \frac{j\omega C_{\mathrm{gs}}}{g_m} i_d\right|^2}}{\left|Z_S + R_g + R_{\ell g} + R_{\ell f} + R_f + j\omega(L_g + L_S) + \frac{i_d}{g_m\left(i_g + \frac{j\omega C_{\mathrm{gs}}}{g_m} i_d\right)}\right|^2} \tag{34}$$

analogy with the results derived by Pucel *et al.*, (34) can be put in the form of (4) if G_n, R_u, and Z_C are defined as follows:

$$G_n = \left| \frac{j\omega C_{\rm gs}}{g_m}\sqrt{g_m P} - jC\sqrt{R\frac{\omega^2 C_{\rm gs}^2}{g_m}} \right|^2 + \left(1-C^2\right) R\frac{\omega^2 C_{\rm gs}^2}{g_m} \tag{35}$$

$$R_u = R_g + R_{\ell g} + R_{\ell f} + R_f + \frac{P}{g_m}\frac{\left(1-C^2\right)}{G_n} R\frac{\omega^2 C_{\rm gs}^2}{g_m} \tag{36}$$

$$Z_C = R_g + R_{\ell g} + R_{\ell f} + R_f + j\omega\left(L_g + L_S\right) + \frac{1}{G_n}\left(\frac{-Pj\omega C_{\rm gs}}{g_m} + \frac{jC\sqrt{PR\omega^2 C_{\rm gs}^2}}{g_m}\right) \tag{37}$$

and, thus, the NF of an FET with gate and source inductors are derived.

ACKNOWLEDGMENT

The authors gratefully acknowledge Dr. G. W. Huang, W. Wang,, Nano-Device Laboratory (NDL), Hsinchu, Taiwan, R.O.C., for high-frequency measurements and J. J. Yu, UMC, Hsinchu, Taiwan, R.O.C., forhelpful discussions.

REFERENCES

[1] K. W. Kobayashi, A. K. Oki, L. T. Tran, and D. C. Streit, "Ultra low dc power GaAs HBT S- and C-band low noise amplifiers for portable wireless applications," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 12, pp. 3055–3061, Dec. 1995.

[2] H. Morkner, M. Frank, and D. Millicker, "A high performance 1.5 dB low noise GaAs PHEMT MMIC amplifier for low cost 1.5-8 GHz commercial applications," in *IEEE Microwave Millimeter-Wave Monolithic Circuits Symp. Dig.*, 1993, pp. 13–16.

[3] Y. Tsukahara, S. Chaki, Y. Sakaki, K. Nakahara, N. Andoh, H. Matsubayasi, N. Tanino, and O. Ishihara, "A C-band 4 stage low noise miniaturized amplifier using lumped elements," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1995, pp. 1125–1128.

[4] U. Lott, "Low dc power monolithic low noise amplifier for wireless applications at 5 GHz," in *IEEE Microwave Millimeter-Wave Monolithic Circuits Symp. Dig.*, 1998, pp. 81–84.

[5] S. Yoo, D. Heo, J. Laskar, and S. S. Taylor, "A C-band low power high dynamic range GaAs MESFET low noise amplifier," in *IEEE Microwave Millimeter-Wave Monolithic Circuits Symp. Dig.*, 1999, pp. 81–84.

[6] J. J. Kucera and U. Lott, "A 1.8 dB noise figure low dc power MMIC LNA for C-band," in *IEEE GaAs IC Symp. Dig.*, 1998, pp. 221–224.

[7] M. Soyuer, J.-O. Plouchart, H. Ainspan, and J. Burghartz, "A 5.8 GHz 1-V low noise amplifier in SiGe bipolar technology," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, 1997, pp. 19–22.

[8] H. Samavati, H. R. Rategh, and T. Lee, "A 5-GHz CMOS wireless LAN receiver front end," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 765–772, May 2000.

[9] E. Westerwick, "5-GHz band CMOS low noise amplifier with a 2.5 dB noise figure," in *IEEE Int. VLSI Technology, Systems, Application Symp. Dig.*, 2001, pp. 224–227.

[10] P. Leroux and M. Steyaert, "High-performance 5.2-GHz LNA with on-chip inductor to provide ESD protection," *Electron. Lett.*, vol. 37, pp. 467–469, Mar. 2001.

[11] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory, design, and application," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 288–301, Jan. 2002.

[12] D. J. Cassan and J. R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 427–435, Mar. 2003.

[13] C.-Y. Cha and S.-G. Lee, "A 5.2-GHz LNA in 0.35-mm CMOS utilizing inter-stage series resonance and optimizing the substrate resistance," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 669–672, Apr. 2003.

[14] T. P. Liu and E. Westerwick, "5-GHz CMOS radio transceiver front-end chipset," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1927–1933, Dec. 2000.

[15] B. A. Floyd, J. Mehta, C. Gamero, and K. O. Kenneth, "A 900-MHz, 0.8-μm CMOS low noise amplifier with 1.2-dB noise figure," in *Proc. IEEE CICC*, 1999, pp. 661–664.

[16] H. W. Chiu and S. S. Lu, "A 2.17 dB NF, 5 GHz band monolithic CMOS LNA with 10 mW DC power consumption," in *IEEE VLSI Symp. Dig.*, 2002, pp. 226–229.

[17] M. Aikawa, T. Oohira, T. Tokumitsu, T. Hiroda, and M. Muraguchi, *Monolithic Microwave Integrated Circuits* (in Japanese). Tokyo, Japan: EIC, 1997, p. 90.

[18] Y. Konishi and K. Honjo, *Microwave Semiconductor Circuits* (in Japanese). Tokyo, Japan: Nikan Industrial News Publisher, 1993, p. 114.

[19] D. K. Shaeffer and T. H. Lee, "A 1.5 V, 1.5 GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[20] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and noise properties of Gallium arsenide field effect transistors," in *Advances in Electronics and Electron Physics*, L. Morton, Ed. New York: Academic, 1975, vol. 38, pp. 195–265.

[21] A. V. D. Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986, p. 90.

[22] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998, pp. 272–303.

[23] A. Anastassiou and M. J. O. Strutt, "Effect of source lead inductance on the noise figure of a GaAs FET," *Proc. IEEE*, vol. 62, no. 3, pp. 406–408, Mar. 1974.

[24] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998, p. 47.

[25] H. Fukui, "Design of microwave GaAs MESFET's for broadband low noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 27, no. 7, pp. 643–650, Jul. 1979.

[26] C. P. Yue and S. S. Wong, "On chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, May 1998.

[27] D. Melendy, P. Francis, C. Pichler, K. Hwang, G. Srinivasan, and A. Weisshaar, "Wide-band compact modeling of spiral inductors in RF-IC's," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2002, pp. 717–720.

Hung-Wei Chiu was born in Taipei, Taiwan, R.O.C., in 1976. He received the B.S. degree from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1998, and the M.S. and Ph.D. degrees from National Taiwan University, Taipei, Taiwan, R.O.C., in 2000 and 2003, respectively, all in electrical engineering.

In 2004, he joined the Taiwan Semiconductor Manufacturing Company, Taiwan, R.O.C., as a Designer with the Mixed-Mode and RF Library Division. Since then, he has been involved in the area of automation of mixed-mode and RF circuit design.

Shey-Shi Lu (S'89–M'91–SM'99) was born in Taipei, Taiwan, R.O.C., on October 12, 1962. He received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1985, the M.S. degree from Cornell University, Ithaca, NY, in 1988, and the Ph.D. degree from the University of Minnesota at Minneapolis–St. Paul, in 1991, all in electrical engineering. His M.S. thesis concerned the planar doped barrier hot electron transistor. His doctoral dissertation concerned the uniaxial stress effect on the AlGaAs/GaAs quantum well/barrier structures.

In August 1991, he joined the Department of Electrical Engineering, National Taiwan University, where he is currently a Professor. His current research interests are in the areas of radio-frequency integrated circuits (RFICs)/monolithic microwave integrated circuits (MMICs), and micromachined RF components.

Yo-Sheng Lin (M'02) was born in Puli, Taiwan, R.O.C., on October 10, 1969. He received the Ph.D. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 1997. His Ph.D. degree concerned the fabrication and study of GaInP/ InGaAs/GaAs doped-channel FETs and their applications on monolithic microwave integrated circuits (MMICs).

In 1997, he joined the Taiwan Semiconductor Manufacturing Company (TSMC), as a Principle Engineer for 0.35/0.32 dynamic random access memory (DRAM) and 0.25 embedded DRAM technology developments with the Integration Department of Fab-IV. Since 2000, he has been responsible for 0.18/0.15/0.13-μm CMOS low-power device technology development with the Department of Device Technology and Modeling, Research and Development. In 2001, he became a Technical Manager. In August 2001, he joined the Department of Electrical Engineering, National Chi-Nan University, Puli, Taiwan, R.O.C., where he is currently an Associate Professor. His current research interests are in the areas of characterization and modeling of RF active and passive devices, and radio-frequency integrated circuits (RFICs)/monolithic microwave integrated circuits (MMICs).