行政院國家科學委員會專題研究計畫　成果報告

無線通訊低密度同位元檢查碼效能評估與架構設計

計畫類別：個別型計畫
計畫編號：NSC92-2213-E-002-105-
執行期間：92 年 08 月 01 日至 93 年 07 月 31 日
執行單位：國立臺灣大學資訊工程學系暨研究所

計畫主持人：顧孟愷

報告類型：精簡報告

處理方式：本計畫可公開查詢

中　華　民　國 93 年 11 月 1 日

1. Project Summary

Next-generation high speed communication system requires high performance forward-error-correction (FEC) codec to provide the coding gain necessary to transmit large amount of data at a realistic signal-to-noise ratio. In this project we focus our efforts to low density parity check (LDPC) code. LDPC code and their iterative decoding algorithms were proposed by Gallager in 1962[1]. Recently LDPC codes was re-discovered and has been shown to achieve good coding gain performance that is very close to the Shannon limit[2]. Recently there are many research that is focused on the construction of the LDPC codes that possessed the best possible coding gain performance[4][5]. On the practical application side, LDPC code has been adopted as the FEC code for next generation satellite TV in the DVB-S2 standard. Due to its good coding gain performance and relatively low implementation cost compared with Turbo code, we foresee LDPC codes will be widely employed in future wireless multimedia communication systems.

The purpose of this project is to design a flexible architecture for the LDPC code that can be used in different modulation schemes, and is both power and hardware efficient. To achieve the design goal, multiple issues need to be studied. The first step is the design of a LDPC code generator matrix that provides the optimal balance between coding gain and hardware cost. A flexible simulation environment is built to evaluate and refine the quality of our LDPC code design. Multiple decoding algorithms are evaluated in this environment based on their impact to coding gain and hardware complexity. Finite word-length study is carried out for the eventual hardware implementations, and a hardware architecture design is proposed for implementation on a FPGA platform. On the system side, the LDPC encoder / decoder module is integrated with OFDM transceiver to investigate the performance gain LDPC code can provide in wireless communication. All these issues need to be considered as a whole to achieve the best overall LDPC codec design.

1.1 Code Design

Our hardware-aware code design method focus on several principles. First of all, the code size and matrix are optimized for hardware implementation. Secondly, the code parity check matrix should be regular (i.e. the weight of all rows are equal and the weight of all columns are equal) to ease the hardware implementation. All short cycles (cycle with length 4) in the Tanner graph of the code are eliminated to ensure decoding convergence.

We used three different methods to construct (3,6)-regular code without short cycles. (3,6)-regular code means that in the parity check matrix **H** each column has weight three and each row has weight six.

Method 1**:** As shown in Fig 1, the parity check matrix is divided into three layers. Layer1 is composed of six identity sub-matrices. Layer2 is composed of six identity sub-matrices with various

shifting. Layer 3 is constructed to keep the resulting matrix regular, and to ensure overlap between any pair of columns to be equal or less than one.

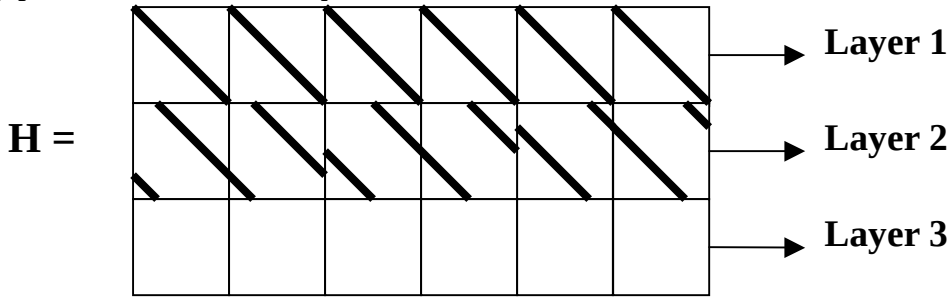

Figure 1: Parity Check Matrix of Method 1

Method 2: This method is similar to Method1 but with a slight modification. Instead of using only identity matrices in layer 1, all sub-matrices must shift right n-steps. The overlap of any pair of columns in Layer1 and Layer2 can not be greater than one. The construction of Layer3 follows the same rule as method 1.

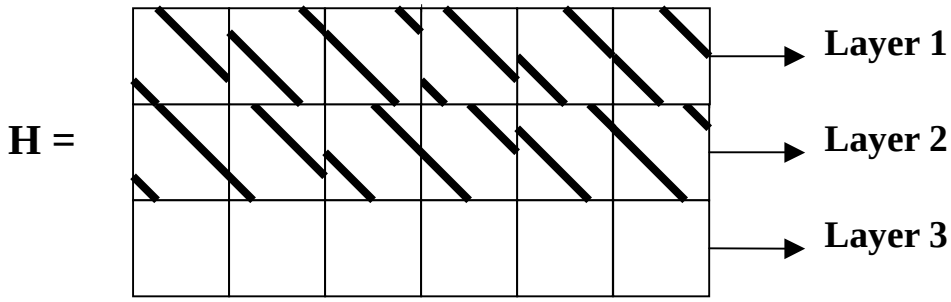

Figure 2: Parity Check Matrix of Method 2

Method 3: As shown in Figure 3**.** Layer1 is composed of six identity sub-matrices same as method 1. The six sub-matrices in Layer2 are constructed differently. Each sub-matrix is constructed by assembling six sub-sub-matrices and zero matrices. All of these sub-sub-matrices are identity matrix right shifted by n-steps. The location of these sub-sub-matrices is shown in the graph. Similar to method 2, the overlap of any pair of columns in Layer1 and Layer2 can not be greater than one. Layer 3 is constructed by putting one '1' in each column, while each row of Layer3 should has six number of "1" exactly to keep the (3,6) format, and the overlap between any pair of columns can not be greater than one.

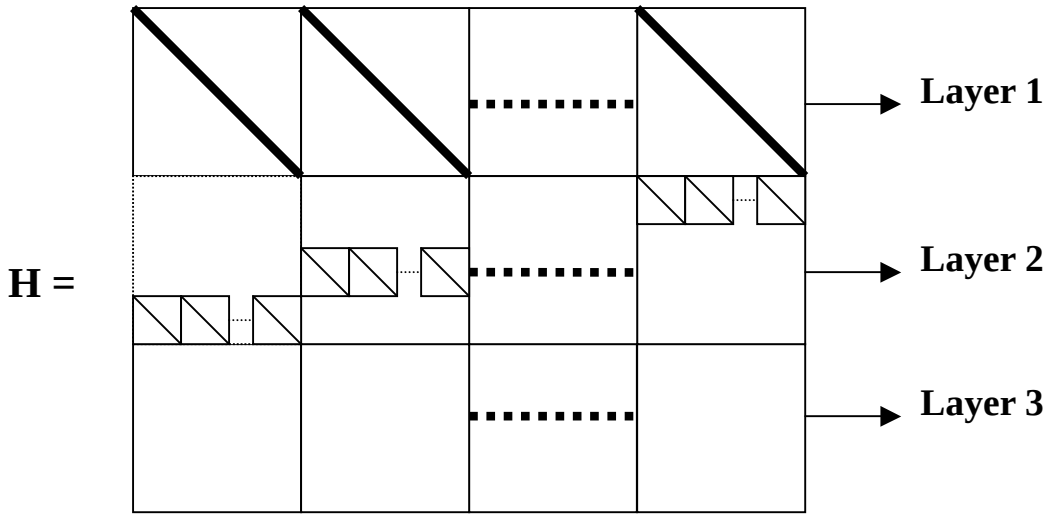

Figure 3: Parity Check Matrix of Method 3

Figure 4. shows the simulation result of the generated code. Results from code generated using Neal's method are included as comparison. The code using Neal's algorithm is generated randomly, and generally randomly generated code performs better than regular code under similar code parameters. We found that the performance of method 3 is similar to Neal's randomly generated code while the code generated by method1 and method2 are about 0.2bB worse than Neal's code at BER = 1e-3. The code generated by method 3 performs up to randomly generated code while maintaining the regular property to ease hardware implementation.

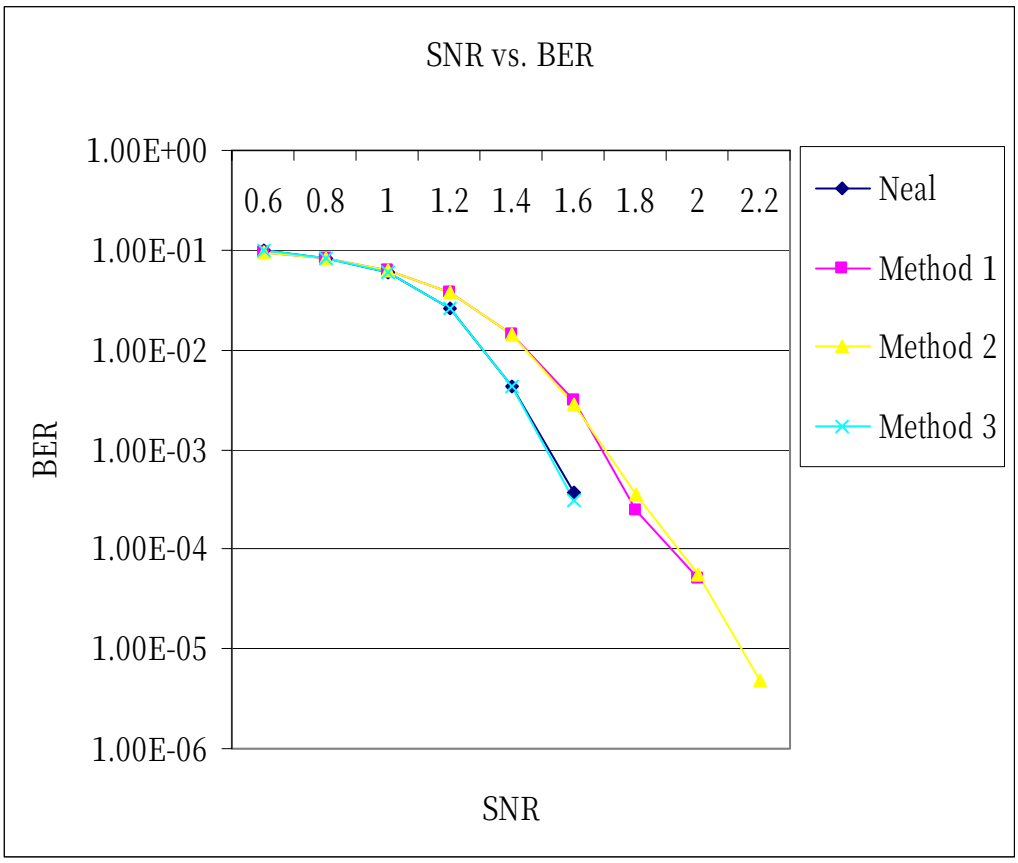

Figure 4: Performance comparison of (5040,2520) code with 40 iterations

1.2 Simulation Environment

A simulation environment for LDPC is set up such that the performance of codes with different code parameters, decoding algorithm and internal wordlengths can be evaluated easily and efficiently. The following figure shows the performance of various codes versus the published Neal code performance.

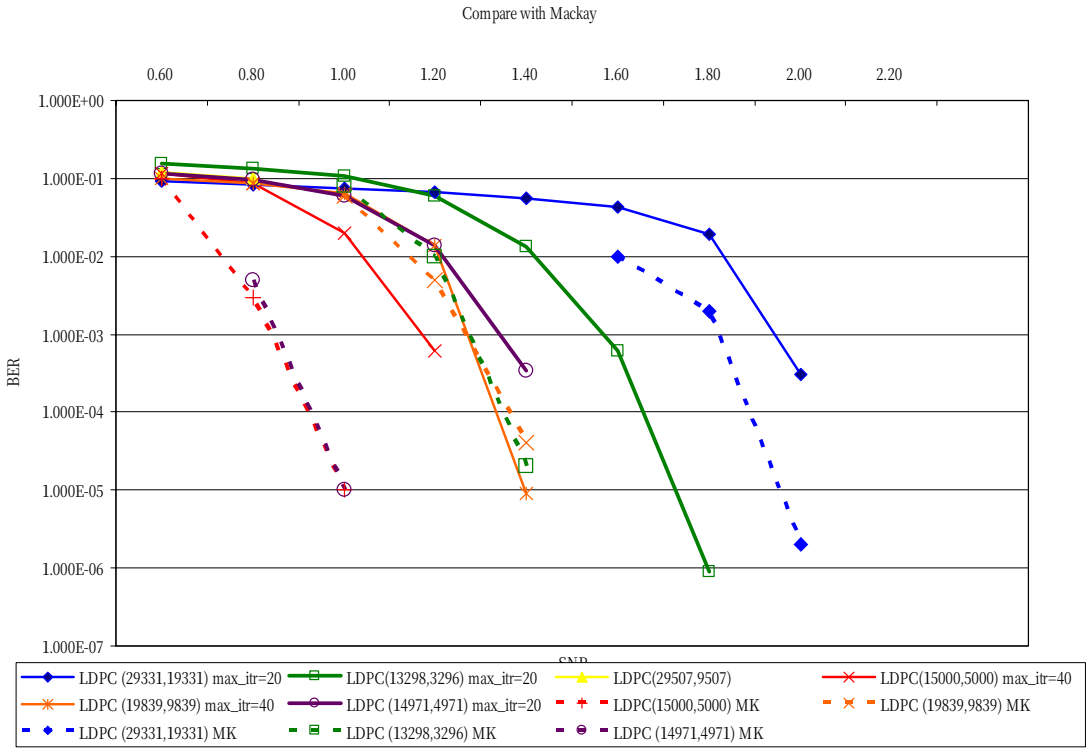

Figure 5: Some simulation results

Finite Word Length Simulation

LDPC decoder uses sum-product algorithm which finds the most likely codeword iteratively. The performance of hardware implementation depends heavily on the internal finite word length chosen in the algorithm. Floating point simulation results are used as a baseline to find the proper internal word length for our hardware implementation. First, we modified Sum-product algorithm into finite precision version. According to the simulation result (Figure 6), 16-bit worlength is necessary for each message to get the same performance of double precision. There is also error floor problem under high SNR situation. To reduce the memory requirement, eliminating error floor problem and evaluating finite precision impact, we modified the Sum-product algorithm from likelihood ratio to log-likelihood ratio and run the simulation again.

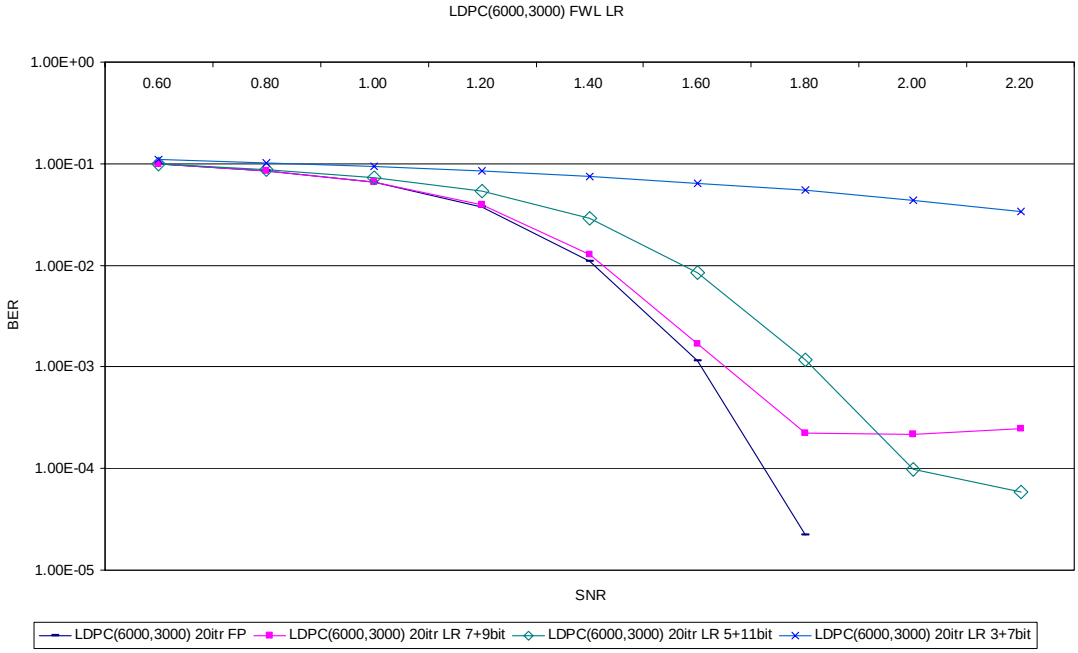

Figure 6: Finite word length simulation under likelihood ratio

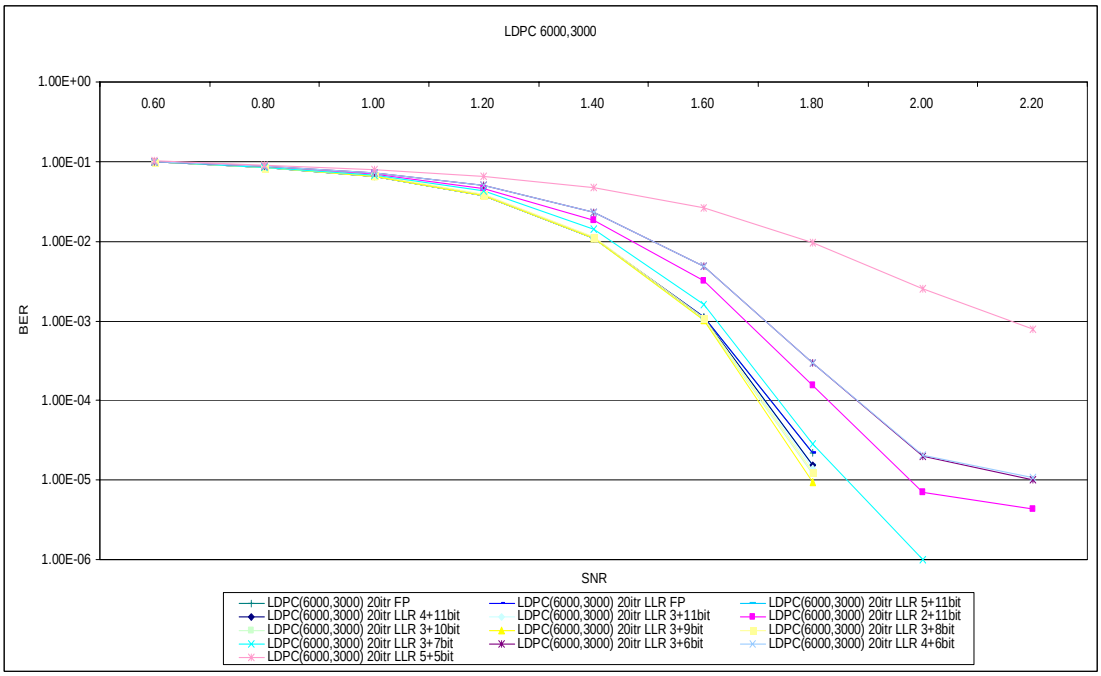

Figure 7: Finite word length simulation under log-likelihood ratio

As shown in the graph (Figure 7), after the algorithm modification, 10-bit precision can be used with no performance degradation. In order for sum-product algorithm to archive good performance under log domain, we have to implement hyperbolic tangent and inverse hyperbolic tangent functions in hardware. These two functions are complicated mathematical operations, but it can be implemented

by LUT.

1.3 Hardware Architecture Design

A general-purpose LDPC decoding architecture which can be used for regular or irregular codes is shown in the following figure. Initially, we store the likelihood ratio in initial memory and pass these ratios to check computational units. After check computational unit get these information, it will generate messages and store in LR memory. Bit computational unit reads messages from LR memory and generate new message for next message which will be stored in PR memory. This unit will also make a hard decision of current iteration result.

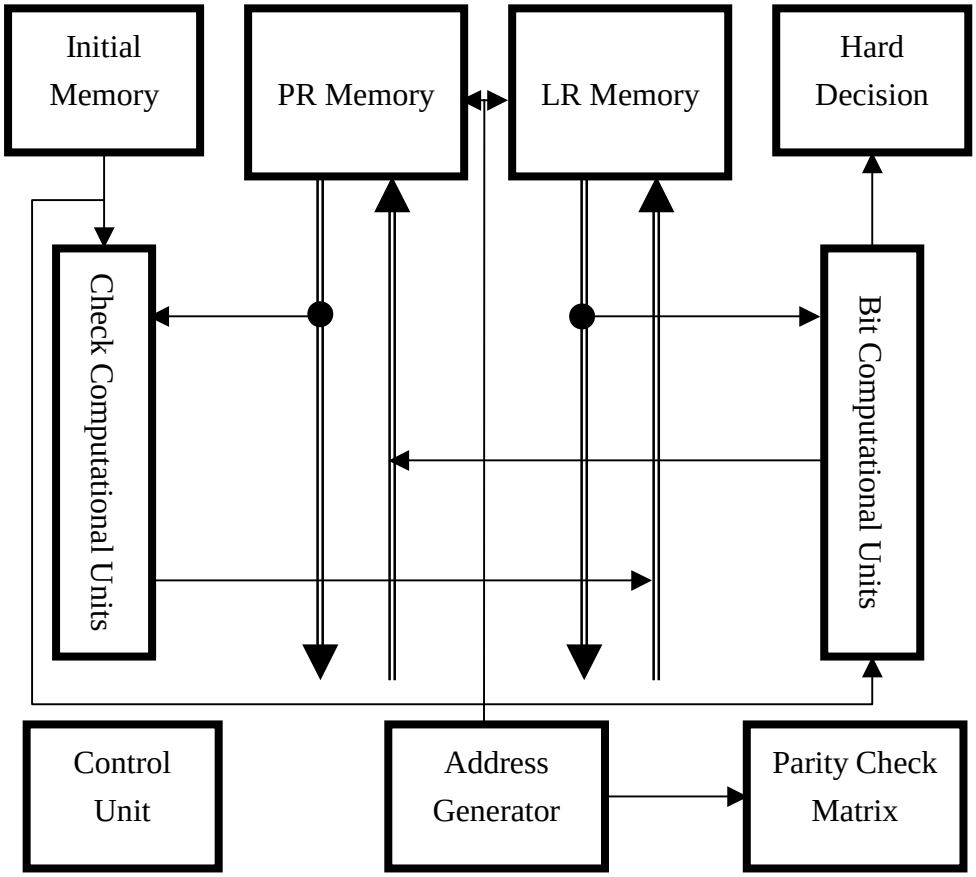

Figure 8: LDPC Decoder architecture

1.4 System Level Simulation

To evaluate the performance of LDPC code in wireless communication systems, an orthogonal frequency division multiplexing (OFDM) system model have been constructed. This model includes OFDM modulator / demodulator, LDPC encoder / decoder, and peak-to-average ratio reduction components. Multi-level modulation schemes are being investigated and will be integrated in this model. This model is highly parameterizable to facilitate the simulation and design of proper

LDPC-coded modulation scheme. In double Gray-code labeling symbol mapping scheme, Rate K/N LDPC code encode K information bits into a binary codeword of length N. The symbol mapper collects groups of coded bits, possible along with uncoded information bits and builds QAM symbols for frequency domain modulation by an inverse discrete Fourier transform. Uncoded bits are mapped to the more significant bits of a QAM symbol, which are less prone to detection errors at the receiver. While the less significant bits are more prone to detection errors thus need protection and encoded.

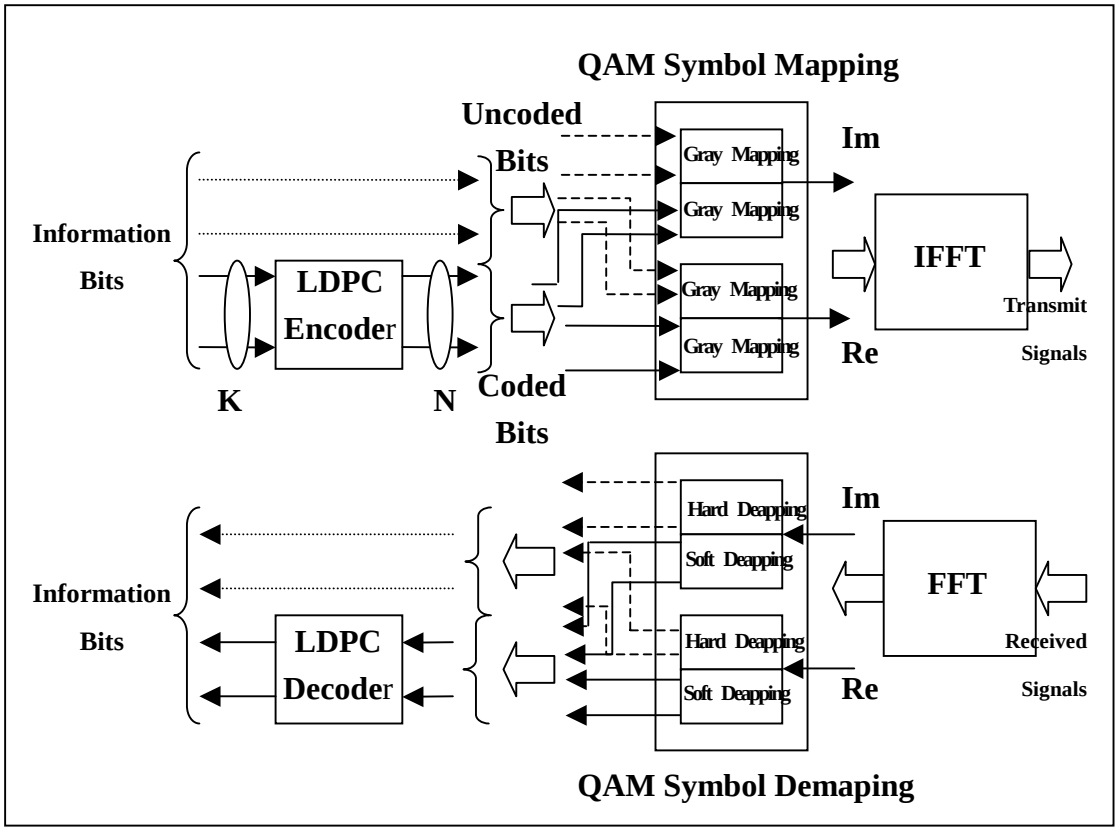

Figure 9: General structure of LDPC Coded OFDM system with multilevel modulation

2. Self Evaluation of Project

In this project, we have created a good number of tools for the design of LDPC codec. A complete simulation environment with OFDM modem is built such that the performance of LDPC code in a real system can be evaluated[10][11]. Multiple algorithms for code design are implemented, their performances compared. Finite word length study is carried out to define the hardware implementation parameters. We have also proposed an architecture design for the LDPC decoder, and started some pilot work to implement it on FPGA boards. My team of first-year graduate students has learnt a great deal about error correction systems, LDPC codes and hardware design trade-off considerations. They are getting good training to become a future communication system /

IC designer. I think we have laid the ground work for the eventual LDPC hardware implementations, and good progress has been made in the LDPC system design area. Since LDPC code has been adopted in the DVB-S2 standard, the communication IC industry will take a serious look at LDPC codes and their applications. I believe our research result will be valuable in bringing this cutting edge technology for Taiwanese IC design industry.

Reference

[1] R. G. Gallager, “Low-density parity-check codes,” IRE Trans. Inform. Theory, vol. IT-8, pp.21-28, Jan 1962

[2] R. G. Gallager, Low Density Parity Check Codes, no. 21 in Research Monograph Series, Cambridge, MA: MIT Press, 1963

[3] D.J.C. Mackay and R.M. Neal, “Near Shannon limit performance of low density parity check codes,” IEE Electronics Letters, vol. 33, no.6, pp. 457-458

[4] T.J. Richardson, M.A. Shokrollahi, and R.L. Urbanke, “Design of capacity-approaching irregular low-density parity-check codes,” IEEE Trans. Information Theory, vol.47, pp.619-637, Feb. 2001

[5] S.Chung; G.D. Forney, T.J. Richardson, and R. Urbanke, “On the design of low-density parity-check codes within 0.0045 dB of the Shannon limit,” IEEE Comm. Letters, vol.5, pp.58-60, Feb. 2001.

[6] Tong Zhang; Parhi, K.K “Joint (3,k)-regular LDPC code and decoder/encoder design” Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on] , Volume: 52 , Issue: 4 , April 2004 Pages:1065 - 1079

[7] Karkooti, M.; Cavallaro, J.R “Semi-parallel reconfigurable architectures for real-time LDPC decoding” Information Technology: Coding and Computing, 2004. Proceedings. ITCC 2004. International Conference on , Volume: 1 , April 5-7, 2004 Pages:579 – 585

[8]Olcer, S.;” Decoder architecture for array-code-based LDPC codes” Global Telecommunications Conference, 2003. GLOBECOM '03. IEEE , Volume: 4 , 1-5 Dec. 2003 Pages:2046 - 2050 vol.4

[9] Xiao-Yu Hu; Eleftheriou, E.; Arnold, D.-M.; Dholakia, A.; “Efficient implementations of the sum-product algorithm for decoding LDPC codes” Global Telecommunications Conference, 2001. GLOBECOM '01. IEEE , Volume: 2 , 25-29 Nov. 2001 Pages:1036 - 1036E vol.2

[10]William Y. Zou and Yiyan Wu, "COFDM: an overview", IEEE Trans. On Broadcasting, vol. 41, no. 1, pp. 1-8, Mar. 1995.

[11] Futaki, H. and Ohtsuki, T., "Low-density parity-check (LDPC) coded OFDM systems", IEEE Vehicular Technology Conference, 2001. IEEE VTS 54th, vol. 1pp. 82-86, Jan 2001.