A Low-Power Low-Phase-Noise *LC* VCO With MEMS Cu Inductors

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***Abstract*—A 2–3 GHz CMOS inductance–capacitance (*LC*) voltage-controlled oscillator (VCO) integrated with high-Q micro-electromechanical systems (MEMS) Cu inductors is reported. While dissipating only 6.3 mW, a phase noise of -121 dBc/Hz at 600 kHz offset from 2.78 GHz carrier is achieved. This MEMS VCO has the largest power-frequency normalized figure-of-merit (12.5 dB) among the Si bipolar and CMOS *LC* VCOs.**

***Index Terms*—Micro-electromechanical systems (MEMS), voltage-controlled oscillators (VCOs).**

I. Introduction

THE integrated inductance–capacitance (*LC*) voltage-controlled oscillators (VCOs) are important building blocks for single-chip communications system. The primary challenge in designing VCOs is minimizing phase noise while maintaining smallest power consumption, which can be achieved by improving the poor quality factor (Q) of the on-chip inductors due to silicon substrate losses and series resistance of inductors [1]. High ohmic substrates usually provided by bipolar or BiCMOS processes can be adopted to limit the substrate losses [1]. However, for integration of the RF front-end with the digital baseband signal processing, a standard CMOS technology is mandatory [1]. Recently many state-of-the-art integrated *LC* CMOS VCOs have been implemented in 0.35-μm BiCMOS technology [2]–[4]. Even for these fully optimized VCOs, the excellent phase noise performance achieved is still limited by the Q of the integrated inductors. The other way to break the barrier is to reduce the inductor series resistance, which can be achieved by the use of post-processed Cu inductors, usually fabricated by MEMS technology. The attempt [5] in 0.5-μm bipolar technology has shown excellent phase noise performance but with a relatively larger power consumption (18 mW) than that ($\sim$ 10 mW) of CMOS VCOs [2]–[4] implemented in 0.35-μm BiCMOS technology. In this work, the performance of an integrated *LC* VCO implemented in standard 0.25-μm CMOS with 7-μm thick MEMS Cu inductors is reported. It is found that the use of high Q MEMS Cu inductors improves the performance of the integrated *LC* CMOS VCO substantially in terms of phase noise and power consumption.

Manuscript received November 12, 2004; revised December 17, 2004. This work was supported in part by the ROC Ministry of Economic Affairs under Grant 91EC17A05-S10017 and the National Science Council under Grant NSC93-2752-E002-002-PAE and NSC93-2215-E002-028. The review of this letter was arranged by Associate Editor J.-G. Ma.

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Digital Object Identifier 10.1109/LMWC.2005.850565

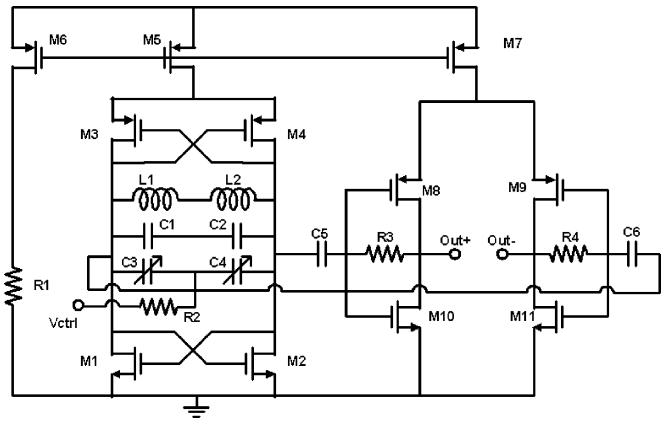

Fig. 1. VCO schematic.

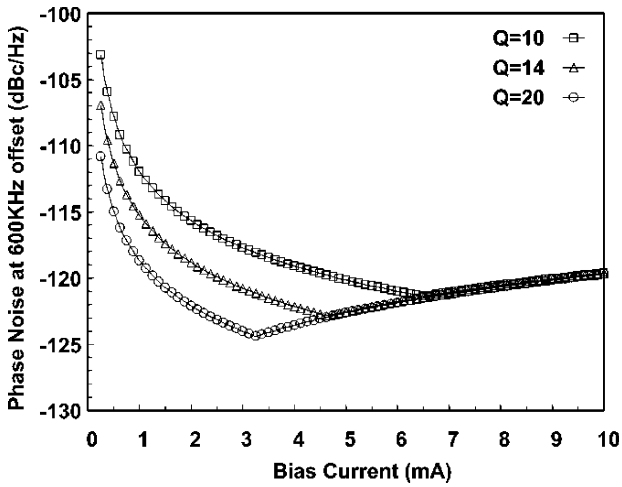

Fig. 2. Phase noise as a function of bias current.

II. Circuit Design

The schematic of our CMOS VCO is shown in Fig. 1. The double cross-connected nMOS (M1-M2) and pMOS (M3-M4) differential pairs provide the negative resistance. M5 and M7 mirror the pMOS current source (M6) for sourcing the core (M1-M4) and buffer stages (M8-M11). The determination of core bias current (I_{BIAS}) is nontrivial since it depends on the Q value of the chosen inductor. According to the formula proposed in [2], phase noise as a function of I_{BIAS} with different Q values can be plotted as shown in Fig. 2.

Optimal I_{BIAS} points are different for different Q values, respectively. The minimum phase noise corresponds to the point

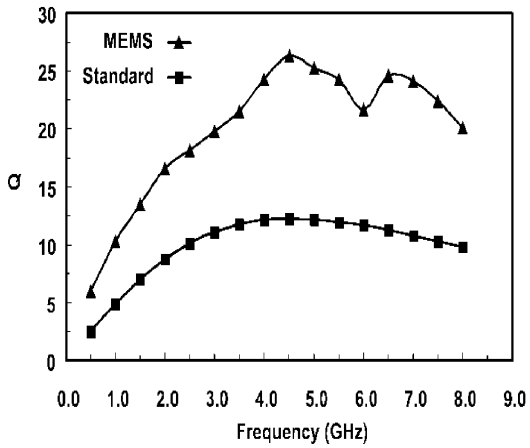

Fig. 3. Measured Q of the standard and MEMS inductors.

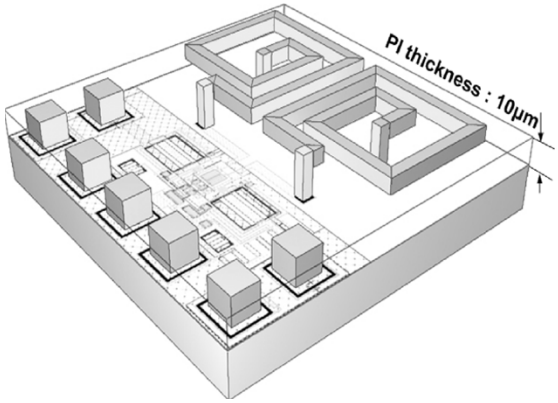

Fig. 4. Perspective view of MEMS VCO.

where the maximum voltage swing is first attained. Further increase of $I_{\rm BIAS}$ results in higher noise with a constant voltage swing and thus phase noise is degraded. In this work, $I_{\rm BIAS}$ is optimized for the VCO with MEMS Cu inductors.

III. MEMS Processing

VCOs with and without foundry-provided standard aluminum inductors, which we call STD VCO and MEMS VCO, respectively, were implemented in a standard 0.25-μm CMOS process for contrast experiment. The STD VCO and MEMS VCO have the following circuit parameters: transistor size M1-M4:$(W/L) = 25/0.35\ \mu{\rm m}/\mu{\rm m}$, M5: $(W/L) = 150/0.35\ \mu{\rm m}/\mu{\rm m}$, M6: $(W/L) = 50/0.35\ \mu{\rm m}/\mu{\rm m}$, M7: $(W/L) = 200/0.35\ \mu{\rm m}/\mu{\rm m}$, M8-M9:$(W/L) = 40/0.24\ \mu{\rm m}/\mu{\rm m}$, M10-M11:$(W/L) = 20/0.24\ \mu{\rm m}/\mu{\rm m}$, $C_1 = C_2 = 1.16$ pF, and $C_5 = C_6 = 26.5$ fF. $L1\ (= L2)$ is 2.5 nH and 1.53 nH for STD VCO and MEMS VCO, respectively. The Q of the foundry provided inductor is $\sim$ 10.1 at 2.4 GHz while that of the MEMS inductor is $\sim$ 18.2 as can be seen in Fig. 3, where the measured characteristics of Q versus frequency are shown. The peak-Q frequency of the MEMS inductor is 4.8 GHz. To prevent the degradation in tank Q, the AC coupling capacitance is $3 \sim 4$ times smaller than the buffer loading capacitance, which inevitably incurs significant loss in voltage swing. The perspective view of the VCO with the MEMS inductors formed on the die is illustrated in Fig. 4. The 24 μm$\times$ 26 μm Metal5 bond pads of the VCOs without foundry-provided inductors are left open for the connection of post-processed MEMS inductors to the underlying core circuitry. The MEMS inductors are fabricated in a commercial MEMS foundry (Kuender Corporation) to achieve the lowest phase noise and power consumption simultaneously. The thickness of the electroplated Cu is 7 μm. The inductors are spaced from the die by 10-μm polyimide. The die photo of the finished MEMS VCO is shown in the Fig. 5. Manufacturing issues, such as electrostatic discharge (ESD), involved with post processing CMOS devices may hinder the use of post-processed MEMS inductors from practical applications and any ESD protection may adversely impact the performance. However, it is found experimentally that the yield of the post-processed VCOs in the 5 mm $\times$ 5 mm die is 100% even without any ESD protection.

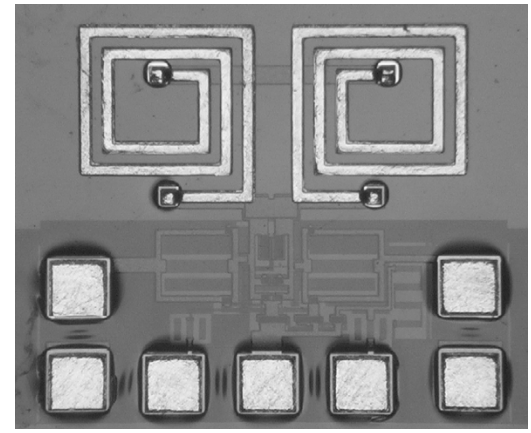

Fig. 5. Die photo of the MEMS VCO.

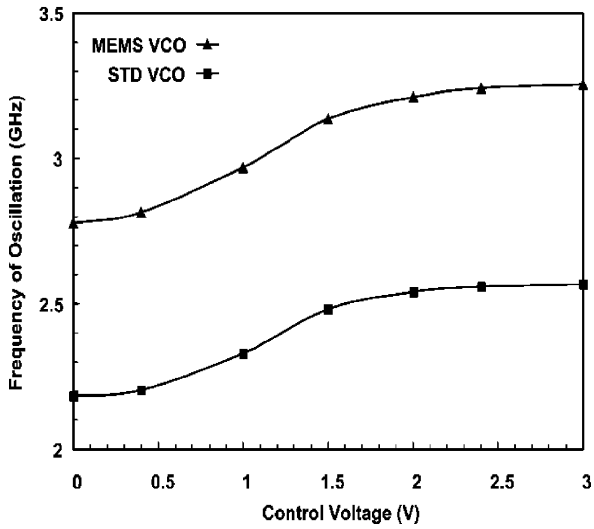

Fig. 6. VCO tuning range.

IV. Measured Results and Discussion

The core of VCOs draws a current of 2.1 mA from a 3-V supply. The MEMS VCO (STD VCO) operates from 2.78 (2.18) to 3.25 (2.57) GHz, which corresponds to a center frequency of 3.02 (2.38) GHz and a tuning range of 15.6% (16.4%), as shown in Fig. 6. The higher oscillation frequency of MEMS VCO is due to the smaller inductance used. The substrate capacitance of

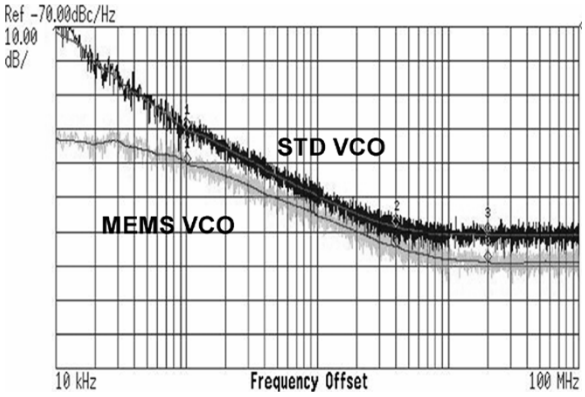

Fig. 7. Measured phase noise.

TABLE I
COMPARISON OF MEMS *LC* VCO

	Tech.	P_{sup} (mW)	f_o (GHz)	f_{offset} (Hz)	Phase Noise (dBc/Hz)	FOM (dB)
This work	CMOS STD	6.3	2.2	600k	-115.0	4.4
	CMOS MEMS	6.3	2.8	600k	-121.0	12.5
Ref [5]	Bipolar	18.2	2.0	100k	-106.0	5.6
Ref [7]	CMOS	15.0	2.6	600k	-122.0	9.1
Ref [8]	SiGe BiCMOS	2.8	2.8	1M	-122.0	12.8

the MEMS inductor with 10-μm thick polyimide is reduced and hence can also contribute to the increase of the center frequency.

The carrier power of MEMS VCO and STD VCO are -14.42 and -24.94 dBm, respectively, evidencing a higher Q is indeed achieved in MEMS VCO due to the use of thick Cu inductor. The oscillator phase noise is measured by using Agilent E4440A spectrum analyzer with phase-noise measurement utility in a shielding room. The plots of the phase noise versus the offset frequency from 2.78-GHz carrier (MEMS VCO) and the 2.18-GHz carrier (STD VCO) are shown in Fig. 7. The flattening off of the straight curves for larger offset frequencies ($>\sim$ MHz) is due to the limited dynamic range of the system [1].

The MEMS VCO shows a phase noise of -121 dBc/Hz at 600 kHz offset while dissipating only 6.3 mW. The achieved phase noise performance is benchmarked to the STD VCO that realizes a phase noise of -115 dBc/Hz at 600 kHz offset. For fair comparison of VCOs with different oscillation frequencies and power consumptions ($P_{\rm sup}$), the widely-accepted power-frequency-normalized figure-of-merit (FOM) [2], [6] given below is calculated and summarized in Table I for the recently reported 2–3 GHz band MEMS LC-VCOs [5], [7], [8] along with the VCOs of this work.

$$FOM = 10\log\left[\frac{kT}{P_{\rm sup}}\cdot\left(\frac{f_0}{f_{\rm off}}\right)^2\right] - L\{f_{\rm off}\} \qquad (1)$$

where $L\{f_{\rm off}\}$ represents the phase noise at an offset frequency $f_{\rm off}$ from the carrier frequency f_0. When compared to the STD VCO, our MEMS VCO has an 8.1 dB improvement in FOM at 600-kHz offset due to the use of high Q MEMS Cu inductors. The current consumption (2.1 mA) of our MEMS VCO core seems to be on the high-side compared to that (125 μA) of [8]. Nevertheless, the achieved FOM of this work is quite comparable to that of [8]. The MEMS VCO has the largest FOM of 12.5 dB among the $2\sim 3$ GHz-band Si bipolar and CMOS integrated *LC* VCOs.

V. CONCLUSION

VCOs with post processed MEMS inductors and foundry-provided aluminum inductors were implemented in a 0.25-μm CMOS process for comparison. It is found that the MEMS VCO shows an 8.1 dB improvement of power-frequency-normalized figure-of-merit than the standard VCO.

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