A NOVEL VIDEO SIGNAL PROCESSOR WITH RECONFIGURABLE PIPELINED ARCHITECTURE

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ABSTRACT

A programmable 133 MOPS (mega operations per second) processor is designed for video signal processing. It consists of Data-path Processing Part (DPP) and Address Generating Part (AGP). Through a flexible network, the DPP can be efficiently reconfigured as any types of pipelined architecture in terms of video coding algorithms. It is especially suitable to implement irregular algorithms, such as the fast discrete cosine transform (FDCT) and the three-step hierarchical search (3SHS) algorithm for motion estimation. The AGP can generate addresses to perform desired memory access operations for various irregular video coding algorithms. By using this video signal processor (VSP), video processing systems can be easily implemented, and video data can also be smoothly processed in single or multiple VSP configurations. The realization of MPEG-2 is evaluated, and its performance is also presented.

1. INTRODUCTION

With the recent advances in VLSI and ATM networking technology, low-cost video communication services appear possible. Several standards for image and video coding algorithms, such as CCITT H.261 [1], MPEG-2 (Moving Picture Experts Group) [2][3], and JPEG (Joint Photographic Experts Group)[4], have been recommended. In these standards, both the coder and decoder need high speed video coding operations, such as motion estimation (ME), motion compensation (MC), discrete cosine transform (DCT), loop filtering (LF), and variable length coding/decoding (VLC/VLD). Due to the complexity of these operations and the large amount of video data, Video Signal Processors (VSP's) will be required to have very high computing rates.

There are two approaches to implement the video coding algorithms. One is to use dedicated architectures [5]-[7]. The architectures offer a high performance processing capability, but they take considerable time and effort to fabricate and test. Thus, they have less flexibility . The other is to use programmable architectures [8]-[11]. Their main advantages are function flexibility and multiprocessing capability. However, their performance is not high due to complex architectures.

This paper proposes a programmable and reconfigurable video signal processor. It combines the flexibility of programmable architectures with the high performance of dedicated architectures. To achieve high performance and flexibility, the architecture is divided into DPP and AGP, which can efficiently calculate data and address, respectively. Owing to these improvements, a variety of video processing algorithms can be efficiently implemented in the VSP.

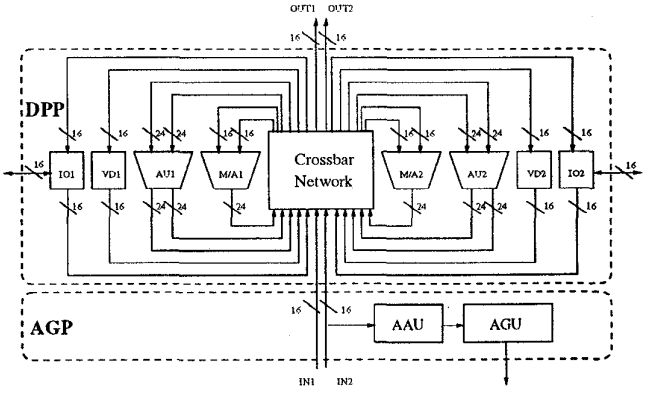

Figure 1. Block diagram of the VSP.

The organization of the paper is as follows: Section 2 describes the system architecture including data-path processing part, address generating part, and control mechanism. Section 3 uses FDCT to analyze the mapping process. Performance results with MPEG-2 algorithm and VLSI implementation are then described in section 4 and section 5, respectively. Section 6 gives a conclusion.

2. VSP ARCHITECTURE

2.1. Block Diagram

A block diagram of the VSP is shown in Fig. 1. It is composed of Data-path Processing Part (DPP) and Address Generating Part (AGP) [8][10]. The DPP contains a flexible network, 2 Multiplier/Adder's (M/A), 2 Arithmetic Unit's (AU), 2 Variable Delay's (VD), 2 input ports(IN), 2 output ports (OUT), and 2 programmable Input/Output ports (IO). These processing units are interconnected to operate in a pipelined fashion by a dynamically configurable crossbar network. The AGP contains Address Arithmetic Unit (AAU) and Address Generating Unit (AGU). It is designed to compute video data addresses efficiently. It is especially suitable to perform memory access operations about image and video processing. In addition, in order to meet high speed processing requirements, the DPP and the AGP have proprietary control mechanisms to control their processing units.

2.2. Data-Path Processing Part (DPP)

To ensure flexible and smooth data flow, a highly connective and non-blocking network is used to interconnect all kinds of processing units. The crossbar network which has equal or better features than multi-stage network meets these re-

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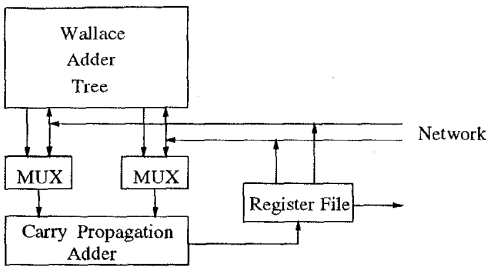


Figure 2. Architecture of Multiplier/Adder.

quirements [12]. However, a fully connective crossbar network occupies a very large area in VLSI. It makes VLSI implementation costly. To solve this issue, the network is partitioned into two smaller sub-networks. The two sub-networks can route the video data in parallel. This saves nearly 1/2 switches. Furthermore, the property of each processing unit is examined. If the connection between the two processing units is redundant, the switch between them will be eliminated. For example, no connection is needed from input port directly to one output port. Through the above process, the number of switches is reduced from 168 to 72. The reduced network is much smaller than the original one, and time delay gets also shorter.

A multiplier is usually located on the critical path of a digital signal processor. A 16-b × 16-b Booth multiplier with a Wallace-tree is designed to achieve high speed requirement [13]. However, there are no multiplications in some algorithms, such as Motion Estimation (ME). The existence of these multipliers will cause low utilization. To solve this problem, the adder in the multiplier can be selected to perform addition through a multiplexer. Therefore, the total utilization is improved. Fig. 2 shows the architecture.

AU can execute those instructions which are frequently used in video coding algorithms. For example, the instruction set contains the absolute value instruction, abs(a-b), which is employed in motion estimation, and the {a-b, a+b} instruction which is employed to execute butterfly-type operations in discrete cosine transform, discrete Hadamard transform, and other image processing algorithms.

The VD is a special unit for image and video processing. It can be utilized as the line memory which can store the preceding row of image. The data of the preceding row can be computed with the data of the current row. It saves an input port and the time spent on address generation and data transfer of the preceding row. Meanwhile, it can also serve as a time delay unit in signal flow graph (SFG).

Two input ports and two output ports are available for the reception and transmission of data, respectively. Another two I/O ports can be programmed to input data or output data. Users may utilize these I/O Ports in terms of the the property of video coding algorithms. Two mapping types, tree-type and non-tree type, for motion estimation are shown in Fig. 3.

2.3. Address Generating Part (AGP)

According to the characteristics of image and video processing algorithm, most data is processed in two-dimensional block access fashion, as shown in Fig. 4. Two-dimensional address generation of the image and the video data will be executed smoothly using the AGP, as shown in Fig. 5. The AGP is composed of Address Generating Unit (AGU) and

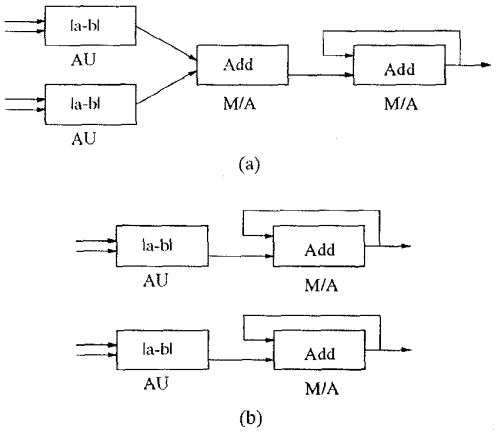


Figure 3. (a) Tree type motion estimation, (b) Non-tree type motion estimation.

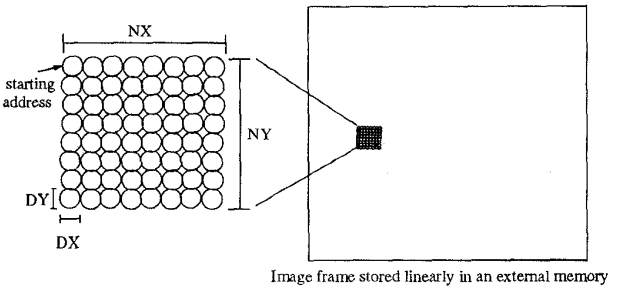


Figure 4. Address generation of a window in an image frame.

Address Arithmetic Unit (AAU).

Address Generating Unit (AGU) is a dedicated unit for video signal processing. Its function is to generate the address of each pixel in each block. In video coding algorithms, the window with size 16×16 or 8×8 is usually used. In CCITT H.261, MPEG-1, and MPEG-2 standards, different-sized blocks are needed, e.g. 16×16 blocks for motion estimation, 8×8 blocks for DCT and IDCT, and 3×3 blocks for loop filter. For most algorithms, only the starting address (SA) of the block varies regularly while the program is executing, such as DCT operation in MPEG-2 algorithm. Nevertheless, the 3-step motion estimation is an exception. Its starting address of each block is variable. This can be overcome by using the Address Arithmetic Unit (AAU). The Address Arithmetic Unit (AAU) is a programmable unit containing an adder, a register file, and a program memory. Its function is to compute the starting address of the next block. The block may be a variable-sized block located on any position. By programming it, many irregular types of memory access operations for image and video processing can be easily executed, e.g. 3-step motion estimation.

2.4. Control Mechanism

The DPP is designed to implement the SFG of video coding algorithms. It executes the program cyclically in a pipelined fashion. Various pipelined structures can be formed by configuring the crossbar network. In many presented programmable digital signal processor, a complex sequencer always occupies a significant part of the die size. To avoid

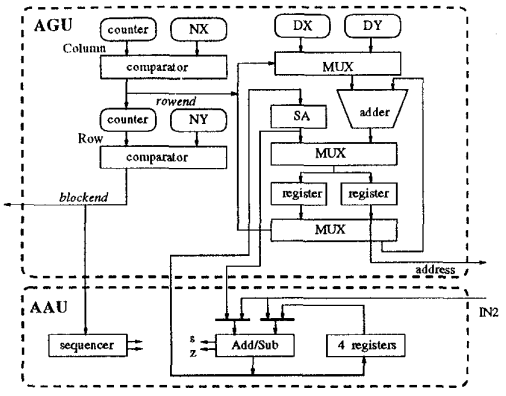


Figure 5. Architecture of Address Generating Unit.

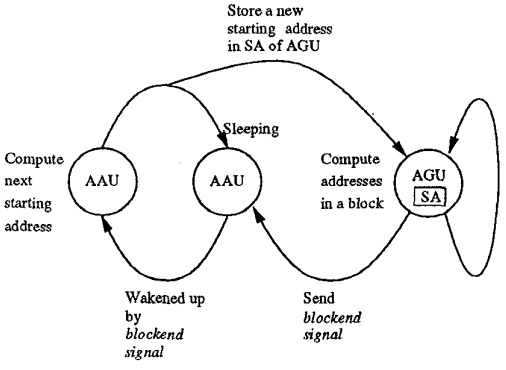


Figure 6. State flow graph of AG.

this complex sequencer, there is a local program memory in each processing unit of the DPP. The local program memory stores the program executed cyclically by the processing unit.

During AGU generating the address of the pixel data in the current block, there is enough time for AAU to compute the starting address of the next block. After the next starting address is generated, it is sent to the SA register. As soon as the starting address is stored in the SA register, the AAU falls asleep. It detects the signal *blockend* generated by the AGU, while it is sleeping. At the end of the current block, the AGU sends the signal *blockend* to wake the AAU up. Then the AGU uses the starting address in the SA register to handle the next block, and the AAU continues to compute the next one. They work in this way cyclically until the frame is finished, as shown in Fig. 6.

3. PERFORMANCE ANALYSIS

The fast DCT algorithm is used as an example to illustrate the mapping process between SFG and the VSP architecture. 8×8 DCT is used in CCITT H.261, JPEG, MPEG, and other video communication standards. After DCT, an image block is transformed into frequency domain. Then, the energy of the block is concentrated in only a few low-frequency coefficients. This technique is often used in image and video signal processing. However, the original algorithm of 8×8 DCT takes 64 multiplications and 64 additions. It is a high computation for a high speed application. There are many fast algorithms of DCT proposed. Due to their irregularity, it is difficult to implement these algo-

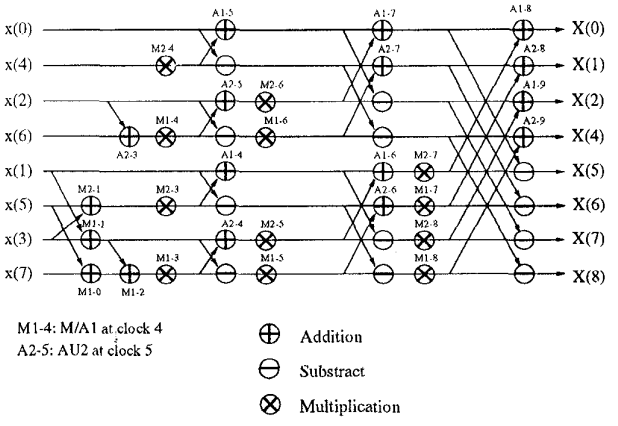


Figure 7. Mapping the FDCT to the DPP.

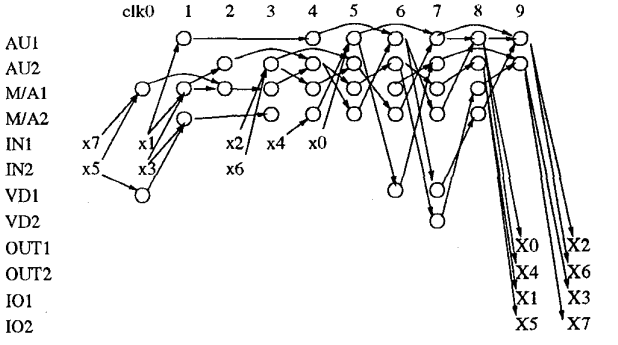


Figure 8. Time for executing FDCT on the DPP.

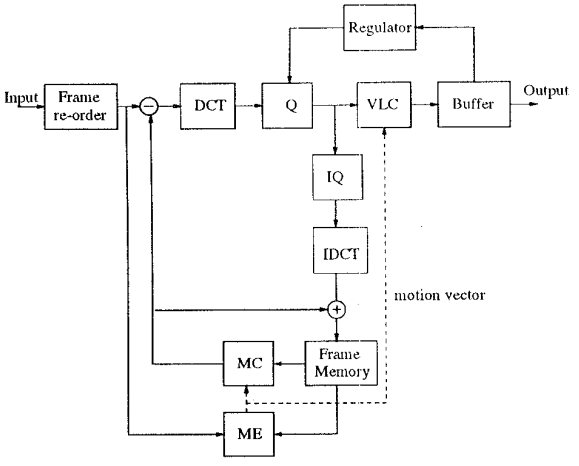
rithms on VLSI. The DPP has a flexible interconnection network which is suitable for the irregular algorithms. The fast algorithm [14] which is shown in Fig. 7 can be realized on the DPP. It is feasible to map the fast DCT to two or more DPP's for higher speed. AU1 and AU2 work from clock 1 through clock 9. M/A1 and M/A2 work from clock 0 through clock 8. Thus, the whole SFG of fast DCT is computed within 9 clocks in a pipelined way, as shown in Fig. 8.

4. APPLICATION FOR MPEG-2

To evaluate the performance of this architecture for video coding algorithms, we implemented a program of the MPEG-2. Fig. 9 shows the MPEG-2 compression scheme. In the MPEG-2 scheme, the execution time of the main operations, including ME, MC, DCT, IDCT, Q, IQ, subtraction, and addition, is listed in Table 1 [15]. In the table, "time" indicates clock cycles required to execute the operation for one macro block (MB : 16×16 pixels). The total time required for the main operations of the codec is evaluated as 5917 cycles. It is possible to realize the MPEG-2 standard by several chips if appropriate scheduling and partition are utilized.

5. VLSI IMPLEMENTATION

The layout of the VSP chip was designed by using Magic which is an interactive system for creating and modifying VLSI circuit layout. The VSP chip was implemented with a 1.2 μm CMOS technology. It contains 76.2K transistors.



DCT: Discrete Cosine Transform
IDCT: Inverse Discrete Cosine Transform
Q: Quantization
IQ: Inverse Quantization
VLC: Variable Length Coding
ME: Motion Estimation
MC: Motion Compensation

Figure 9. Simplified block diagram of an MPEG-2 video encoder.

Table 1. Performance for an MPEG2-Based Codec

Algorithm	Time (clock cycles/Macro Block)
ME (3 step)	3467
MC	42
DCT	865
IDCT	865
Q	194
IQ	194
Sub	194
Add	96
Total	5917

The layout is 7.2 mm × 9.14 mm. It can operate at a maximum clock of 22.2 MHz (45 ns/cycle). There are six parallel operations to be executed simultaneously in the DPP, so the performance is about 133 MOPS. Table 2 summarizes the features of the VSP chip.

6. CONCLUSION

A novel programmable video signal processor with a reconfigurable pipelined architecture is developed. The flexible structure makes complex video coding algorithm to be realized easily. The elaborate design for the processing units design of Data-path Processing Part and Address Generating Part are made to attain high performance requirements. It is shown by using this video signal processor (VSP), video processing systems can be easily implemented. An evaluation for the configuration of MPEG-2 has been made. The successful completion of MPEG-2 standard will accelerate to realize the Video-on-Demand service.

Table 2. Chip Features

Technology	TSMC 1.2 μm CMOS
Die Size	7.2 mm × 9.14 mm
Number of Transistors	76.2K
Number of Pins	169 pins
Instruction Cycle	45 ns
Performance	133 MOPS

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