CMOS exponential-control variable gain amplifiers

W. Liu, S.-I. Liu and S.-K. Wei

Abstract: New CMOS exponential-control variable-gain amplifiers (VGAs) are presented. The control signal can be either current-mode or voltage-mode. Since no multiplier is needed in the proposed circuits, the proposed VGAs can be very compact. For the case of supply voltages $V_{DD}=|V_{SS}|=1.5$ V, the power dissipation is only 0.48 mW. The gain control range of the proposed VGA can be 30 dB. The proposed circuits have been fabricated in a 0.5 μm n-well CMOS process. Experimental results are given to confirm the feasibility of the proposed VGAs, which are expected to be useful in analogue signal processing applications.

1 Introduction

Variable gain amplifiers (VGAs) can be widely used in analogue signal processing, such as disc drives [1], telecommunications [2, 3] and automatic gain control (AGC) circuits [4, 5]. Traditionally, a VGA can be realised by a multiplier with an input signal and an exponential one [5, 6]. However, unlike the inherent exponential characteristics of bipolar devices, there is no intrinsic exponential device in CMOS technologies. To realise the exponential function, the approximated Taylor series expansion [4–6] can be utilised. Alternatively, a pseudo-exponential function, which is given as (1) [7–9], can also be used to approximate the exponential function $\exp(2nx)$.

$$f(x) = \left(\frac{1+x}{1-x}\right)^n \approx e^{2nx} \quad (1)$$

where $|x|<1$.

In this paper, new CMOS exponential-control VGAs based on (1) are presented. Unlike the traditional design, the multiplier is not used in the proposed circuits. The exponential-control range can be tuned either by a current-mode signal or a voltage-mode signal. The proposed circuits have been fabricated in a 0.5 μm n-well CMOS process and the experimental results are given to demonstrate the proposed VGAs.

2 Circuit implementation

The proposed VGA is shown in Fig. 1. Assume that, transistors M1, M2 and M3 are biased in the triode region without body effect. The drain currents I_1, I_2 and I_3 can be expressed as

$$I_1 = \frac{K_{n1}}{2}\left(2(-V_{SS}-V_{Tn1})V_{DS1}-V_{DS1}^2\right) \quad (2)$$

$$I_2 = I_B - I_c + I_5 = \frac{K_{n2}}{2}\left(2(V_{in}-V_{SS}-V_{Tn2})V_{DS2}-V_{DS2}^2\right) \quad (3)$$

and

$$I_3 = I_B + I_c + I_6 = \frac{K_{n3}}{2}\left(2(V_{out}-V_{SS}-V_{Tn3})V_{DS3}-V_{DS3}^2\right) \quad (4)$$

where I_B is a bias current generated by M10 and M11 through a reference voltage V_B, I_c is a control current, $K_{n1,2,3}$ are the transconductance parameters and $V_{Tn1,2,3}$ are the threshold voltages of M1, M2 and M3, respectively. The current mirror (M7, M8 and M9) is used to duplicate the current I_1, so that

$$I_1 = I_4 = I_5 = I_6 \quad (5)$$

Assume that M4, M5 and M6 are perfectly matched (i.e. $K_{n4}=K_{n5}=K_{n6}$ and $V_{Tn4}=V_{Tn5}=V_{Tn6}$) and all of them are biased in saturation. According to the square-law characteristics of MOSFETs, the following equation can be obtained:

$$V_{GS4} = V_{GS5} = V_{GS6} = \sqrt{\frac{2I_1}{K_{n4}}} + V_{Tn4} \quad (6)$$

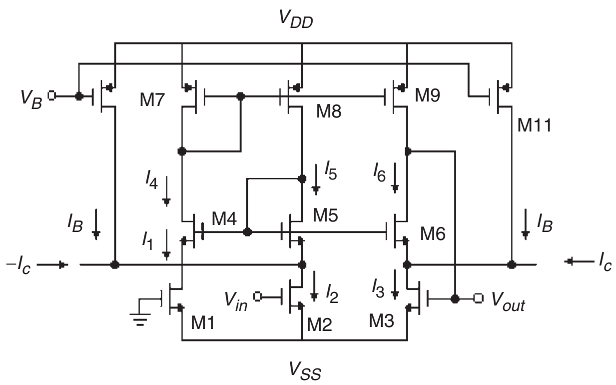

Fig. 1 *Current-mode exponential-control VGA*

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According to (6) and $V_{GS4} + V_{DS1} = V_{GS5} + V_{DS2} = V_{GS6} + V_{DS3}$, one can obtain

$$V_{DS1} = V_{DS2} = V_{DS3} \tag{7}$$

Since the source voltages of M4, M5 and M6 are equal (i.e. $V_{SB4} = V_{SB5} = V_{SB6}$), one can obtain $V_{Tn4} = V_{Tn5} = V_{Tn6}$. Assume that M1, M2 and M3 are perfectly matched (i.e. $K_{n1} = K_{n2} = K_{n3} = K_n$ and $V_{Tn1} = V_{Tn2} = V_{Tn3} = V_{Tn}$) according to (7) and substituting (2) into (3) and (4), one can obtain, respectively,

$$I_B - I_c = K_n \cdot V_{in} \cdot V_{DS2} \tag{8}$$

and

$$I_B + I_c = K_n \cdot V_{out} \cdot V_{DS3} \tag{9}$$

From (7), (8) and (9), one can have

$$V_{out} = V_{in} \cdot \frac{I_B + I_c}{I_B - I_c} = V_{in} \cdot \frac{\left(1 + \frac{I_c}{I_B}\right)}{\left(1 - \frac{I_c}{I_B}\right)} \tag{10}$$

Comparing (10) with (1) and provided that $I_c < I_B$, one can obtain

$$V_{out} \approx V_{in} \cdot \exp\left(2 \cdot \frac{I_c}{I_B}\right) \tag{11}$$

From (11), a VGA can be realised and its gain can be exponentially controlled by the current I_c.

Figure 2 shows that, if the gates of M10 and M11 are connected to the voltages $V_b + V_c$ and $V_b - V_c$ (where V_b is a bias voltage and V_c is a control voltage), respectively, a voltage-mode exponential-control VGA can also be realised. Assume that M10 and M11 are perfectly matched (i.e. $K_{p10} = K_{p11} = K_p$ and $V_{Tp10} = V_{Tp11} = V_{Tp}$) and both of them are embodied in individual wells to avoid the body effect. If both M10 and M11 are biased in saturation, one can obtain

$$I_{10} = \frac{K_p}{2}\left(V_{DD} - (V_b + V_c) - |V_{Tp}|\right)^2 \tag{12}$$

and

$$I_{11} = \frac{K_p}{2}\left(V_{DD} - (V_b - V_c) - |V_{Tp}|\right)^2 \tag{13}$$

Replacing '$I_B - I_C$' and '$I_B + I_C$' in (3) and (4) by I_{10} and I_{11}, respectively, and according to (5)–(7), one can obtain

$$I_{10} = K_n \cdot V_{in} \cdot V_{DS2} \tag{14}$$

and

$$I_{11} = K_n \cdot V_{out} \cdot V_{DS3} \tag{15}$$

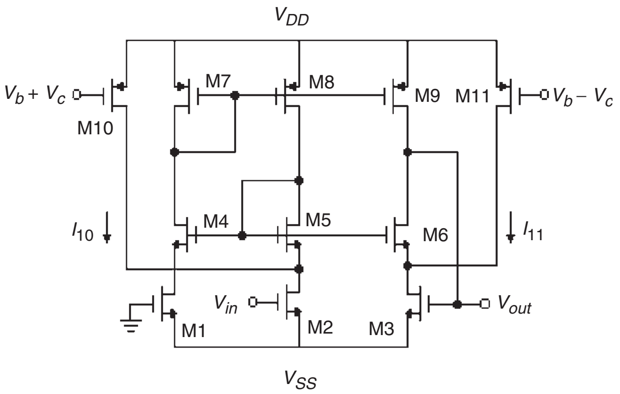

Fig. 2 *Voltage-mode exponential-control VGA*

From (7), (14) and (15), one can obtain

$$\begin{aligned} V_{out} = V_{in} \cdot \frac{I_{11}}{I_{10}} &= V_{in} \cdot \frac{\left(V_{DD} - (V_b - V_c) - |V_{Tp}|\right)^2}{\left(V_{DD} - (V_b + V_c) - |V_{Tp}|\right)^2} \\ &= V_{in} \cdot \left(\frac{(V_{DD} - V_b - |V_{Tp}|) + V_c}{(V_{DD} - V_b - |V_{Tp}|) - V_c}\right)^2 \\ &= V_{in} \cdot \left(\frac{1 + \frac{V_c}{V_{DD} - V_b - |V_{Tp}|}}{1 - \frac{V_c}{V_{DD} - V_b - |V_{Tp}|}}\right)^2 \end{aligned} \tag{16}$$

Comparing (16) with (1) and providing that $V_b < 0$ and $V_{DD} - V_b > |V_{Tp}|$, one can obtain

$$V_{out} \approx V_{in} \cdot \exp\left(4 \cdot \frac{V_c}{V_{DD} - V_b - |V_{Tp}|}\right) \tag{17}$$

From (17), a VGA can be realised and its gain can be exponentially controlled by the voltage V_c. According to (11) and (17), if two proposed VGAs are cascaded, then the output exponential-control range can be further increased.

To keep the proposed VGAs working properly, M1, M2 and M3 should be biased in the triode region and other transistors should be in saturation. Since $I_B - I_C$ (also I_{10} in Fig. 2) must flow into the drain of M2, the operating range can be derived as

$$V_{ss} + V_{Tn} \le V_{out} \le V_{DD} - \sqrt{\frac{2I_1}{K_{p9}}} \tag{18}$$

and

$$V_{in} > 0 \tag{19}$$

where I_1 is defined in (2) and K_{p9} are the transconductances of M9.

If the threshold voltages of M1, M2 and M3 are mismatched due to the process variation, for example, $V_{Tn1} = V_{Tn}$, $V_{Tn2} = V_{Tn} + \Delta V_{Tn2}$, and $V_{Tn3} = V_{Tn} + \Delta V_{Tn3}$, then (10) can be written as

$$V_{out} = V_{in} \cdot \frac{I_B + I_c - K_n \cdot \Delta V_{Tn2} \cdot V_{DS}}{I_B - I_c - K_n \cdot \Delta V_{Tn2} \cdot V_{DS}} \tag{20}$$

Based on the same mismatch assumption, (14) can be written as

$$V_{out} = V_{in} \cdot \frac{\left(V_{DD} - (V_b - V_c) - |V_{Tp}|\right)^2 - K_n \cdot \Delta V_{Tn3} \cdot V_{DS}}{\left(V_{DD} - (V_b + V_c) - |V_{Tp}|\right)^2 - Kn \cdot \Delta V_{Tn2} \cdot V_{DS}} \tag{21}$$

According to (20) and (21), the mismatch of the threshold voltages of M1–M3 will cause the nonlinear errors of the proposed VGAs. If the nonlinear errors are significant, long-channel devices for M1, M2 and M3 can be used to reduce the errors.

Again, if the transconductances of M1, M2 and M3 are mismatched, for example, $K_{n1} = K_n$, $K_{n2} = K_{n1} + \Delta K_{n2}$, and $K_{n3} = K_{n1} + \Delta K_{n3}$, then (10) can be written as

$$V_{out} = V_{in} \cdot \frac{I_B + I_c - \Delta K_{n3} \cdot \left((V_{out} - V_{ss} - V_{Tn}) \cdot V_{DS} - V_{DS}^2\right)}{I_B - I_c - \Delta K_{n2} \cdot \left((V_{in} - V_{ss} - V_{Tn}) \cdot V_{DS} - V_{DS}^2\right)} \tag{22}$$

Based on the same mismatch assumption, (14) can be written as

$$V_{out} = V_{in} \cdot \frac{\left(V_{DD} - (V_b - V_c) - |V_{Tp}|\right)^2 - \Delta K_{n3}\left((V_{out} - V_{ss} - V_{Tn}) \cdot V_{DS} - V_{DS}^2\right)}{\left(V_{DD} - (V_b + V_c) - |V_{Tp}|\right)^2 - \Delta K_{n2}\left((V_{in} - V_{ss} - V_{Tn}) \cdot V_{DS} - V_{DS}^2\right)} \quad (23)$$

According to (22) and (23), the variation of the transconductances of M1–M3 will contribute the nonlinearities of the proposed VGAs. However, through careful layout considerations and long-channel devices, the deviation can be reduced.

3 Experimental results

The proposed VGAs have been fabricated in a 0.5 μm n-well CMOS process. The die photograph is shown in Fig. 3. The aspect ratios of all the transistors for the proposed circuit are listed in Table 1 and the experiments were performed with the supply voltages $V_{DD} = |V_{SS}| = 1.5V$. The experimental results of Fig. 1 are shown in Fig. 4*a*. The input voltage V_{in} was set to 0.25 V, 0.3 V and 0.35 V, respectively, and the bias current I_B was 30 μA. As the control current I_c varies in the range −25 to +25 μA, the output voltage varies in the range 0.15–0.9V, which corresponds to a dynamic range of about 15 dB. The input range of the proposed VGA is limited by (19). As the input voltage V_{in} was increased to 0.55 V, the measured output range can be about 13.5 dB. Figure 4*b* shows the linearity gain errors between the measured results and the theoretical values calculated by (11). According to Fig. 4*b* the linearity gain errors are within ±0.5 dB. Also, the power dissipation is about 0.63 mW (I_c = 25 μA, V_{in} = 0.35 V). The experimental results confirm the theoretical analysis calculated by (11). Figure 5*a* shows the experimental results of the proposed VGA shown in Fig. 2. The experiments were performed with the input voltage V_{in} = 0.15 V, 0.2 V and 0.25 V, respectively, and the bias voltage V_b was set to −0.2 V. As the control voltage V_c varies in the range −0.35 to +0.35 V, the output voltage varies in the range 0.03–1.15 V, which corresponds to an output dynamic range of about 30 dB. As the input voltage V_{in} was increased to 0.5 V, the measured output range can be about 25 dB. Figure 5*b* shows the linearity gain errors between the measured results and the theoretical values calculated by (17). According to Fig. 5*b* the linearity gain errors are within ±0.5 dB. Also the power dissipation is 0.48 mW (V_c = 0.35 V, V_{in} = 0.25 V). The experimental results confirm the theoretical analysis calculated by (17).

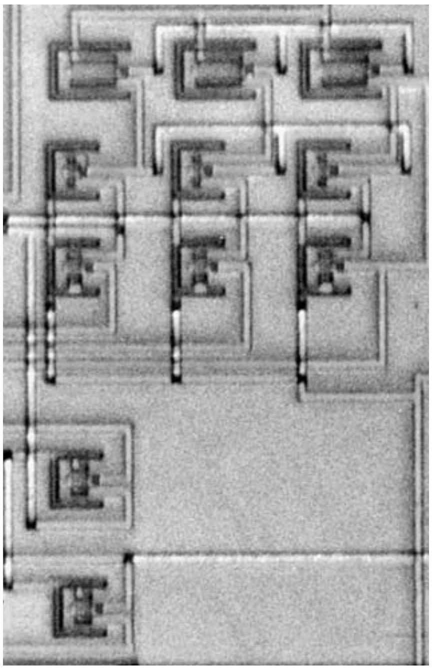

Fig. 3 *Die photo of the exponential-control VGA in Figs.1 and 2*

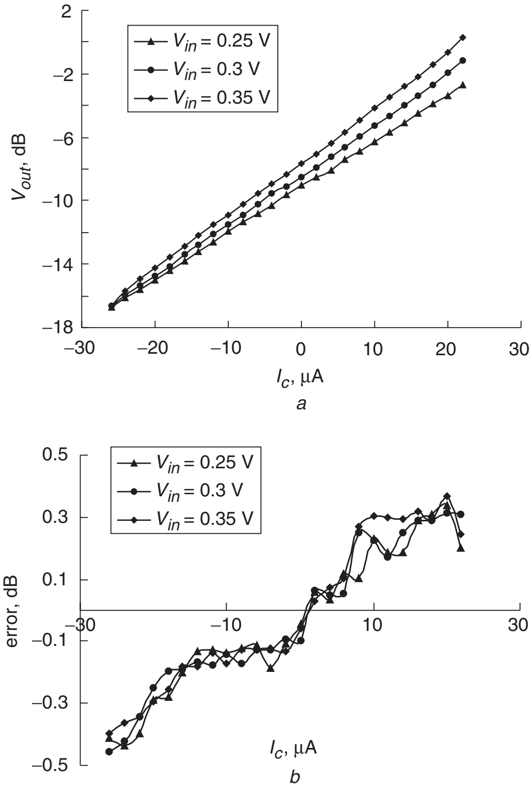

Fig. 4 *Results for the proposed current-mode exponential-control VGA*
a Experimental results
b Linearity gain errors between measured results and theoretical values

Table 1: Aspect ratios of the MOSFETs of the proposed exponential-control VGA

Transistors	Aspect ratio (*W/L*) (μm/μm)
M1–M3	2/1
M4–M6	1/1
M7–M9	7.5/1
M10, M11	2.5/1

The frequency response of Fig. 1 is shown in Fig. 6*a*, which was performed with the control current I_c = −5 μA, 0 μA and 5 μA and the corresponding −3 dB bandwidth can be 56.1 MHz, 38.9 MHz and 26.2 MHz, respectively. Also the corresponding input referred noise values are 147.6, 124.5 and 115.8 nV/(Hz)$^{1/2}$, respectively. Figure 6*b* shows the frequency response of the proposed voltage-mode exponential-control VGA. As the control voltage V_c = −0.05 V, 0 V and 0.05 V, the corresponding −3 dB bandwidth can be 21.9 MHz, 8.9 MHz and 4.23 MHz, respectively. Also, the corresponding input referred noise values are 151.2, 138.8 and 126.9 nV/(Hz)$^{1/2}$, respectively. The summary of the experimental results is listed in Table 2.

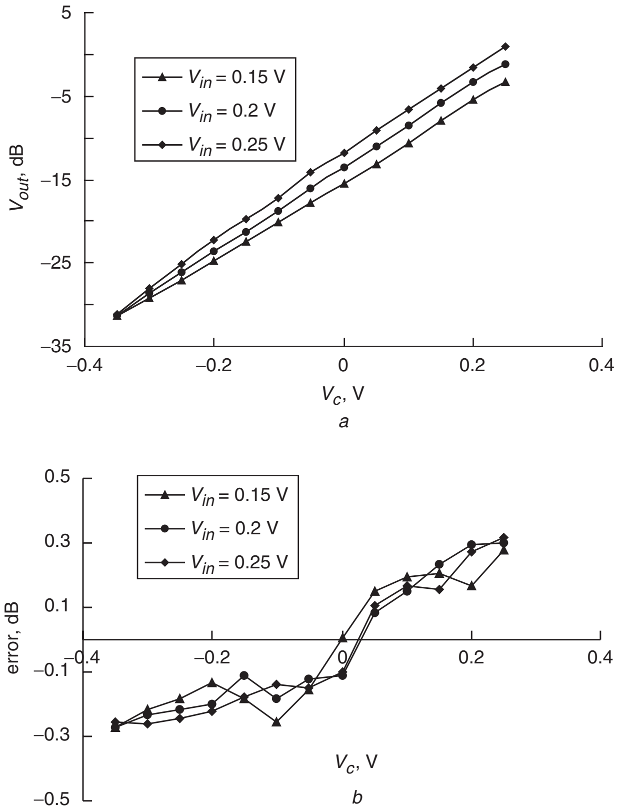

Fig. 5 *Results for the proposed voltage-mode exponential-control VGA*
a Experimental results
b Linearity gain errors between measured results and theoretical values

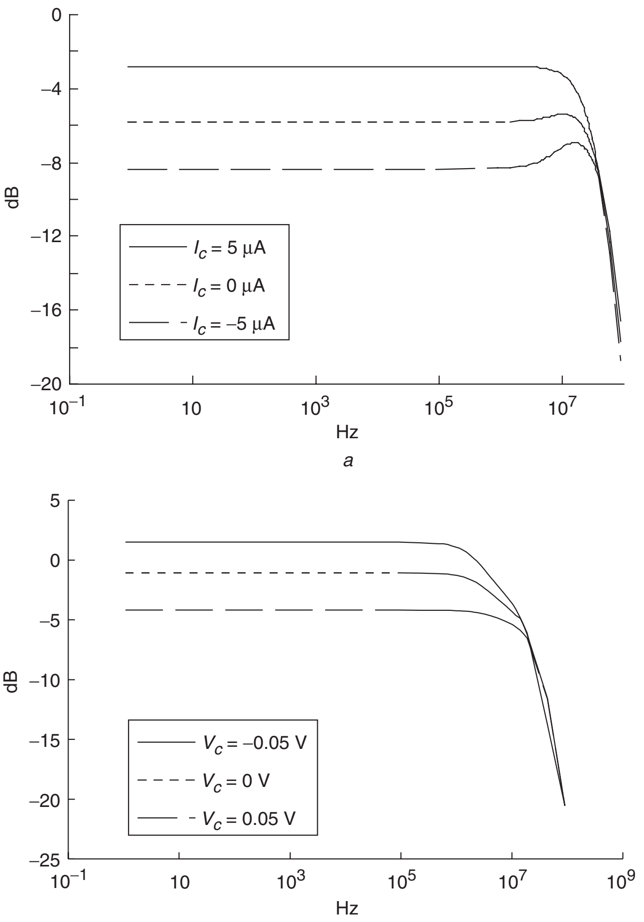

Fig. 6 *Frequency response of the proposed VGA*
a Current-mode exponential-control VGA
b Voltage-mode exponential-control VGA

Table 2: Summary of experimental results

Parameter	Current-mode VGA	Voltage-mode VGA
Supply voltage	±1.5 V	±1.5 V
Minimum gain	−16.5 dB	−31.4 dB
Maximum gain	0.26 dB	−0.89 dB
Linearity gain error	±0.5 dB	±0.5 dB
−3dB frequency	56.1 MHz (at $I_c = -5\,\mu A$)	21.9 MHz (at $V_c = -0.05\,V$)
	38.9.1 MHz (at $I_c = 0\,\mu A$)	8.9 MHz (at $V_c = 0\,V$)
	26.2 MHz (at $I_c = 5\,\mu A$)	4.23 MHz (at $V_c = 0.05\,V$)
Input range	0–0.55 V	0–0.5 V
Output range	0.15–0.9 V	0.03–1.15 V
Input referred noise	146.6 $nV/(Hz)^{1/2}$ (at $I_c = -5\,\mu A$)	151.2 $nV/(Hz)^{1/2}$ (at $V_c = -0.05\,V$)
	124.5 $nV/(Hz)^{1/2}$ (at $I_c = 0\,\mu A$)	138.8 $nV/(Hz)^{1/2}$ (at $V_c = 0\,V$)
	115.8 $nV/(Hz)^{1/2}$ (at $I_c = 5\,\mu A$)	126.9 $nV/(Hz)^{1/2}$ (at $V_c = 0.05\,V$)
Power consumption	0.63 mW	0.48 mW

4 Conclusions

In this paper, new CMOS exponential-control variable-gain amplifiers have been developed. Only a small number of transistors is used in the design, and the power dissipation is very low. Experimental results have been given to confirm the validity of the theoretical analysis. The proposed circuits are expected to be useful in the design of an AGC and other analogue signal processing applications.

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