行政院國家科學委員會補助專題研究計畫成果報告

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※「K-頻段無線收發關鍵元組件之研究」子計畫三：※

※ 升降頻器之研製(1/3)(2/3)(3/3) ※

※ Research and Development of Down- and Up-Converters ※

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計畫類別：☐個別型計畫　☑整合型計畫

計畫編號：NSC 88-2219-E-002-015

NSC 88-2219-E-002-020

√ NSC 89-2219-E-002-042

執行期間：87 年 8 月 1 日至 90 年 7 月 31 日

計畫主持人：王　暉

共同主持人：

本成果報告包括以下應繳交之附件：

☐赴國外出差或研習心得報告一份

☐赴大陸地區出差或研習心得報告一份

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☐國際合作研究計畫國外研究報告書一份

執行單位：

中　華　民　國　90 年　10　月　11　日

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Research and Development of Down- and Up-Converters

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一. 中文摘要（關鍵詞：K-頻段，單晶微波積體電路、降頻器、升頻器、收發機。）

本計畫預備研究及設計 K-頻段(21-26 GHz)之降頻器與升頻器元組件。該元組件係應用於微波電信機之傳送接收器。製作此微波電路晶片，將使用國外之砷化鎵單晶微波電路之代工之高速場效電晶體製程與異質接面雙極性電晶體製程。此升降頻器中之電路將包含低雜訊放大器、混波器及中頻放大器等。

在此三年計畫中，元件模型、電路設計及佈局、晶片製作與測試均將進行。在電路設計方面，我們使用國科會晶片中心所提供之高速場效電晶體與異質接面雙極性電晶體代工製程為主。第一年計畫中，將用現有之模式進行單一功能電路之初步設計，同時設計測試電路、而後製作第一循環之晶片；混成電路實驗亦將進行以驗證線路之設計理念。第一年計畫中，已完成製作第一循環之單一功能電路之晶片，同時並完成部分電路之測試。第二年度除繼續進行電路量測工作外，並利用 0.15 微米高速場效電晶體以及異質接面雙極性電晶體的製程，進一步設計各項單一及多功能晶片。第三年計畫中則加入製作在 K 頻帶的低雜訊放大器與單平衡混頻器模組，以及 20 兆赫的介電質振盪器。

Abstract (Keywords : K-band, MMIC, Downconverter, Upconverter, Transceiver.)

This project is aimed at the development and the design of K-band (21-26 GHz) downconverter and upconverter components for microwave radio transceiver applications using commercial foundry GaAs MMIC process technologies. The components will include low noise amplifiers, mixers and IF amplifiers.

In this 3-year project, device modeling, MMIC design, chip layout, fabrication and chip evaluation will all be exercised. In the MMIC design portion, we use the HEMT and HBT foundry service provided by CIC. In the first year, we have completed individual single-function components based on existing models. Part of the circuits have been measured. In second year, in addition to the on going chip measurement effort, we used the 0.15-μm PHEMT and HBT MMIC processes to further develop the various single- and multi-functional MMIC chips. In the third year we designed and produced K band low noise amplifier and single balance mixer module, and 20GHz dielectric resonator oscillator.

二. 計畫緣由與目的

There has been some research and development effort devoted in low microwave frequency range (< 10 GHz) MMIC frequency converters in Taiwan. The goal of this project is to push the MMIC frequency converters design technology to K-band (20-30 GHz) and demonstrate the up- and down-converters implemented in MMIC chips. Since the GaAs HEMT and HBT MMIC process technologies are available through commercial foundries, we used of the accessible MMIC processes to develop learn the MMIC design and modeling techniques.

This project provided a starting point of frequency converter MMIC development to K-band frequency in Taiwan and also established the infrastructure in our institute. The importance of this step-stone for future wireless MMIC technology development is obvious.

三. 研究方法與結果

(1) Device model investigation

For each solid-state device, the device figure of merit (FOM) need to be calculated in order to decide the circuit topology, e.g., f_T, f_{max}, maximum available gain of the transistor and cut-off frequency of the diode. For those devices which the models are not available, we need to perform the device dc and RF characterization and generate the model.

(2) Passive model library establishment

Mainly for CPW component.

(3) Circuit topology trade study and initial circuit design

After the device FOM is obtained, the gain stage number of amplifiers can be determined. During the trade study, some of hybrid form circuit will be constructed and tested to verify some of the concept.

(4) Circuit simulation, detailed design and layout

In MMW frequency, the EM analysis of entire matching structure may be needed.

(5) Circuit fabrication and evaluation

We plan to use the 0.2 micron PHEMT MMIC process and get the chip fabricated through CIC of National Science Council. For circuit testing, on-wafer probing is planned to avoid the complicated fixture test.

(6) Refine device models for next iteration

After the testing of both circuit and test structures have been complete, we will investigate the measure date and compare with the simulated results and then conduct the necessary model refinement. The next iteration design will be based on the updated models and the lesson-and-learns in the designs from the previous iterations.

(7) LNA

The low noise amplifier was designed using four-finger 120-μm PHEMT to operate at 21 to 26 GHz [3]. Inductive T transformers were used to match the device impedance to 50 Ω input and output. MIM capacitors were used for dc block and RF bypass. Fig. 4(a) and 4(b) show the chip photo and the measured small-signal gain and return loss of two-stage LNA. At 24 GHz, the small signal gain is 16.4 dB and input/output return losses are 7.5/11.6 dB.

(8) Driver Amplifier

The driver amplifier was designed using 120-μm PHEMT to drive 300-μm PHEMT. Inductive T transformers were used to match the device impedance to 50-ohm input and output [4]. The 90 ° hybrid, Lange coupler, and the single-end design are used as the balanced amplifier. MIM capacitors were used for DC blocking and RF bypassing. Fig. 5(a) and 5(b) show the chip photo and the measured small-signal gain of two-stage single-ended PA, the single-end amplifier demonstrated a small signal gain of 19 dB at 24 GHz. The power performance of the single-ended one is shown in Fig. 5(c). It has a 1-dB compressed power point (P_{1dB}) of 14.6 dBm at 22 GHz.

(9) Mixer

The subharmonically pumped mixer used two anti-parallel diodes each with four gate finger of 40 μm width to operate from 21 to 26 GHz of RF frequency. This circuit is suitable for both frequency upconversion and downconversion. Fig. 6(a) and 6(b) show the chip photo and the measured results of the subharmonically pumped mixer. The measured conversion loss is 12 dB for up conversion and 14 dB for down conversion.

(10) IF Amplifier

Five PHEMTs with a total gate periphery of 660 μm were used as the active devices for these amplifiers [5], [6]. Both microstrip line and GCPW are used to form the artificial gate and drain transmission lines. They are periodically loaded with the capacitive gate and drain impedance of the FET's forming lossy transmission line structures of different characteristic impedance and propagation constant. The resultant effective input and output propagation structures acted as gate and drain lines. An RF signal applied at the input end of the gate line travels down the line to the other end, where it is absorbed by the terminating impedance. The chip photos are shown in Fig. 7(a) and 7(c). Fig. 7(b) and Fig. 7(d) show the measured small-signal gain and return loss via on-wafer probing. The microstrip-line design demonstrated a small signal gain of 12±2.5 dB, and the GCPW design has a small-signal gain of 10±0.5 dB.

In addition, we also complete the circuit designs using the GCS HBT process and TRW 0.15-μm PHEMT process. Table 1 lists the results of these circuits.

(11) LNA and single balance Mixer receiver chip

LNA design procedure is just similar with option (7), however the single balance mixer is just different t from the subharmonically pumped mixer described. The designed single balance mixer uses 90 lange coupler and then the signal through the schotky diode the produce the intermodulation signal and filter out the IF signal what we design for. This circuit is suitable for downconvertor. The layout of the whole module and measurement results of the two circuit are shown in Fig. 8(a), Fig. 8(b), Fig 8(c) and Fig. 8(d) respectively. The small signal gain >20dB between 21~26GHz and return loss of the input and output also >10dB in band. The conversion loss of the mixer is 10dB loss roughly in the LO power 10dBm situation and LO to RF isolation is 5dB and LO to IF isolation is 35dB.

(12) DRO

Using the characteristic of the source feedback to produce the unstability of the chip and the design of the matching circuit of the drain end to make the circuit to operate in linear oscillation region of operating frequency. The DRO module picture is shown in Fig. 9(a). Dielectric resonator is put on a 50 ohm mictrostrip line which is on Teflon substrate. One side of the 50 ohm line is connected with 50 chip resistor and other side is connect the gate of the device. The source end of the device is connect one open stub and a short stub to make sure the oscillation may occur. The DRO chip photo is shown in Fig. 9(b). The initial test result is the spectrum of the DRO and the output power is 5.7dBm, which is shown in Fig. 9(c).

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vol. 7, no. 8, pp. 219-221, Aug. 1997.

Table 1

First year MIC and MMIC design summery

MMICs		
NAME	DESCRIPTION	PERFORMANCE
LNA001	◆1-stage SE, 120-μm PHEMT ◆microstrip line design	G = 9 dB NF = 2.3 dB @24 GHz
LNA002	◆2-stage SE, 120-μm each stage ◆microstrip line design	G = 17.8 dB NF = 3.2 dB @ 24 GHz
Mix001	◆4-finger, 40-μm gate-PHEMT diode ◆singly balanced design with a Lange coupler	Convertion loss = 8 dB with RF @ 24 GHz, IF @ 2.5 GHz at LO of 10 dBm
Mix002	◆4-finger, 40-μm gate-PHEMT diode ◆singly balanced design with a modified Rat-race	Convertion loss = 9 dB with RF @ 20 GHz, IF @ 1 GHz at LO of 10 dBm
Mix004	◆4-finger, 40-μm gate-PHEMT diode ◆subharmonically pumped mixer for both up and down-frequency conversion	Conversion loss = 12~13 dB for up and 11~13 dB for down-conversion with LO of 7dBm
PA001	◆1-stage ◆6-finger, 300-μm	G =6.5 dB @24GHz PAE = 26.9%
PA002	◆2-stage SE, 0.12mm driving 0.3 mm	G =13.3 dB @24GHz PAE = 19.3%
PA003	◆2-stage balanced design, 0.12 mm driving 0.3 mm	G = 12.9 dB @24GHz PAE = 21.4%
WAMP	◆SE, 6-finger, 300-μm gate-PHEMT	G = 1561 dB
MICs		
Mixer	◆Doubly balanced diode mixer ◆Both up and down-frequency conversion	Conversion loss = 15 dB for up and 12 dB for down-conversion with LO of 4dBm

Table 2

Second year MMIC design Summary

0.15-μm PHEMT Process		
Name	Description	Simulated Results
FIL001	◆Active filter ◆4-finger, 120-μm PHEMT ◆microstrip line design	G = 7 dB @19 GHz
LNA	◆4-finger, 120-μm PHEMT ◆microstrip line design	G=21 dB, NF=1.7 dB @ 24 GHz
Mixer	◆4-finger, 40-μm gate-PHEMT diode ◆singly balanced design with a Lange coupler	Conversion loss < 10 dB Return loss > 10 dB
HBT Process		
Name	Description	Measured Results
VCO	◆12-μm² emitter area HBT ◆microstrip line design	Frequency : 29 GHz Power : -5 dBm

■ **Table 3**

Third year MMIC design Summary

0.15-μm PHEMT Process		
Name	Description	Simulated Results
LNA and Mixer	◆4-finger, 120-μm PHEMT for LNA ◆Schottky Diode for Mixer ◆microstrip line design ◆singly balanced design with a Lange coupler for Mixer	G=22dB NF=1.7dB @23GHz for LNA Conversion loss = 8dB Return loss >10dB for Mixer
DRO	◆DR for resonator ◆microstrip line design	Output power 2.7dBm

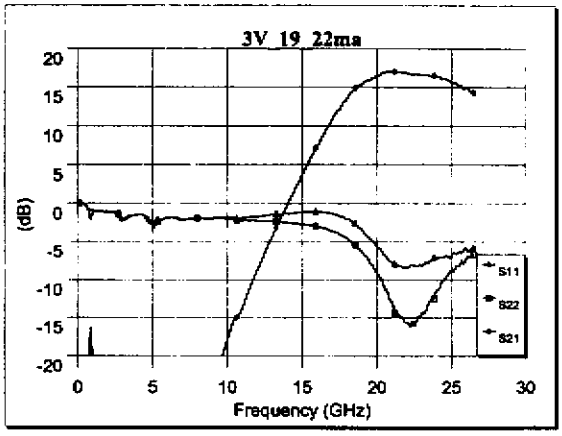

Figure 1. Test result of two-stage LNA(S parameter).

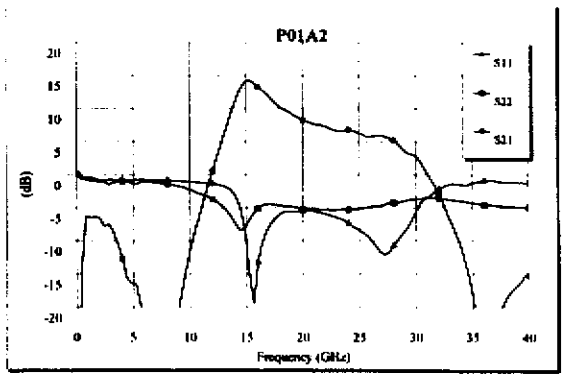

Figure 2. Test result of one-stage PA(S parameter).

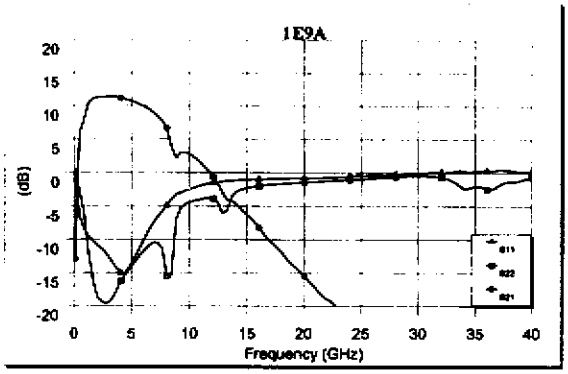

Figure 3. Test result of 1-6 GHz IF amplifier.

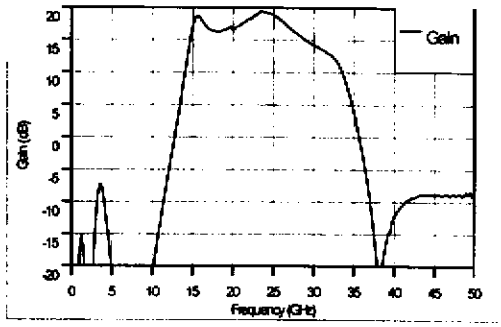

Fig. 5(b) Measured small-signal gain of two-stage single-ended PA.

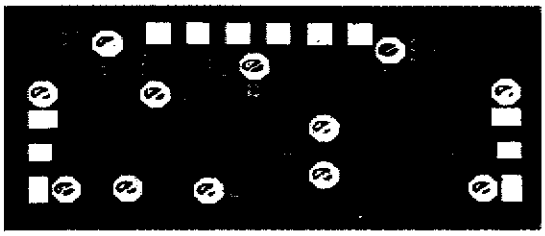

Fig. 4(a) The chip photo of two-stage LNA.

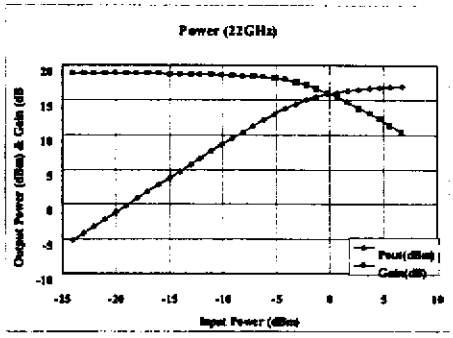

Fig.5(c) Measured power performance of two stage single-ended PA.

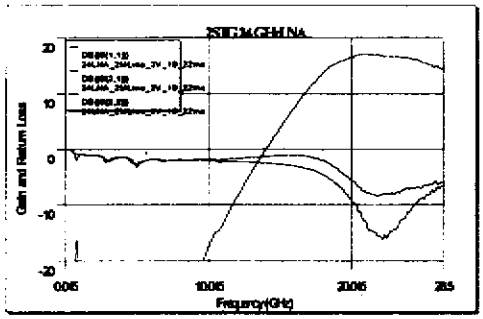

Fig. 4(b) Measured small-signal gain and return loss of two-stage LNA.(conversion loss)

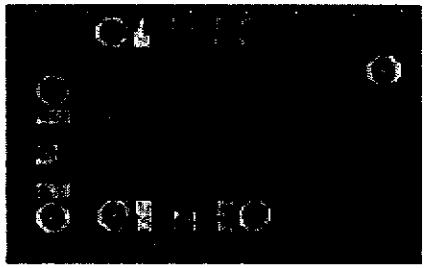

Fig. 6(a) Chip photo of the subharmonically pumped mixer.

Fig. 5(a) The chip photo of two-stage PA.

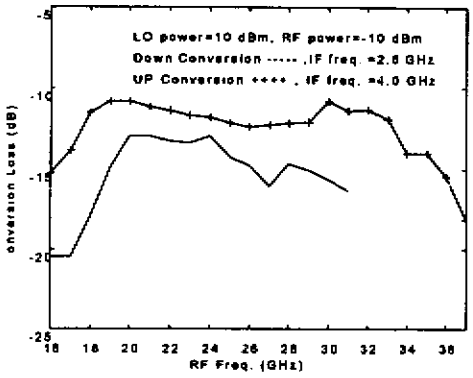

Fig. 6(b) Measured conversion loss of the subharmonically pumped mixer.

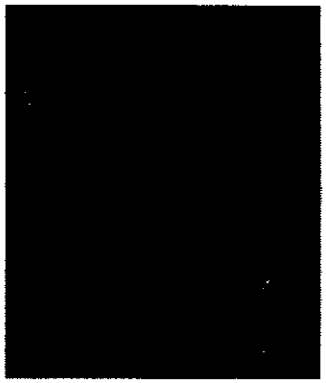

Fig. 7(a) The chip photo of the microstrip- line DA.

Fig. 7(b) The chip photo of the GCPW DA.

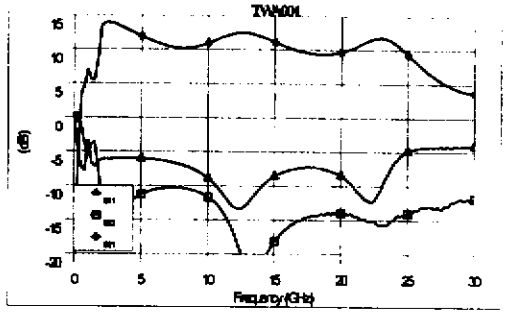

Fig. 7(c) Measured small-signal gain and return loss of microstrip-line DA.

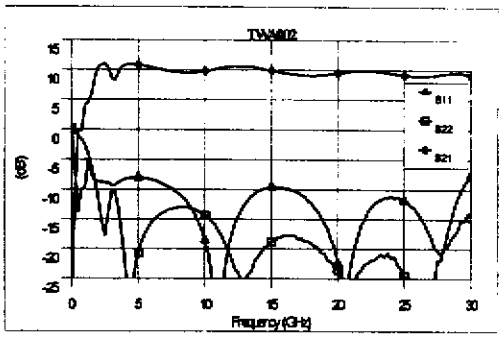

Fig. 7(d) Measured small-signal gain and return loss of GCPW DA.

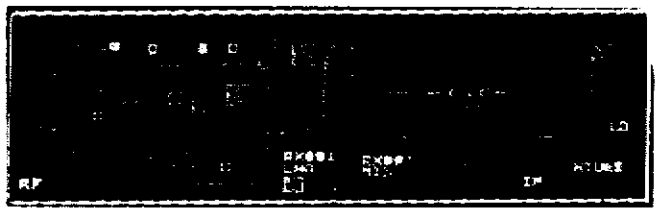

Fig. 8(a) The layout of LNA and mixer.

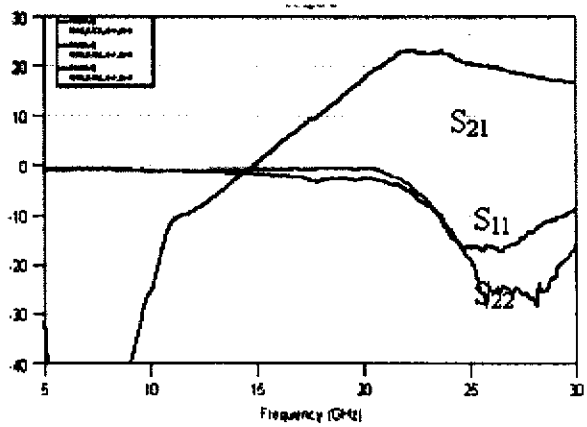

Fig. 8(b) Measured small signal gain and return loss of the LNA.

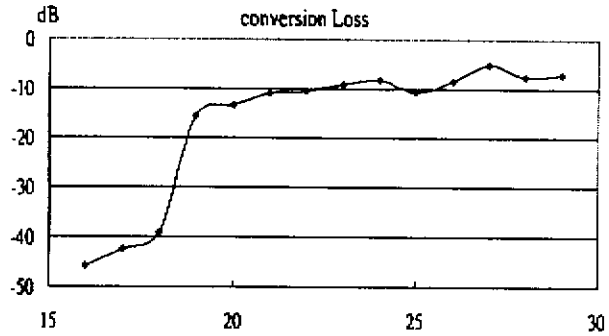

Fig. 8(c) Measured conversion loss of the mixer of the module.

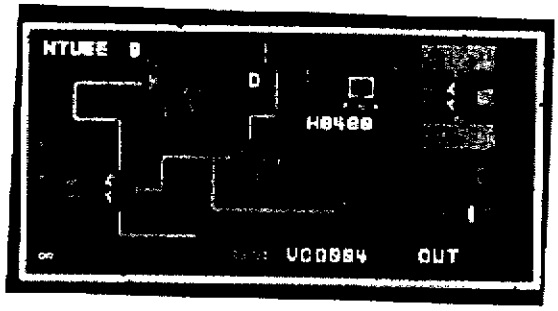

Fig. 9(b) The photo of the DRO chip.

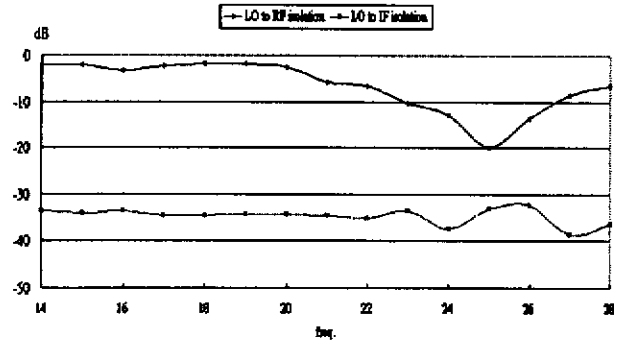

Fig. 8(d) Measured LO to RF isolation and LO to IF isolation of the mixer of the module.

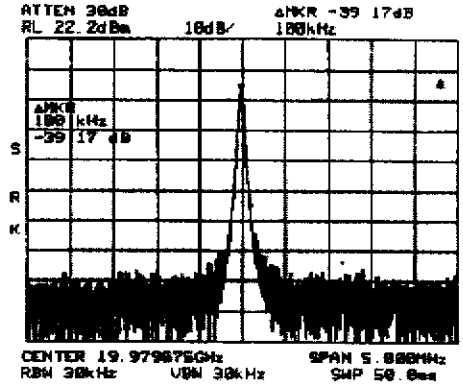

Fig. 9(c) Measured result in Spectrum analyzer of the DRO module.

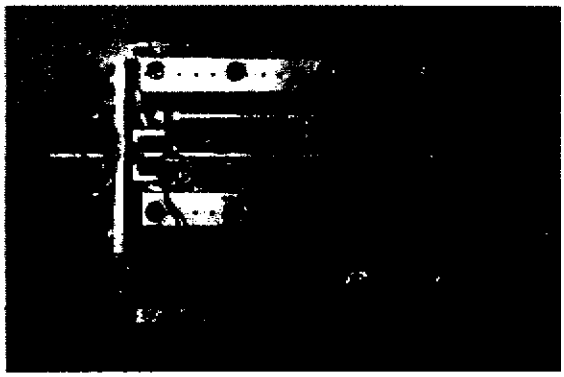

Fig. 9(a) The photo of the DRO module.