Performance Enhancement of Ring Oscillators and Transimpedance Amplifiers by Package Strain

Feng Yuan, *Student Member, IEEE*, Ching-Fang Huang, *Student Member, IEEE*,
Ming-Hsin Yu, and Chee Wee Liu, *Senior Member, IEEE*

***Abstract*—The appropriate external stress can enhance a device and circuit performance. The 7.4% speed enhancement is achieved for the 250-nm node ring oscillator under uniaxial tensile strain for a mutually perpendicular layout of the NFET and the PFET. The speed enhancement is less than 1.5% for the conventional parallel layout of the NFET and the PFET. A 180-nm node transimpedance amplifier has a $\sim 5\%$ bandwidth enhancement using a biaxial tensile strain or a uniaxial tensile strain parallel to the NFET channel to tune the peaking frequency of active inductor in the circuit. The package strain can provide an extra useful parameter for the future digital and analog circuit design.**

***Index Terms*—Layout direction, mechanical strain, package strain, ring oscillator, strain, transimpedance amplifier (TIA).**

I. Introduction

THE SCALING down of the MOSFET increases the circuit performance rapidly in the last decade. The circuit performance from one generation to another not only needs complicate-process improvement, but also requires the new design of circuitry to fully take advantage of the new processing technologies. The strained Si is the production technology to enhance the device speed. The process strain obtained by the silicon nitride cap, silicide, and SiGe source/drain is now used in the production of a 90-nm node for CPU products [1]–[3]. The process strain providing the uniaxial strain has the advantage of simplicity and low cost. However, the process strain only can be applied in small devices, and the strain advantage diminishes in the large devices such as a 180 or a 250-nm node. The strain introduced in the process is much smaller (approximately one third) as compared to the substrate strain [4], [5], which is induced by the SiGe buffer layers underneath the silicon circuitry. The substrate strain provides a large biaxial strain but suffers the thermal budget, threading defects, and the high cost. It is still a long way to go for the substrate strain to be used in the production. Alternatively, the strain on the Si channel can be induced by bending the Si wafer directly (mechanical strain) [6] or bending a package substrate with Si chip glued firmly on its surface (package strain) [7], [8]. Both substrate strain from the misfit and mechanical/package strain produce the global strain that imposes the similar strain condition on the NFET and the PFET. The enhanced device performance is achieved on the MOSFET devices under the mechanical/package strain [7], [8]. The package strain is also found to have no inferior effect on the Al/oxide and Cu/low-k interconnects in our experiments. Note that the process strain can provide the uniaxial strain, while the substrate strain gives the biaxial strain. However, the package strain has the flexibility to give uniaxial strain or biaxial strain to the circuitry depending on the stress mechanism. The speed enhancement of ring oscillator is 10%–20% under the biaxial tensile strain induced by the SiGe buffer layer [5], and 5%–10% under the process strain [3]. The strain level of the substrate strain is larger than the package strain, but the circuit performance cannot be optimized from the substrate strain. The package strain can be applied after the process and further enhance the circuit performance after the circuit fabrication. The package strain can also be applied on the substrate strain or process-strain devices and provides the extra performance enhancement [8]. The low-cost, flexibility, and modular properties make the package strain attractive for future production. The review of mobility enhancement technologies can be found in [9].

In this paper, the optimal layout of the CMOS is reported to increase the ring oscillator speed under the package strain. The transimpedance amplifier (TIA) is also designed to have a bandwidth enhancement under the package strain by tuning the inductive peaking frequency of an active inductor.

II. Experiment

A 43-stage ring oscillator with an Al interconnect is fabricated using a conventional 250-nm process with $f_T \sim 35$ GHz. A TIA is also fabricated using a 180-nm process with $f_T \sim 50$ GHz. Fig. 1 shows the schematic diagram of the setup to provide the package strain. The die (~ 1 mm^2) of the test circuit is tightly glued on the Si wafer/strip as the package substrate. The mechanical stress is applied to the package substrate, and the chip die is stressed via the glue between the chip and the package substrate. The glue must be properly selected to bond the chip and the package substrate tightly, and allow the stress to propagate into the chips from the package substrate. The bad glue degrades the strain level of the chip die. The uniform mechanical displacement at the centerline is applied on the Si strip to introduce the uniaxial strain (Fig. 1). For the biaxial strain, the die is also glued on the center of a 100-mm diameter Si wafer with a mechanical displacement at the center (Fig. 1). Note that to apply a compressive strain, the chip has to be located near the center on the same side of the mechanical displacement (Fig. 1).

Manuscript received October 13, 2005; revised January 18, 2006. The work done by the National Taiwan University group was supported by the National Science Council, Taiwan, R.O.C., under Contract NSC-94-2215-E-002-040. The review of this paper was arranged by Editor V. R. Rao.

The authors are with the Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei 106, Taiwan, R.O.C. (e-mail: chee@cc.ee.ntu.edu.tw).

Digital Object Identifier 10.1109/TED.2006.870568

0018-9383/$20.00 © 2006 IEEE

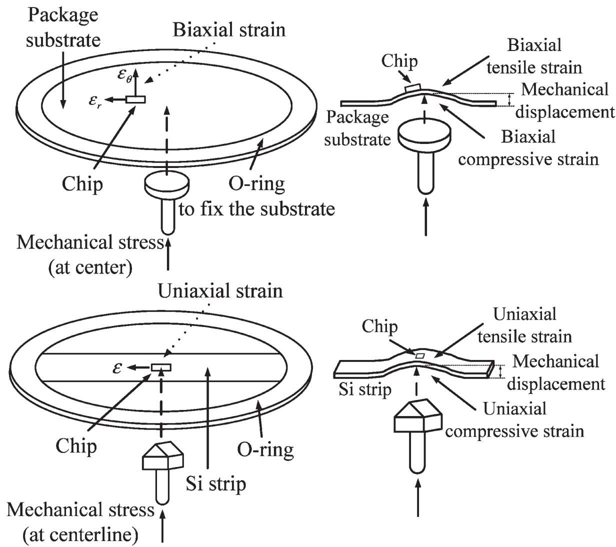


Fig. 1. Schematic diagram of the externally applied biaxial and uniaxial package strain. The glue between devices and package substrates is selected to allow the stress to propagate into the chips from the package substrate.

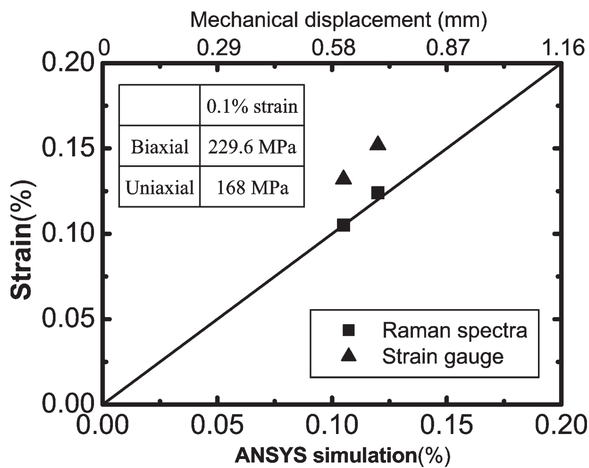


Fig. 2. Strain measured by Raman spectra, strain gauge and simulated by finite element analysis tool (ANSYS). There is a good agreement between the simulation and the measurement.

The strain at a different mechanical displacement can be obtained from the Raman spectra of bended Si substrates [10]. The strain gauge [11] and the finite element simulation by ANSYS are also used to investigate the strain on the package substrate. There is a good agreement between the simulation and the measurement for the biaxial tensile strain generated by the central displacement (Fig. 2). Then, other strain conditions in this paper are analyzed by the ANSYS simulation. The relationships between the percentage notation of the strain level and the actual value of strain are also shown in Fig. 2 [12].

To avoid the measurement error caused by the process variation, the strain effect is measured on the same chip with and without the strain application. The external strain is also small enough ($\leq 0.065\%$ in our experimental setup) to avoid the possible damage. The electrical characteristics after removing the strain have no change to ensure no damage of the devices.

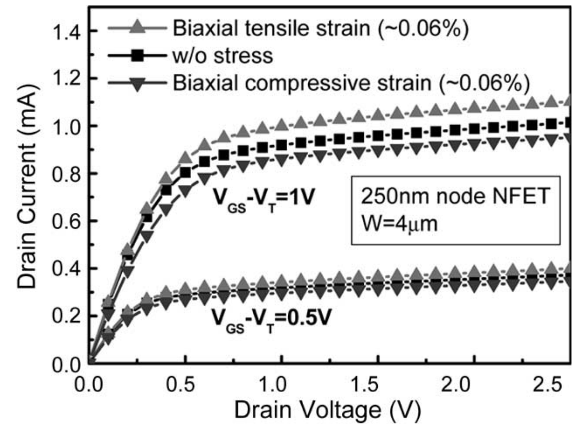


Fig. 3. Output characteristics of a 250-nm node NFET under the biaxial strain.

III. MOSFET Device

The mobility change of a single MOSFET device under the package strain was reported previously [7], [8], [13]. The electron mobility of the NFET can be enhanced by the biaxial tensile strain. The output characteristics of a 250-nm node NFET device under a 0.06% biaxial package strain are also shown in Fig. 3. The drive current of the NFET is enhanced/decreased under the biaxial tensile/compressive package strain. Therefore, the biaxial tensile strain induced by the SiGe buffer layer (substrate strain) is the effective way to enhance the electron mobility of the NFET. However, the biaxial compressive strain has nearly no effect on the hole mobility of the PFET at a high vertical electric field. The width mismatch on the PFET and the NFET increases under substrate strain. The uniaxial strain is proved to have enhancements on both electron mobility of the NFET and hole mobility of the PFET [1]. The significant improvement of the hole mobility under the uniaxial strain at a high vertical electric field is due to the separation between the light hole and heavy hole bands. The strength and direction of the uniaxial strain can be tuned in the process flow to have both the mobility enhancements on the NFET and the PFET [1]. Table I shows the current enhancement of the single NFET and PFET device biased at the saturation region under the 0.06% package strain. The widths of the NFET and the PFET are 4 and 10 μm, respectively. The biaxial strain has nearly no effect on the hole mobility of the PFET, similar to [8] and [13]. For the NFET, the uniaxial tensile strain parallel to the channel and biaxial tensile strain can give a significant improvement. For the PFET, both the uniaxial compressive strain parallel to the channel and the uniaxial tensile strain perpendicular to the channel give reasonable enhancement.

IV. Ring Oscillator

Two kinds of inverter cell layout, 1) p-channel perpendicular to n-channel (perpendicular layout) and 2) p-channel parallel to n-channel (parallel layout), are studied. The widths of the NFET and the PFET are 4 and 10 μm, respectively, for each stage and the output buffer of the ring oscillator. The gate length is 240 nm. The output waveform was measured by a TDS3052 oscilloscope. The oscillation frequency of the 43-stage ring oscillator biased at $V_{dd} = 2.5$ V is ~ 270 MHz for

TABLE I
CHANGE OF SATURATION CURRENT FOR THE 250-nm NODE MOSFET DEVICES. THERE IS AN ENHANCEMENT UNDER THE TENSILE STRAIN FOR THE NFET. UNDER THE UNIAXIAL COMPRESSIVE STRAIN PARALLEL TO CHANNEL AND THE UNIAXIAL TENSILE STRAIN PERPENDICULAR TO CHANNEL, THE PFET IS ENHANCED

Current change (%) At $\lvert V_{GS}\rvert - \lvert V_T\rvert = 1V$		250 nm node (L_G = 240 nm) Compressive 0.06% strain	250 nm node (L_G = 240 nm) Tensile 0.06% strain
NFET	Uniaxial // channel	-4.3	10.8
	Uniaxial ⊥ channel	-6.9	2.5
	Biaxial	-6.2	8.7
PFET	Uniaxial // channel	5.5	-8.8
	Uniaxial ⊥ channel	-6.8	4.8
	Biaxial	0.3	-0.9

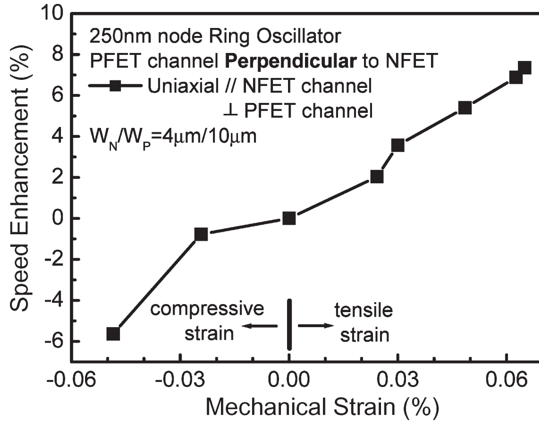


Fig. 4. Measured speed enhancement of the 250-nm node ring oscillator with the perpendicular channel layout under various package strains.

both the perpendicular and parallel layout. Fig. 4 shows the measured speed enhancement of the ring oscillator with the perpendicular layout under various package strain conditions. The speed enhancement is found to be ~ 7.4% under a 0.065% uniaxial tensile strain with the direction parallel to NFET channel and perpendicular to PFET channel. The significant speed enhancement under uniaxial tensile strain parallel to the NFET channel and perpendicular to the PFET channel in the perpendicular layout is due to the large current enhancement for both the NFET and the PFET (Table I). The speed enhancement of the ring oscillator with the parallel layout under various package strain conditions is less than 1.5% (Fig. 5), since no simultaneous significant enhancement of the NFET and the PFET can be obtained in the parallel layout (Table I). As a result, the perpendicular layout is the most effective to enhance the speed of the circuit.

The simulated and measured single-stage delay time of the perpendicular layout circuit at a different voltage supply is shown in Fig. 6. The speed enhancement is nearly independent to the supply voltage. The simulation using the enhanced drive current of each device agrees very well with the experimental data. This result indicates that the package strain can be applied at any bias conditions and is adequate to digital applications, if the layout is properly considered (perpendicular layout).

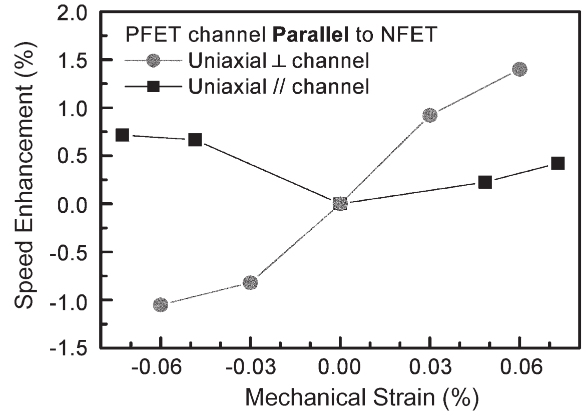


Fig. 5. Measured speed enhancement of the 250-nm node ring oscillator with the parallel channel layout under various package strains. The enhancement is relatively small as compared to perpendicular channel layout due to less current improvement or current degradation of the NFET or the PFET.

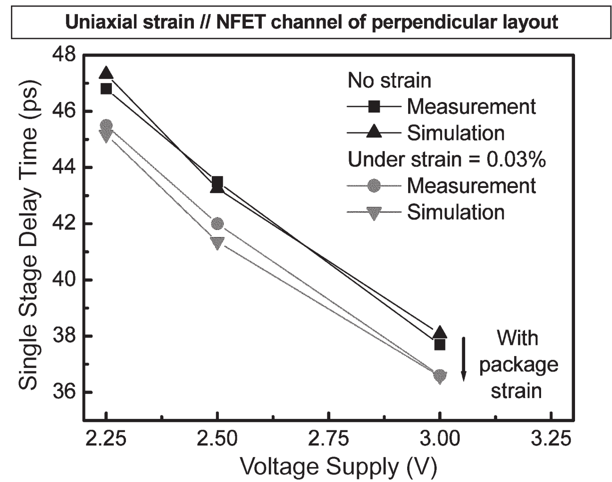


Fig. 6. Simulated and measured single-stage delay time of the perpendicular layout ring oscillator under different voltage supply. The speed enhancement is nearly independent to the voltage supply.

The devices with a 90-nm process was also fabricated and tested under the package strain. The traditional parallel layout ring oscillator under the biaxial tensile strain has a 2.3% speed

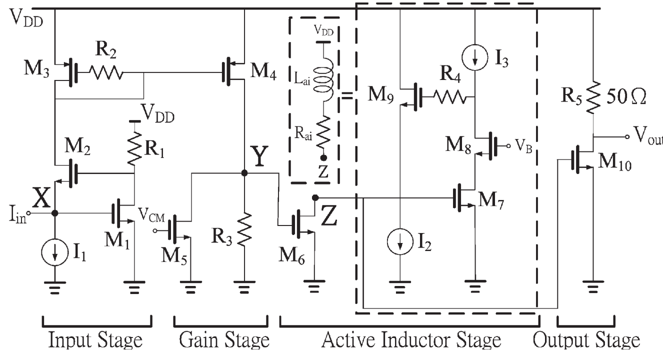


Fig. 7. Circuit diagram of the 180-nm node TIA. The active-inductor stage can be simplified as a series of resistor $R_{\rm ai}$ and inductor $L_{\rm ai}$.

enhancement. However, we have no perpendicular layout ring oscillator with a 90-nm process. For 250-nm devices, the package strain has the advantage to increase the speed of an IC with a 250-nm node without any process modification.

Note that the extra area of the perpendicular layout in CMOS circuit can be minimized by combining two inverters.

V. Transimpedance Amplifier (TIA)

The TIA is a basic analog component widely used in optical-communication circuit, which consists of a photodiode, a TIA, a limiting amplifier (LA), a clock and data recovery, and a digital base band. The main propose of a TIA circuit is to transfer a photocurrent signal from a photodiode into a voltage signal, and an LA amplifies this small voltage signal to the large signal with a square-wave-like waveform. The bandwidth of the whole optical-communication circuit is usually limited by the TIA bandwidth and photodiode capacitance. The TIA circuit design to have a large bandwidth and to minimize the effect of the photodiode capacitance is crucial for the optical-communication circuit.

A TIA [14], [15] circuit (Fig. 7) is fabricated with the bandwidth $\sim$ 3.4 GHz. There are four stages in our TIA circuit (Fig. 7). The bandwidth of the TIA circuit is enhanced by the active-inductor load. The current change of each transistor is dependent on the NFET, the PFET, the direction of the external stress, and the layout of the transistor. The TIA circuit should be carefully designed to respond the effect of the external package strain. Therefore, the bandwidth of our TIA circuit under the package strain is dependent on the NFET of active-inductor stage only. The detailed circuit design of the TIA is described as follows.

As shown in Fig. 7, a regulated-cascode stage is used as the input stage to minimize the input resistance. Since the capacitance of photodiode at input node X is usually much larger than the capacitance of the transistors, the primary effort is to minimize the input resistance of the transistor at node X. The bandwidth of the input stage is dominated by the pole to the input node X, with the pole frequency [16]–[18]

$$\omega_X \approx \frac{C_{\rm in}}{g_{m2}\left(1+g_{m1}R_1\right)} \tag{1}$$

where g_m is the transconductance. $C_{\rm in}$ is the capacitance of the photodiode, which is in the range of 0.1–1 pF, and the parasitic capacitance of the transistor M_1, and M_2 can be neglected. The regulated-cascode stage is an extension of the common-gate stage, but further reduces the input resistance by a factor of $(1+g_{m1}R_1)$ and enhances the bandwidth of the input stage accordingly.

The gain stage is a simple common-source stage. The bandwidth of this stage is dominant by the pole to the node Y, and the pole frequency can be written as [16], [17]

$$\omega_Y \approx [R_3(C_{\rm gd4}+C_{\rm gd5}+C_{\rm gs6})]^{-1} \tag{2}$$

where $C_{\rm gs}$ and $C_{\rm gd}$ are the gate-source and gate-drain capacitance, respectively. The package strain presumably has a small effect on the poly-Si resistor [19]. In our experimental setup, the externally package strain is less than 0.065%, thus the area change of the capacitance is less than 0.13%, insignificant to the pole frequency. Therefore, the pole frequency to node Y and the bandwidth of the gain stage have no change under the package strain.

The output stage is a simple common-source stage with 50 Ω loading resistor and has a very large bandwidth, which can be neglected in considering the bandwidth change of the TIA circuit under the package strain.

The active-inductor stage is a common-source stage with the NFET active inductor, and has a nearly unity gain at low frequency. The active-inductor stage can be simplified as a series of resistor $R_{\rm ai}$ and inductor $L_{\rm ai}$ on Z (Fig. 7)

$$R_{\rm ai} \approx \frac{1}{g_{m7}g_{m9}r_{o7}} \tag{3}$$

$$L_{\rm ai} \approx \frac{C_{\rm gs9}}{g_{m7}g_{m9}}. \tag{4}$$

Its transfer function is [20]

$$\frac{V_Z}{V_Y} \approx -g_{m6}R_{\rm ai}\frac{\omega_n}{2\zeta}\frac{s+2\zeta\omega_n}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{5}$$

$$\omega_n \approx \frac{1}{\sqrt{L_{\rm ai}(C_{\rm gd6}+C_{\rm gs10})}} \tag{6}$$

$$\zeta \approx \frac{R_{\rm ai}}{2}\sqrt{\frac{C_{\rm gd6}+C_{\rm gs10}}{L_{\rm ai}}} \tag{7}$$

where r_{o7} is the output resistance of M_7, and ζ is the damping factor. The damping factor is $\sim$ 0.5 in our circuit. The large damping factor would cause the unstable oscillation of the circuit. The inductive peaking frequency ($\omega_{L\rm pk}$) can be derived from [20]

$$\omega_{L\rm pk} = \left(\sqrt{\sqrt{1+8\zeta^2}-4\zeta^2}\right)\omega_n, \qquad \zeta < \frac{1}{\sqrt{2}}. \tag{8}$$

The capacitance of each transistor presumably has no change under external package strain [19]. Since the percentage decrement of r_o is almost the same as the percentage enhancement of g_m, the $g_{m7}r_{o7}$ is almost constant the under biaxial tensile strain in (3). Therefore, the ω_n is proportional to $\sqrt{g_{m7}g_{m9}}$,

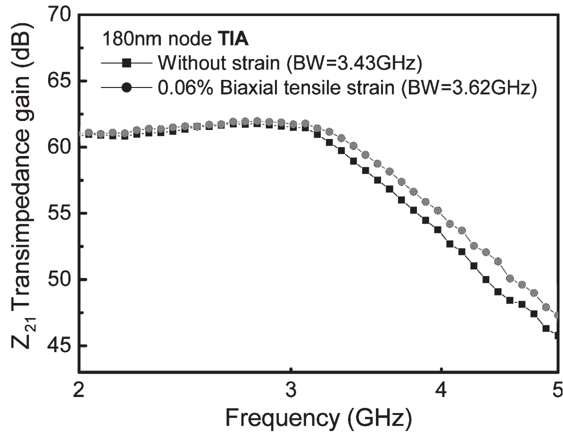


Fig. 8. Measured bandwidth enhancement of the 180-nm node TIA under the biaxial tensile strain.

TABLE II
BANDWIDTH ENHANCEMENT OF THE TIA CIRCUIT WITH A 180-nm NODE CMOS PROCESS UNDER VARIOUS PACKAGE STRAIN CONDITIONS

Bandwidth enhancement (%)	0.06% tensile strain	
	Experiment	Simulation
Uniaxial // channel	5.0	6.3
Uniaxial ⊥ channel	1.6	2.2
Biaxial	5.5	5.2

the ζ is proportional to $(\sqrt{g_{m9}})^{-1}$, and the prefactor of (8) increases as ζ decreases. The enhancement of g_{m7} and g_{m9} cause the $\omega_{L\text{pk}}$ increases. The enhanced transconductance of the NFET can be obtained under biaxial tensile strain and uniaxial tensile strain parallel to the NFET channel. Then, the inductive peaking frequency $\omega_{L\text{pk}}$ increases accordingly.

Therefore, the bandwidth of the TIA circuit is determined by the peaking frequency of the active inductor, since the input stage is designed to have $\sim 3\times$ bandwidth of gain stage, and the bandwidth of gain stage is independent of the package strain. There is $\sim$ 5% bandwidth enhancement of the TIA circuit under a 0.06% biaxial tensile strain in the frequency response (Fig. 8). Table II gives the bandwidth enhancement of TIA circuit under various package strain conditions. There is also a $\sim$ 5% bandwidth enhancement of TIA circuit under uniaxial tensile strain parallel to the NFET channel. The uniaxial tensile strain perpendicular to the NFET channel has the minimum enhancement, consistent with simulation results.

VI. CONCLUSION

The interaction between the circuit design and the package strain is studied. It is demonstrated for the first time that there is a 7.4% speed enhancement of the ring oscillator with the PFET channel perpendicular to the NFET channel under the uniaxial tensile strain parallel to the NFET channel. There is also a $\sim$ 5% bandwidth enhancement of the TIA circuit using the biaxial tensile strain and the uniaxial tensile strain parallel to the NFET channel. The optimal layout for a digital circuits and only the NFET design for analog circuits are demonstrated. These design techniques with package strain give the low cost and the reasonable performance enhancement on both digital and analog circuitry, suggesting a new trend for future circuit design.

ACKNOWLEDGMENT

The authors would like to thank Prof. S. T. Chang, National Chung Hsing University, Taiwan, R.O.C. for helpful discussion and the Chip Implementation Center (CIC), Taiwan, R.O.C., for fabricating the chips.

REFERENCES

[1] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors," in *IEDM Tech. Dig.*, Washington, DC, 2003, pp. 978–991.

[2] K. Rim, "Strained Si surface channel MOSFETs for high-performance CMOS technology," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, San Francisco, CA, 2001, pp. 116–117.

[3] C.-H. Ge, C.-C. Lin, C.-H. Ko, C.-C. Huang, Y.-C. Huang, B.-W. Chan, B.-C. Perng, C.-C. Sheu, P.-Y. Tsai, L.-G. Yao, C.-L. Wu, T.-L. Lee, C.-J. Chen, C.-T. Wang, S.-C. Lin, Y.-C. Yeo, and C. Hu, "Process-strained Si (PSS) CMOS technology featuring 3D strain engineering," in *IEDM Tech. Dig.*, Washington, DC, 2003, pp. 73–76.

[4] J. L. Hoyt, H. M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E. A. Fitzgerald, and D. A. Antoniadis, "Strained silicon MOSFET technology," in *IEDM Tech. Dig.*, San Francisco, CA, 2002, pp. 23–26.

[5] J. R. Hwang, J. H. Ho, S. M. Ting, T. P. Chen, Y.-S. Hsien, C. C. Huang, Y. Y. Chiang, H. K. Kee, A. Liu, T. M. Shen, G. Braithwaite, M. Currie, N. Gerrish, R. Hammond, A. Lochtefeld, F. Singaporewala, M. Bulsara, Q. Xiang, M. R. Lin, W. T. Shiau, Y. T. Loh, J. K. Chen, S. C. Chien, and F. Wen, "Performance of 70 nm strained-silicon CMOS devices," in *VLSI Symp. Tech. Dig.*, San Francisco, CA, 2003, pp. 103–104.

[6] A. Lochtefeld and D. A. Antoniadis, "Investigating the relationship between electron mobility and velocity in deeply scaled NMOS via mechanical stress," *IEEE Electron Device Lett.*, vol. 22, no. 12, pp. 591–593, Dec. 2001.

[7] S. Maikap, C.-Y. Yu, S.-R. Jan, M. H. Lee, and C. W. Liu, "Mechanically strained strained-Si NMOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 1, pp. 40–42, Jan. 2004.

[8] S. Maikap, M. H. Liao, F. Yuan, M. H. Lee, C.-F. Huang, S. T. Chang, and C. W. Liu, "Package-strain-enhanced device and circuit performance," in *IEDM Tech. Dig.*, San Francisco, CA, 2004, pp. 233–236.

[9] C. W. Liu, S. Maikap, and C.-Y. Yu, "Mobility-enhancement technologies," *IEEE Circuits Devices Mag.*, vol. 21, no. 3, pp. 21–36, May/Jun. 2005.

[10] M. H. Liao, M. J. Chen, T. C. Chen, P. L. Wang, and C. W. Liu, "Electroluminescence from metal/oxide/strained-Si tunneling diodes," *Appl. Phys. Lett.*, vol. 86, no. 22, p. 223502, May 2005.

[11] Y. G. Wang, D. B. Scott, J. Wu, J. L. Waller, J. Hu, K. Liu, and V. Ukraintsev, "Effects of uniaxial mechanical stress on drive current of 0.13 μm MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 529–531, Feb. 2003.

[12] M. Madou, *Fundamentals of Microfabrication*. Boca Raton, FL: CRC Press, 1997, pp. 145–163.

[13] M. H. Liao, S. T. Chang, M. H. Lee, S. Maikap, and C. W. Liu, "Abnormal hole mobility of biaxial strained-Si," *J. Appl. Phys.*, vol. 98, no. 6, p. 066104, Sep. 2005.

[14] J. Lee, S.-J. Song, S. M. Park, C.-M. Nam, Y.-S. Kwon, and H.-J. Yoo, "A multiple on oxide of 1 Gb/s 80 dB fully-differential CMOS transimpedance amplifier for optical interconnect applications," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, San Francisco, CA, 2002, pp. 447–448.

[15] B. Razavi, "A 622 Mb/s 4.5 pA/$\sqrt{\text{Hz}}$ CMOS transimpedance amplifier," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, San Francisco, CA, 2002, pp. 162–163.

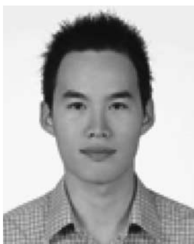
[16] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 4th ed. New York: Oxford Univ. Press, 1998, p. 393. 432–434, 1112–1113.

[17] B. Razavi, *Design of Integrated Circuits for Optical Communications*. Boston, MA: McGraw-Hill, 2003, pp. 110–112.

[18] S. M. Park and C. Toumazou, "Low noise current-mode CMOS transimpedance amplifier for giga-bit optical communication," in *Proc. IEEE Int. Symp. Circuits and Systems*, Monterey, CA, Jun. 1998, vol. 1, pp. 293–296.
[19] F. Yuan, S.-R. Jan, S. Maikap, Y.-H. Liu, C.-S. Liang, and C. W. Liu, "Mechanically strained Si-SiGe HBTs," *IEEE Electron Device Lett.,* vol. 25, no. 7, pp. 483–485, Jul. 2004.
[20] A. Bruce Carlson, *Circuits : Engineering Concepts and Analysis of Linear Electric Circuits*. Pacific Grove, CA: Brooks/Cole, 2000, pp. 476–511.

Feng Yuan (S'01) received the B.S. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, R.O.C., in 2001. He is currently working towards the Ph.D. degree in the Department of Electrical Engineering and Graduate Institute of Electronics Engineering, NTU.

As a graduate student, he has coauthored a number of publications. He also held the first Semiconductor Research Corporation international fellowship in 2004. His current research interests include strained Si devices, SiGe HBT, and their circuit application.



Ching-Fang Huang (S'06) received the B.S. degree in mechanical engineering from National Taiwan University (NTU), Taipei, Taiwan, R.O.C., in 2003. He is currently working toward the Ph.D. degree in the Department of Electrical Engineering and Graduate Institute of Electronics Engineering, NTU.

His current research interests include mechanical strained MOSFETs and speed enhancement of thin film transistors.

Ming-Hsin Yu received the B.S. degree in electrical engineering from the National Cheng-Kung University, Tainan, Taiwan, in 2003, and the M.S. degree from the Graduate Institute of Electronics Engineering, NTU, Taipei, Taiwan, in 2005.

He is currently with Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, Taiwan, as a Circuit Design Engineer. His research interests include strained Si devices and circuits of optical communication.

Chee Wee Liu (M'99–SM'00) received the B.S. and M.S. degrees in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 1985 and 1987, respectively, and the Ph.D. degree in electrical engineering from Princeton University, Princeton, NJ, in 1994.

He is currrently a Professor at NTU. His current research interests include strained Si, CMOS optoelectronics, SiGe high-speed devices, high-k, and metal gate. He invented the first MOS tunneling light emitting diode and photodetector, and has two patents on photodetectors.