A 100-Kbps Power-Line Modem for Household Applications

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Abstract

Communication using power line as a medium provides a convenient and inexpensive way for data transmission and control signaling in the households. In this paper we will introduce a power-line channel model as well as architecture of a spread-spectrum baseband transceiver IC for a power-line modem. The modulation and spreading scheme used in the proposed transceiver is MBOK. This transceiver runs at the carrier frequency of 256 kHz and provides 100 Kbps data rate. Simulation results verify the effectiveness of the proposed architecture in household data communication.

Introduction

Electric power line, which can be found in most buildings, naturally exhibits its potential as a convenient and cheap communication medium. A reliable intra-building communication network based on power line will serve as the most suitable infrastructure for home and office automation. Although some power-line communication systems have already been built and tested, their data rate are usually low and complexity too high for home automation applications [1-3]. Therefore we are motivated to develop a power-line communication modem for both control signaling and data transmission in households. The modem should provide at least 100 Kbps data rate with a BER less than 10^{-6} in the frequency band from 10 kHz up to 450 kHz as specified by the FCC [3].

Power-Line Channel Model

Originally designed for power delivery instead of signal transmission, power line channel possesses non-ideal communication properties, including time- and frequency-varying attenuation and sudden change of channel characteristics. In addition, various inimical noises, such as impulse noise and continuous-wave noise produced by electric loads, and large background noise, are also present in the channel [4-6].

Taking all these effects into consideration, we established a power-line channel model for system simulation and performance evaluation. Its block diagram is shown in Fig. 1. The channel filter receives baseband transmission signal and outputs the corresponding channel-filtered passband signals. The channel-filtered signals are derived from SPICE transient analysis by sampling the responses of a power-line equivalent circuit with perfect transmission signal as input.

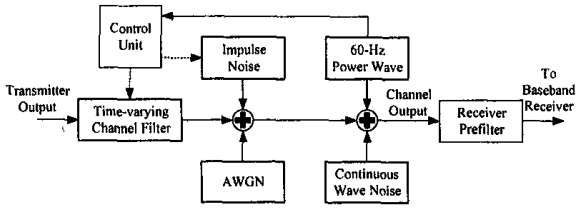

Fig. 1 Block diagram of the power line channel model.

The power-line equivalent circuit is constructed using a second order RC low-pass transmit filter, RLC models of some electric apparatus introduced in [7], and models of power-line wiring. The channel filter accounts for the effects of signal attenuation, distortion, and fading in the channel.

The AWGN, impulse noises, continuous-wave noises, and the 60-Hz power wave are also generated and added to the signal. Besides, in order to effectively simulate the 120-Hz fading phenomenon and higher occurrence probability of impulse noises near the peaks of power wave, a control unit monitors the voltage of power wave; when power wave reaches its peaks, the control unit changes the set of signal samples used in the channel filter and dynamically increase the occurrence probability parameter in the impulse noise generator. Finally the signal and noises pass through a digital FIR filter representing receiver filter in the analog front end. During simulation, the parameters of this channel model, e.g. power spectral density of AWGN, power of continuous-wave noises, and occurrence probability of impulse noises, are set according to the measured values in [4-7].

Baseband Transceiver Structure

As shown in Fig. 2, a power-line communication system basically consists of a transmitter, the power-line channel, and a receiver. In this paper, we focus on the design and implementation of the baseband receiver and transmitter.

A. Modulation Scheme and Transmitter Architecture

Modern spread-spectrum techniques are adopted to combat the hostile power-line channel. After examining performances, spectral efficiencies, and hardware complexities of several modulation/spreading schemes, we decided to use the pilot-assisted *M*-ary Bi-Orthogonal Keying (MBOK) scheme.

The principle of MBOK can be explained with the help of Fig. 3, which shows the block diagram of the baseband

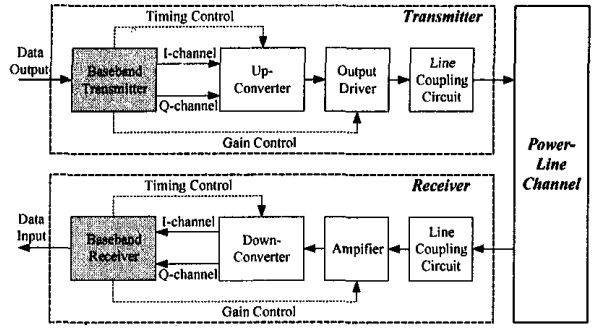

Fig. 2 Block diagram of a power-line communication system.

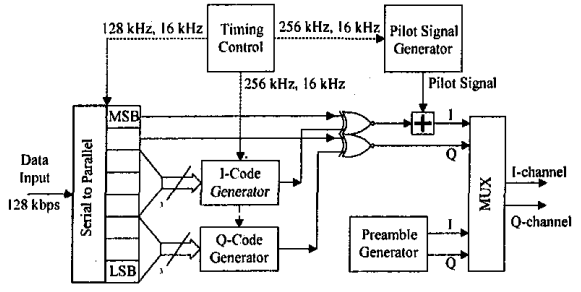

Fig. 3 Block diagram of the baseband transmitter.

transmitter. A data symbol, representing eight data bits, consists of three code sequences transmitted simultaneously: one data code in Q-channel, the other data code and the pilot code, both in I-channel. The data codes transmitted in I- and Q-channel are selected out of a set of eight orthogonal codes, according to two sets of 3-bit in the symbol, respectively. The remaining two bits determine the polarities with which the two data codes are transmitted. The predetermined pilot code sequence is always transmitted in I-channel with positive polarity, and it is orthogonal to all eight possible data codes. The eight data codes plus one pilot code are chosen from 16-bit Walsh codes, and thus are mutually orthogonal.

This scheme adopts a dedicated pilot signal to convey channel information for use by the channel estimator in the receiver. Because the pilot signal is transmitted with the data signal simultaneously through the channel, it suffers from the same distortion and phase change as the data signals. Thus the receiver is able to come up with a very good estimate of the channel. The channel estimation can easily be done through a complex correlator that extracts the phase in the pilot signal.

Obviously, using a dedicated pilot signal decreases power efficiency as well as communication efficiency of the system. The addition of the pilot signal increases transmission power by 1.5 fold, which means a 1.8 dB performance degradation. Nevertheless, we note that this degradation is quite small compared to the dynamic range of channel attenuation, which can be as large as 45 dB [4]. Hence we conclude that it is the channel condition rather than the transmission power level

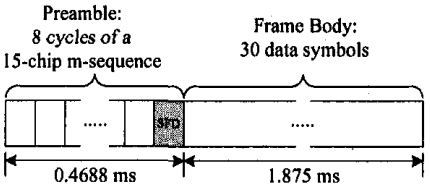

Fig. 4 Data frame structure.

that determines communication quality. This justifies our use of pilot signal for carrier synchronization.

B. Frame Structure and Data Rate Specification

To limit transmission power within the frequency band below 450 kHz, the transceiver is designed to operate at a carrier frequency of 256 kHz and a chip rate of 256 kcps. This gives a symbol rate of 16 Ksymbol/s, and a raw channel data rate of 128 Kbps, since there are 16 chips in a symbol duration and a symbol represents 8 bits of data. However, in order to minimize the effect of sudden change of channel characteristics and lower the probability for a transmitted frame being hit by impulse noises, the frame length is made very short. As shown in Fig. 4, a frame is composed only of 30 data symbols preceded by a preamble consisting of eight cycles of a 15-chip *m*-sequence. The preamble is transmitted in I-channel, and the last cycle of the *m*-sequence, as the Start-of-Frame Delimiter (SFD), has negative polarity while previous seven have positive polarity. After taking the bandwidth occupied by the preamble into consideration, the effective burst data rate reduces to 102.4 kbps.

C. Receiver Structure

At the receiver end, the received passband signal is sampled four times per chip and down-converted to baseband before entering the baseband processor. Fig. 5 shows the basic block diagram of the receiver baseband processor. There are three main functional blocks: the carrier recovery (channel estimation) block, the data detection block, and the timing recovery block.

To demonstrate the operation of demodulation in the receiver, suppose that a transmitter along a power-line send a symbol consisting of the pilot code and the *m*th data code in the I-channel, and the *n*th data code in the Q-channel. The corresponding baseband signal can be written as

$$C_P(t) + P_m \cdot C_m(t) + j \cdot P_n \cdot C_n(t), \qquad (1)$$

where $C_P(t)$ represents the pilot code, and P_m, $C_m(t)$, P_n, $C_n(t)$ are the polarities and codes transmitted in the I- and the Q-channel, respectively. Then assuming that under perfect timing synchronization between the receiver and transmitter in a noiseless situation, the receiver picks up the signal:

$$[\, C_P(t) + P_m \cdot C_m(t) + j \cdot P_n \cdot C_n(t) \,] \cdot e^{j\phi}, \qquad (2)$$

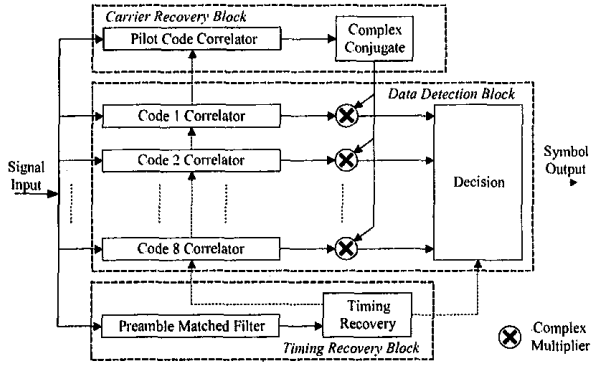

Fig. 5 Block diagram of the baseband receiver.

where ϕ is the total phase shift introduced by the transmit filters, power-line channel, and the receiver filters. This signal then enters eight data code correlators in the data detection block, as well as the pilot code correlator in the carrier recovery (channel estimation) block. After a symbol period, outputs of the mth and the nth data code correlators, and the pilot code correlator are $P_m \cdot e^{j\phi}$, $j \cdot P_n \cdot e^{j\phi}$, and $e^{j\phi}$, respectively. Because the data codes and the pilot code are mutually orthogonal, outputs from all other correlators are zero. The pilot code correlator output $e^{j\phi}$, which estimates the channel phase shift ϕ, will be taken complex conjugate. The result $e^{-j\phi}$ is a reference phase and can be used to compensate for ϕ. Before entering the decision unit, outputs from the eight data code correlators are further multiplied by this reference phase. Thus outputs of the mth and nth complex multipliers becomes P_m and $j \cdot P_n$, while others are still zero. The decision unit will recognize that, among all its inputs, the mth input has the largest magnitude in the real part and the nth input has the largest magnitude in the imaginary part. It can then be decided that the mth code is transmitted in the I-channel and the nth code in the Q-channel. Moreover, the polarities with which they are transmitted, i.e. sgn(P_m) and sgn(P_n), can also be determined.

D. Timing Synchronization and Frame Detection

Because the correlation properties of Walsh codes, which are used as pilot and data codes in MBOK modulation, is different from those of pseudo-noise spreading codes, MBOK is quite sensitive to timing error between the transmitter and the receiver. Timing synchronization is thus crucial to successful operation of this power-line communication system. Another issue arises from the detection of a data frame among various noises in the power-line channel. A robust frame detection mechanism that can provide high detection probability and low false-alarm probability is required.

We note that a data frame consists of 600 chips. Assuming there is a reasonable 100-ppm timing frequency mismatch between the transmitter and the receiver, the timing error in a data frame will accumulate to 0.06 chip, which will not affect system performance very much. Hence there is no need to maintain synchronization during the frame body, if accurate timing alignment has been achieved in the preamble. Timing alignment and frame detection will be done with the help of the preamble in each data frame.

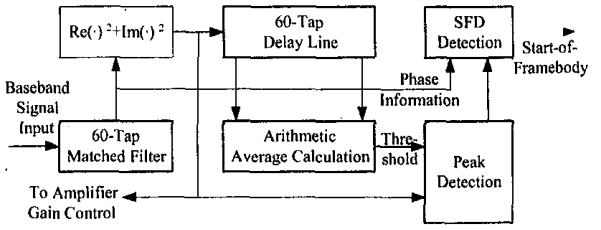

Fig. 6 Architecture of the timing synchronization block.

As shown in Fig. 6, the timing recovery block in the baseband receiver, with a matched filter matched to the m-sequence in the preamble, can detect the presence of a preamble, mark the start of frame body, and achieve accurate timing alignment. The received baseband signal enters the matched filter, and its power calculated. With a period of the m-sequence in the received signals, the matched filter output will have a large peak power; otherwise there will be only noise-like small fluctuations. The power of matched filter output is detected for peak every 15 chips, and the threshold for preamble presence is derived from the average power of the previous matched filter outputs. The SFD detector looks for a train of peaks reappearing every 60 samples (15 chips) and a 180° phase shift in the last peak, and it then issues a signal of frame detection.

Hardware Design and Implementation

Most blocks in the power-line modem baseband receiver, including correlators, preamble matched filter, and timing synchronization circuits, work at the sampling frequency of 1.024 MHz. On the other hand, the complex phase rotation and data decision are executed in symbol rate of 16 kHz. Hence the hardware requirements for speed is relatively loose, while hardware complexity becomes the major concern. In the receiver, operations at symbol rate are done serially instead of in parallel. This greatly reduces the hardware complexity, because one complex multiplier is needed instead of eight and in the decision unit two comparators, one for the real part and one for the imaginary part will suffice.

The baseband transceiver is implemented in gate-level Verilog HDL, and hardware verification is done on a FPGA. Finally a cell-based ASIC implementation of the Verilog code is conducted with a commercially-available automatic place-and-route tool.

Performance Simulation

According to its degree of impairment, we categorize the power-line channel into four scenarios, ranging from a perfect AWGN-only condition to a worst-case one. Fig. 7 shows the simulated BER performance of the proposed power-line modem under these four channel scenarios. Results for BER less than 10^{-4} are not obtained because there are no errors in the 10^7-bit test data when E_b/N_0 is further increased. We note that the performance of this modem under a typical condition is 4 dB worse than that under an AWGN-only channel at a BER of 10^{-4}. This performance degradation is within our design margin and is acceptable.

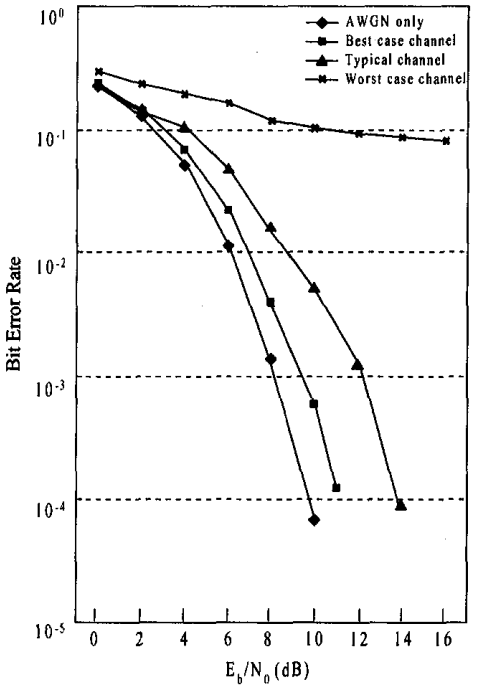

Fig. 7 Baseband transceiver performance simulation results.

Conclusion

With proper design and manipulation, one can use the power line as a communication medium for home automation and communication applications. To this end, a modem providing 100 Kbps data rate over power line is proposed. During the development of this modem, a power-line channel model is constructed for system performance evaluation and functional verification. The modulation scheme and hardware architecture are designed to combat the unfavorable properties of the channel and provide high-quality communication with minimum hardware. We conclude that this pilot-assisted MBOK modem is efficient and viable for power line communication purpose.

Refereces

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