Design and Optimization of MOSFET–Capacitor Filters Using CMOS Current Conveyors

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Abstract

A new CMOS current conveyor is proposed and a MOSFET–capacitor integrator consisting of the CMOS current conveyor, MOSFETs biased in the triode region, and capacitors, and a unity–gain buffer is presented. Based on this integrator high frequency integrated filters can be constructed. However, the design of such filters is complicated by the fact that the effective mobility of each device may vary and the basic building blocks (i.e. operational amplifiers or CMOS current conveyors) are not ideal. We have developed an optimization program to automate the design of this kind of filters. The program iteratively adjusts the W/L ratios and capacitance values through interfacing with SPICE to achieve the desired filtering performance. Simulation results on a six–order bandpass ladder filter with center frequency at 460KHz, 0.5dB ripple in the passband, and a bandwidth of 120KHz is presented.

I. Introduction

The continuous–time integrated filter techniques have recently received considerable attention, because many difficult procedures such as A/D and D/A conversion (for digital filters) and anti–aliasing (for switched–capacitor filters) can be eliminated. In certain mixed analog/digital applications, it has been demonstrated that the continuous–time filter may offer advantages over other types of integrated filters such as switched–capacitor filters and digital filters in certain applications[1][2]. However, conventional operational amplifier (OP AMP) based filters require an amplifier with an open loop gain of several thousands in order to obtain acceptable performance. This will invariantly limit the upper operation frequency of these filters because of the finite gain–bandwidth product of the OP AMPs. On the other hand, various current mode techniques[3], which have been proposed recently, offe. a number of advantages over the traditional voltage–based counterparts from the point of view of bandwidth and performance accuracy at high frequency.

In this paper, we investigate the use of MOS transistors (as voltage–controlled resistors) and a second–generation current conveyor (CCII+) (for its improved high frequency characteristics) in the design and optimization of the high frequency continuous–time filters.

II. Circuit Description

A CMOS CCII+, shown in Fig. 1, consists of a voltage–to–current converter (or an unity–gain amplifier) and current mirrors. Let the current in the three identical constant current sources consisting of MOSFET's (M7,8) (M13,15) and (M14,16), respectively, be I_B. When there is a small current i_x flowing out of Terminal X, the current mirror M9–10 will force a current $I_B - i_x$ through M11 and M12. Consequently, an identical current i_x will flow out of Terminal Z. If the CCII+ is ideal ($i_y=0$, $V_x=V_y$, $i_x=i_z$), the proposed integrator can be constructed as shown in Fig. 2.

For an NMOS FET biased in the triode region, the channel current I_D is given in terms of several basic MOSFET parameters as[4]

$$I_D = F(V_D,V_G) - F(V_S,V_G) \qquad (1)$$

where $F(V_X,V_G) = 2K(V_G - V_B - V_{FB} - \varphi_B)V_X - K(V_X - V_B)^2 - \frac{4}{3}K\gamma(V_X - V_B + \varphi_B)^{2/3}$

$$K = \frac{W}{2L}\mu C_{ox}$$

$$\gamma = \frac{1}{C_{ox}}(2qN_A\epsilon_s)^{1/2}$$

Czarnul[5] has showed that the MOS resistive circuit (MRC), shown in Fig. 2, can completely cancel the even and odd MOS nonlinearities. It is assumed that the transistors of MRC have the same aspect ratios W/L and operate in the triode region. Using Eq. (1), we obtain the output current difference of Fig. 2

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as

$$I_1-I_2=F(V_1,V_{GA})-F(V_1,V_{GB})+F(V_2,V_{GB})-F(V_2,V_{GA})$$
$$=2K(V_{GA}-V_{GB})(V_1-V_2) \quad (2)$$

Further, the output of the integrator can be expressed as

$$V_{out}=V_x-\frac{2}{C}\int i_z\,d\tau \quad (3)$$

$$V_y=\frac{1}{C}\int I_2\,d\tau \quad (4)$$

According to Eqs. (2)–(4), the output voltage is given by

$$V_{out}=-\frac{1}{RC}\int V_{in}\,d\tau \quad (5)$$

where $R=\pm\dfrac{1}{\mu C_{ox}\dfrac{W}{L}(|V_{GA}|-|V_{GB}|)}$ and $V_{in}=V_1-V_2$

In Fig. 2, the gate voltages outside the parentheses apply to an inverting integrator, whereas those inside apply to a noninverting integrator.

III. Performance Analysis

In the above analysis, we have assumed the CCII+ and the MOS transistors to be ideal. However, practically an MOSFET in the strong inversion nonsaturation region can be modeled as a uniformly distributed RC transmission line for small signal operation[6]. The two–port admittance parameters for a uniformly distributed RC transmission line are given[7] by

$$Y=\frac{\sqrt{s\tau}}{R_t\sinh\sqrt{s\tau}}\begin{bmatrix}\cosh\sqrt{s\tau} & -1\\ -1 & \cosh\sqrt{s\tau}\end{bmatrix} \quad (6)$$

where τ is the product of the small–signal drain–to–source channel resistance, R_t, and the parallel combination of the channel–to–gate oxide capacitance and the channel–to–substrate depletion capacitance, C_t. Providing the operating frequency of the circuit is lower than $\omega_\gamma=1/\tau$ of the MOSFET, we can approximate the small signal transfer characteristics of this integrator as

$$V_{out}=\frac{\frac{1}{R_{t_2}}-\frac{1}{R_{t_1}}}{sC}V_{in}+$$

$$\left(\frac{\frac{s\tau}{2^1}+1}{sCR_{t_1}\left(\frac{s\tau}{6^1}+1\right)}+\frac{\frac{s\tau}{2^2}+1}{sCR_{t_2}\left(\frac{s\tau}{6^2}+1\right)}+1\right)(V_x-V_y)$$

$$\simeq\frac{\frac{1}{R_{t_2}}-\frac{1}{R_{t_1}}}{sC}V_{in} \quad (7)$$

R_{t_1} and C_{t_1} are the total distributed resistance and capacitance of the MOS transistors connected to V_{GA} in Fig. 2. Similarly, R_{t_2} and C_{t_2} are the total distributed resistance and capacitance of the MOS transistors connected to V_{GB}. This indicates that the output error of this integrator is mainly due to the offset voltage (V_x-V_y) of the input stage of the CCII+. However, departures from the ideal performance of this CCII+ may occur due to component mismatch, parasitic elements, and channel length modulation. The first output error is contributed by the voltage–to–current converter. If an impedance $Z=R_L$ is connected at Port X of Fig. 1, then we can calculate the percentage error of the transconductance G_m of the V–I converter as

$$\frac{\delta G_m}{G_m}\simeq\frac{1}{1+R_L\dfrac{g_{m_9}\,g_{m_1}}{g_{ds_6}}} \quad (8)$$

The second output error is associated with the current mirror formed by M9–M16, which can be expressed as

$$\frac{\delta I}{I}=\left(\frac{\delta K}{K}\frac{2\,\delta V_T}{V_T}+\frac{\delta\lambda\;V_{DS}+\lambda\;\delta V_{DS}}{1+\lambda\;V_{DS}}\right)_{M_{15\text{-}16}}$$
$$\pm\left(\frac{\delta K}{K}-\frac{2\,\delta V_T}{V_T}+\frac{\delta\lambda\;V_{DS}+\lambda\;\delta V_{DS}}{1+\lambda\;V_{DS}}\right)_{M_{9\text{-}10}} \quad (9)$$

where λ is the channel length modulation coefficient. The above errors will cause performance degradation from that predicted by Eqs. (5) and (7).

IV. Design and Optimization

A CMOS current conveyor including junction and layout parasitics was simulated. The transistor sizes are shown in Table 1, and the simulated performances are shown in Table 2. Based on the above building blocks, fully integrated continuous–time MOSFET–capacitor filters using CMOS CCIIs can be constructed. As an example, a six–order doubly terminated ladder filter is designed to realize a bandpass response with center frequency at 460KHz, 0.5dB ripple in the passband, and a bandwidth of 120KHz. In this filter, the output buffer of the proposed integrator is realized as a unity–gain buffer. According to equation (5), one could design the required filter performance to meet the specifications. However, it is based on the assumptions that the effective channel mobility μ is constant, the parasitic capacitances are negligible, and all the building blocks are ideal. To reduce the deviations caused by nonideal device characteristics, it is desirable to automate the design of the filters [8].

We have implemented the *Steepest descent* algorithm and test several examples. The program interfaces SPICE and adjusts the design parameters directly on the SPICE input deck. Since our ESPICE[9] does not have sensitivity computation capability, the required sensitivities are computed by the *finite difference approximation*. The simulated frequency response of this six–order bandpass filter before and after optimization are both shown in Fig. 3(b). The resulting design parameters are compared as shown in the Table 3.

V. Conclusions

We have proposed a new CMOS current conveyor and continuous–time integrators suitable for high frequency IC filter applications. A six–order ladder bandpass filter is designed using the proposed method as an example. Results from extensive ESPICE simulations have verified the

functionality of this technique. The results reported in the paper will be useful in the realization of high frequency integrated MOSFET–capacitor filters.

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Table 1 TRANSISTOR SIZES

CMOS Current Conveyor(Fig 1(b))						
	W	L		W	L	units: μm
M_1	40	5	M_9	130	5	
M_2	40	5	M_{10}	130	5	
M_3	40	10	M_{11}	130	5	
M_4	40	10	M_{12}	130	5	
M_5	65	5	M_{13}	60	5	
M_6	65	5	M_{14}	60	5	
M_7	60	5	M_{15}	60	5	
M_8	60	5	M_{16}	60	5	

Table 2 Simulated performances of Fig. 1(b)

Unity–GBW (C_L=10pF), MHz	9.8
Slew rate (C_L=10pF), V/μs	8
Output range, V	+4, –4
THD (@$R_L \geq$50K,100KHz,±3V) (Total harmonic distortion)	0.014%

Table 3 Aspect ratios for MRC in Fig. 3(a)

Resistors	Original design W/L	Optimized design W/L unit:μm
R_1	6/40	6/34
$R_{2,5,6}$	6/40	6/39
$R_{4,7,8}$	6/40	6/36
$R_{10,12}$,R_L	6/40	6/41
R_3	6/40	6/36
R_9	6/40	6/30
R_{11}	6/40	6/46

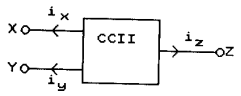

Fig 1(a) The CMOS CCII+ symbol

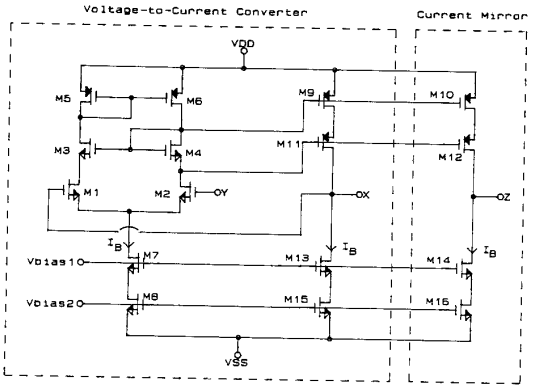

Fig 1(b) The simplified CMOS CCII+ circuit

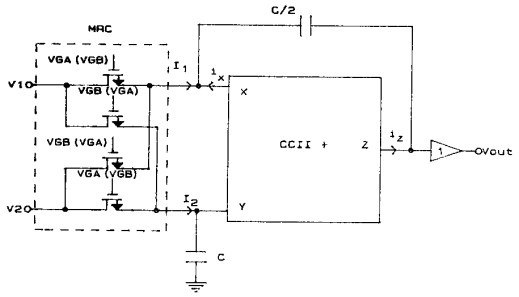

Fig 2 The integrator circuit

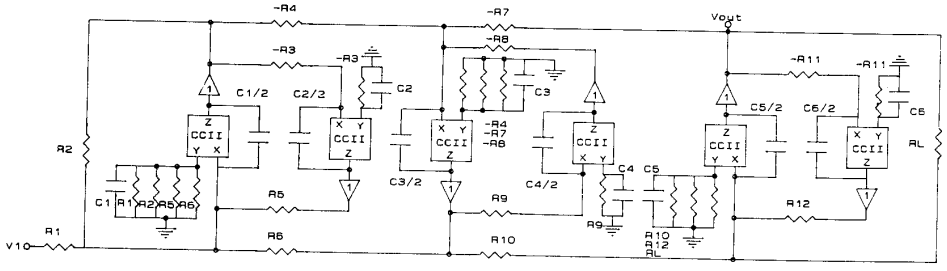

Fig 3(a) A sixth–order bandpass filter circuit with a passive R–pair representing the MRC in the Fig 2

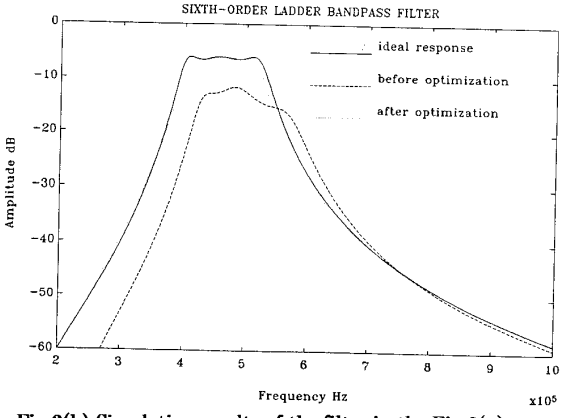

Fig 3(b) Simulation results of the filter in the Fig 3(a)