A Low-Voltage Fully-Integrated 4.5-6-GHz CMOS Variable Gain Low Noise Amplifier

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Abstract — **A 4.5-6 GHz CMOS low-voltage wideband variable gain low noise amplifier (VGLNA) with wide gain-control range has been demonstrated in this paper. The VGLNA, operating at a supply voltage as low as 1 V, achieves a small signal gain of 20 dB and 3-dB bandwidth of 1.5 GHz with good return losses. The noise figure is 3.5 dB at 5.5 GHz. A figure-of-merit for gain efficiency (Gain/P_{DC}) of 1.23 dB/mW is achieved, which is believed to be the best among reported results for a CMOS VGLNA operating at multi-GHz frequency.**

I. INTRODUCTION

The CMOS RF chips are getting more and more attractive owing to the advantages of low cost and integration ability with baseband circuits. LNAs using CMOS process have demonstrated good gain and noise per- formance in the 5-6 GHz ISM band [1-3]. Variable gain low noise amplifiers (VGLNAs) were realized in order to maximize the overall system dynamic range [4]. A 1.4-dB NF variable-gain low noise amplifier using InGaP emitter HBT has been presented in [4], but GaAs-based chip is difficult to integrate with CMOS baseband circuits. A variable gain cascode amplifier using SiGe HBT technology has been demonstrated in [5], however, the cascode topology is not suitable for variable-gain low noise and low voltage application [7]. A CMOS 900-MHz fully differential [6] and a CMOS 8-9-GHz low voltage [7] variable-gain low noise amplifier have also been proposed, but off-chip elements are required. In this paper, we used 0.18- m CMOS process to design a low-voltage variable-gain low noise amplifier without any off-chip elements. Wide bandwidth is also achieved by splitting inter-stage matching frequency. Table 1 summarizes the recently reported performance of variable gain low noise amplifiers compared with this work. It is observed that our chip demonstrated the widest bandwidth, gain-control range (GCR) and the best gain efficiency for a CMOS VGLNA operating at multi-GHz frequency. The VGLNA chip achieves 20-dB gain, bandwidth of 1.5 GHz, noise figure of 3.5 dB, input return loss of 13 dB, and output return loss of 23 dB, operating at a low

	Freq. (GHz)	BW (GHz)	BW/fc (%)	NF (dB)	Gain (dB)	GCR (dB)	Gain / P_{DC} (dB/mW)	$\|S_{11}\|$ (dB)	$\|S_{22}\|$ (dB)	P_{DC} (mW)	Vdd (V)	Ref.
InGaP HBT	1.95	-	-	1.4	15	40	0.45	-	-	33	3	[4]
0.5μm SiGe HBT	8	4	50	-	12.5	16	0.33	-7.5	-13	400	4	[5]
0.35μm CMOS	0.9	0.2	22.2	2	22 *	5	1.02	-	-	21.6	2.7	[6]
0.18μm CMOS	7.5	1.2	16	3.2	13.5	11.4	0.6	-5.8	-14	22.4	1	[7]
0.18μm CMOS	8.6	1.2	14	3.7	12.2	11.2	0.62	-5.4	-12	19.6	1	[7]
0.18μm CMOS	**5.2**	**1.5**	**28.8**	**3.5**	**20**	**20**	**1.17**	**-13**	**-25**	**17**	**1**	**This work**

Table 1. Recently reported performance of variable gain low noise amplifiers. BW: 3-dB bandwidth. f_c: center frequency. Gain/P_{DC}: the ratio of gain to dc-power-consumption [9]. The notation * means voltage gain.

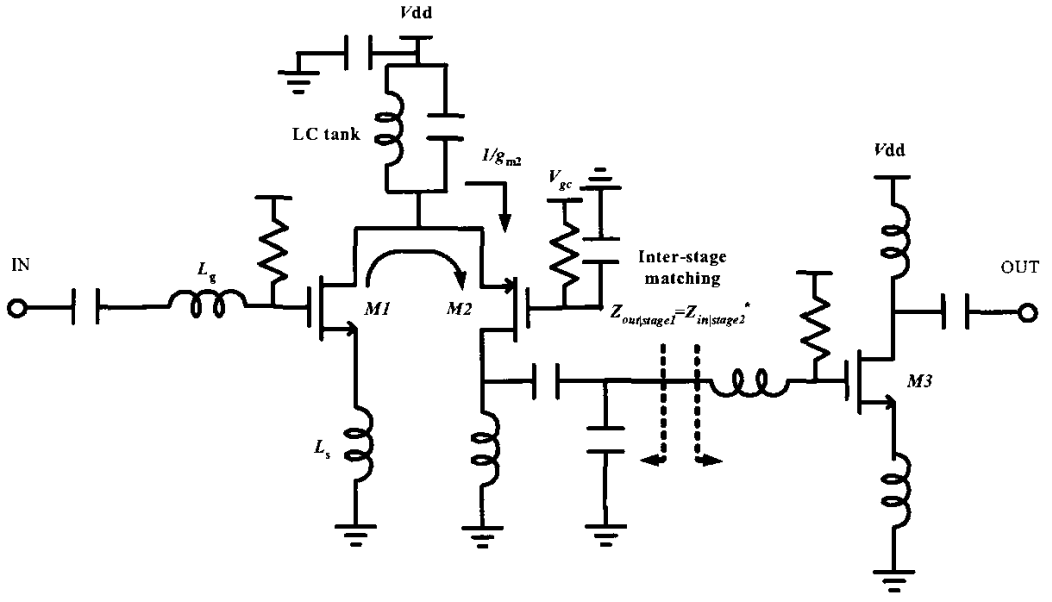

Fig. 1. Circuit schematic diagram of the folded cascode variable gain low noise amplifier.

supply voltage of 1 V and 17 mW power consumption, with a chip size of 1.2 × 1 mm^2 using a 0.18-μm CMOS standard process.

II. CIRCUIT DESIGN AND FABRICATION

In contrast to the conventional cascode FET, the VGLNA design employes a folded cascode structure in order to operate at a low supply voltage [7]. In this paper, VGLNA includes three portions: the first is the low-noise stage, the second is the gain control stage and the last is the gain stage. The schematic of this VGLNA is shown in Fig. 1.

Input matching, which is necessary to minimize signal reflection and noise, is an important design issue. There is usually a trade-off between noise and input impedance matching in LNA design. The input matching is achieved by selecting L_g, L_s and the gate-to-source capacitance (C_{gs1}) of the input NMOS common-source transistor to fulfill the following equations [8]:

$$\omega_{RF} = \frac{1}{\sqrt{(L_g + L_s)C_{gs1}}} \quad (1)$$

$$R_{source} = \frac{g_{m1}}{C_{gs1}} L_s \quad (2)$$

where ω_{RF} is the carrier frequency, g_{m1} is transconductance of the input common-source transistor and R_{source} is the impedance of the signal source.

Between the two folded cascode FETs is an LC-tank network, acting as a high impedance element at resonant frequency to force signal passing through the followed PMOS for overall small signal gain ($|S_{21}|$). In our circuit, we design the resonant frequency slightly higher than the target frequency, 5-6 GHz. The second inter-stage impedance matching network is designed at about 4.2 GHz, slightly lower than in-band frequency, to compensate the narrow-band property of LC tank to achieve wideband performance. The LC tank network between low-noise stage and gain-control stage, shown in Fig. 1 is a high impedance network, and also supports bias current path to both stages. The main advantage of this LC-tank folded cascode design is that it does not require any off-chip element, such as RF-choke inductors. First LC-tank network and second inter-stage matching are designed to fit higher frequency and lower frequency, respectively. Simulation result of small signal gain is shown in Fig. 3. It is observed that operation frequency is from 4.2 - 6.5 GHz by splitting matching frequency.

The gain-control is achieved by modifying the gate voltage of the PMOS common-gate transistor (V_{gc}) without affecting the bias condition and impedance matching, which are determined by the input NMOS common-source transistor. Hence, the optimum input noise is almost not affected when controlling the overall gain of this circuit. This CMOS VGLNA was fabricated using a 0.18-μm standard CMOS process. A die micrograph is shown in Fig. 2. The chip size is 1.2 × 1 mm^2.

III. MEASUREMENT RESULTS

The circuit was measured via on-wafer probing. Figs. 3 and 4 show the measured and simulated results of the gain, return loss and noise figure. With a power consumption of around 17mW from a 1 V supply, the small signal gain is 20 dB with a 3-dB bandwidth of 1.5 GHz. The minimum input and output reflection coefficients are -13 dB and -23 dB respectively. The measured noise figure is only 3.5 dB at 5.6 GHz and below 5 dB in the frequency of interest. The measured results of S-parameters and noise figure agree with the simulation well. Variable gain performance with 2.5-dB gain steps from is shown in Fig. 5. The GCR is about 20 dB while bandwidth is maintained over all variable-gain condition. The variable gain control performance of the amplifier was achieved by current limiting of the common-gate PMOS in the folded cascode topology. The input P_{1dB} is -15 dBm. The measurement results show that this CMOS VGLNA design can operate properly at a high frequency with a low supply voltage down to 1 V.

IV. CONCLUSION

An ISM-band variable-gain low noise amplifier has been designed, fabricated, and tested. The VGLNA uses folded-cascode configuration and was fabricated by TSMC standard 0.18-μm CMOS technology. Our circuit demonstrated the widest bandwidth, gain-control range (GCR) and the best gain efficiency for a CMOS VGLNA operating at multi-GHz frequency. The VGLNA chip achieves a 20-dB gain, a bandwidth of 1.5 GHz, a noise figure of 3.6 dB, an input return loss of 13 dB, and an output return loss of 23 dB, operating at a low supply voltage of 1 V and 17 mW power consumption, with a chip size of 1.2 × 1 mm^2 in a 0.18-μm CMOS standard process.

V. ACKNOWLEGEMENT

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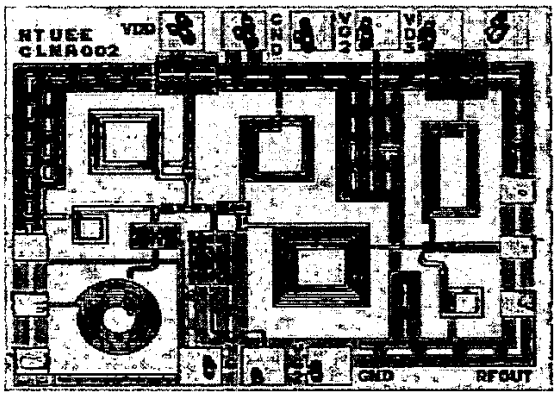

Fig. 2. The die photo of the VGLNA with chip area of 1.2×1 mm^2.

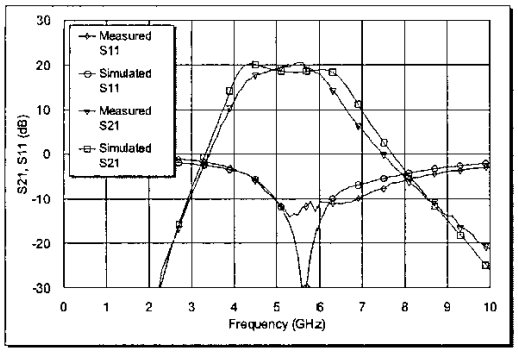

Fig. 3. The measured and simulated results of the power gain and input return loss.

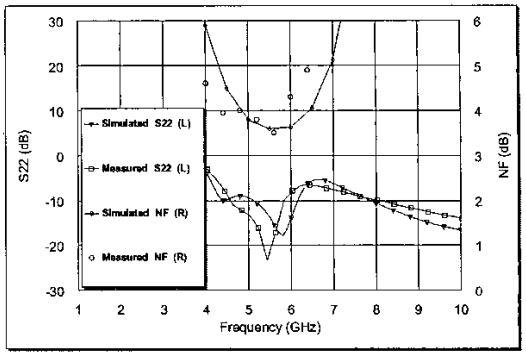

Fig. 4. The measured and simulated results of the noise figure and output return loss.

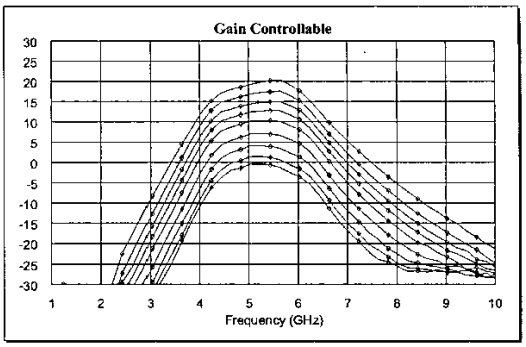

Fig. 5. The measured variable gain performance in 2.5-dB gain steps versus frequency, V_{gc}= 0-1.8 V.