Quality Improvement of Ultrathin Gate Oxide by Using Thermal Growth Followed by SF ANO Technique

Yi-Lin Yang and Jenn-Gwo Hwu, *Senior Member, IEEE*

***Abstract*—Rapid thermal oxide followed by anodization in direct current superimposed with scanning frequency alternating current was demonstrated for the first time to have an improved quality in ultrathin gate oxides. Compared with the thermal oxide grown without the scanning-frequency anodization (SF ANO) treatment, the gate leakage current density (J_g) of SF ANO sample is significantly reduced without increasing the thickness of gate oxide. In addition, it could be observed that the interface trap density (D_{it}) is reduced with tighter distribution. It is suggested that the bulk traps and interface traps in thermally grown oxide can be repaired during the SF ANO process.**

***Index Terms*—Metal–oxide–semiconductor (MOS), scanning frequency anodization (SF ANO), ultrathin gate oxide.**

I. Introduction

SILICON dioxide (SiO_2) has been used as the gate dielectric in metal–oxide–semiconductor field-effect transistors (MOSFETs) for 40 years because of its excellent stability, uniformity, and simple fabrication process. The gate oxide thickness below 2 nm is required as the devices are scaled [1]. Ultrathin oxide is hard to achieve through a rapid thermal process (RTP) under conventional high temperature because of the high oxidation rate. However, as the growth temperature of thermally grown ultrathin oxides is reduced for better control, many weak spots and pinholes are generated, and result in unreliable properties [2], [3]. It is believed that the defects in the oxide will enhance the gate leakage current significantly, which in turn degrade the device performance and cause device failure eventually [4], [5]. The oxide reliability now becomes a serious issue [6], [7]. A new method called thermal growth followed by scanning frequency anodization (SF ANO), characterized by changing the frequency during the anodization process is proposed in this work to prepare ultrathin gate oxide. The experimental results show that the SF ANO samples have reduced gate leakage current and interface trap density without increasing the thickness of gate oxide.

Manuscript received June 29, 2004; revised July 26, 2004. This work was supported by the National Science Council of China under Contract NSC 93-2215-E-002-016. The review of this letter was arranged by Editor C.-P. Chang.

Y.-L. Yang is with the Department of Electrical Engineering, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, R.O.C.

J.-G. Hwu is with the Department of Electrical Engineering, Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. and also with the Department of Electronics/Electrical Engineering, National United University, Miaoli, Taiwan, R.O.C. (e-mail: hwu@cc.ee.ntu.edu.tw).

Digital Object Identifier 10.1109/LED.2004.836031

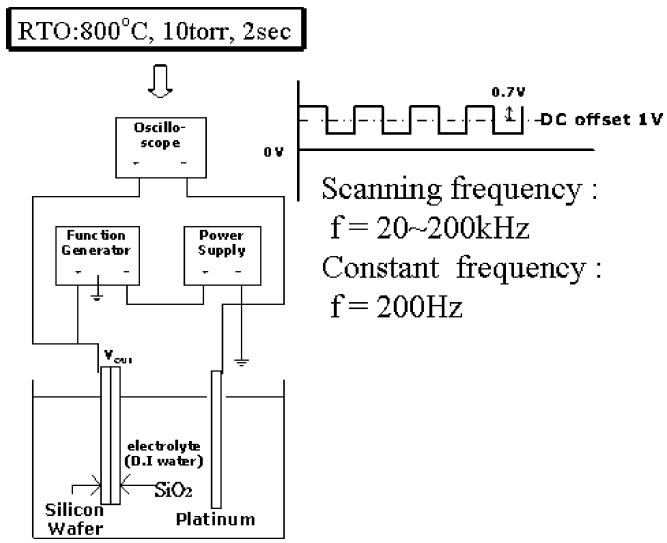

Fig. 1. Schematic diagrams of the experimental setup of anodization and dc superimposed with ac (DAC) applied voltage.

II. Experimental

The 3-in boron-doped p-type (100) silicon wafers with a resistivity of 1–10 Ω-cm were used in this experiment. After standard RCA cleaning, thermal oxides of 18-, 20-, and 23-Å thicknesses were performed on three pieces of wafers in RTP with O_2 ambient, separately. Subsequently, two samples of each thickness were treated in anodization process for 10 min, as shown in Fig. 1. A positive dc voltage of 1 V superimposed with an ac oscillation of 0.7 V was used in the anodization process. Such low applied voltage was used to ensure that there was no increasing of oxide thickness during the anodization process. Deionized water was used as electrolyte to avoid contamination. Two conditions of ac frequencies, that is, constant-frequency (CF) at 200 Hz and SF from 20 Hz to 200 kHz, were considered as shown in Fig. 1 in the anodization process. These two samples were denoted as RTO+CF ANO and RTO+SF ANO, respectively. Another sample without anodization treatment was denoted as RTO. Post oxidation annealing was carried out to all samples in 100 torr N_2 at 850 °C for 15 s. After Al film deposition, the MOS capacitors of size 150 × 150 μm were formed by conventional photolithography. The back oxide was removed with buffered HF solution, and Al was formed as the back contact. The capacitance–voltage (C–V) curves were measured with an HP4280 precision LCR meter and the current–voltage (J–V) curves with an HP-4140.

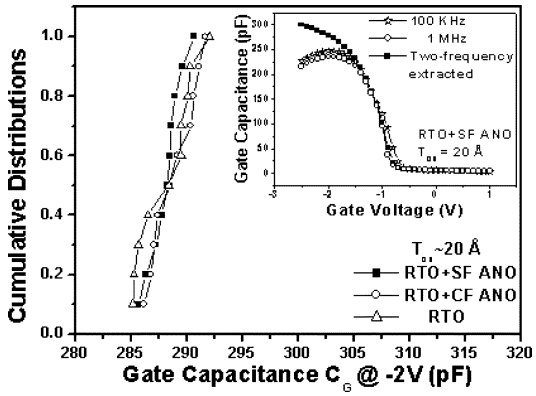

Fig. 2. Cumulative distributions of gate capacitance for RTO+SF ANO, RTO+CF ANO, and RTO samples. The inset shows the *C–V* curves measured at 100 K, 1 MHz and after two-frequency extraction for a RTO+SF ANO sample.

III. Result and Discussion

The extracted capacitance was obtained from the two-frequency correction method [8] as shown in the inset of Fig. 2, and the oxide thickness could be fitted from the extracted capacitance under the consideration of quantum mechanical effect [8]. Cumulative distributions of extracted gate capacitance C_G at -2 V for $\mathrm{T_{ox}} = 20$ Å samples are plotted in Fig. 2. It is observed that the oxide thickness does not increase after the anodization process because of the sufficiently low anodization voltage, and oxide grew only over the weak spots during the anodization process [9]. The capacitance could not be measured precisely for the thinner oxide (i.e., less than 18 Å) because of the large gate leakage current; however, it is believed that there will not be a significant increase in oxide thickness after the anodization process.

The *J–V* characteristics of the samples are shown in Fig. 3(a), and the cumulative distributions of gate current density at $V_{\mathrm{FB}} - 1$ V for all samples with two different oxide thicknesses are plotted in Fig. 3(b). It is observed that J_g is reduced after the anodization treatment as the weak spots and traps in gate oxides are repaired and modified during the anodization process. At the moment of voltage switching, the redistribution and reselection of $\mathrm{OH^-}$ ions, which are frequency-related, will move toward the leaky path and repair the defects in the oxides [10]. The $\mathrm{OH^-}$ ions can only passivate the imperfect dangling bonds in the interface areas related to leaky paths but not interact with the interface areas protected by perfect bulk oxides in the low electric field. Comparing the CF and the SF samples, the SF sample shows a smaller gate leakage current. It is suggested that the bonding energies of defects in the gate oxide differ from each other; for example, the trivalent Si atom with oxygen vacancy in the gate oxide shows its special energy level, and different response times are needed to patch the defects with various energy levels. The various response times are provided by using SF, and it is proposed that more defects could be repaired and more traps could be modified. It can also be observed that the improvement for the thinner oxide is more significant than the thicker one. It is because the thinner oxide grown in a lower temperature and in a shorter time results in more defects created. Therefore, the

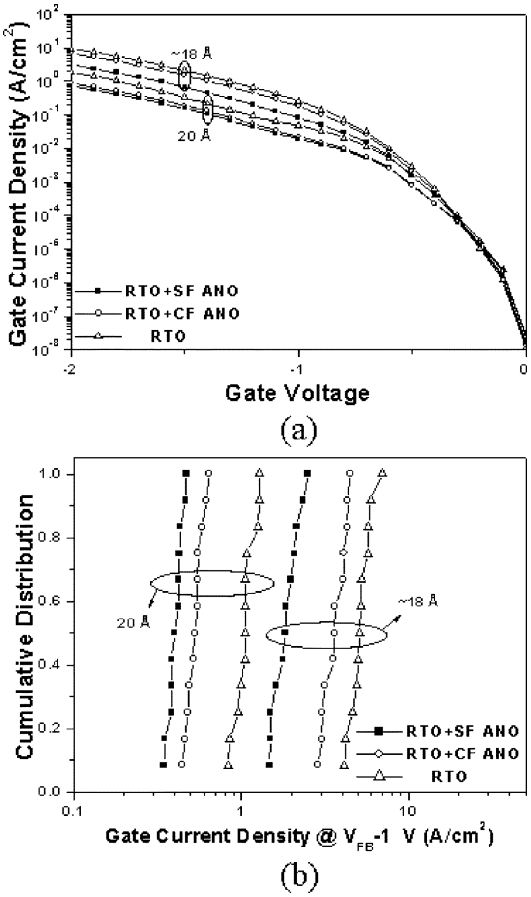

Fig. 3. (a) *J–V* curves at negative gate bias for typical samples with 18- and 20-Å gate oxide thickness. (b) Cumulative distributions of gate current density at $V_{\mathrm{FB}} - 1$ V gate bias for RTO+SF ANO, RTO+CF ANO, and RTO samples with two oxide thicknesses.

effect of anodization reparation in the thinner oxide is more apparent than in the thicker oxide, and the SF ANO is more effective than the CF.

The 10 K and 100 KHz *C–V* curves are used to evaluate interface trap density in this work [11]. The electrons that could be caught and held by the interface traps at low frequency performed an interface trap-induced capacitance (C_{it}) near flatband voltage, and interface trap density (D_{it}) could be obtained. A hump could be observed near the flat band voltage V_{FB}. The higher hump means more interface traps exist in the oxide/Si-substrate interface. By examining the *C–V* curves in the depletion region, one can find that RTO+SF ANO sample shows the least interface trap density in the three samples, and the RTO+CF ANO sample also shows less D_{it} than the RTO sample. The comparison of C_{it} with 23-Å oxide thickness samples is illustrated in Fig. 4. The sample RTO+SF ANO shows not only the smallest C_{it} but also the best uniformity in all samples. Sample RTO+CF ANO also shows a slight improvement in interface trap density than the RTO sample. It is possible that during the anodization process, $\mathrm{OH^-}$, which is divided from $\mathrm{H_2O}$ by the electrical field, is attracted into the interface. As the ac signal changes with frequency, $\mathrm{OH^-}$ is caught by silicon–dangling bond and combined with it during the positive cycle, and relaxed during the negative cycle. $\mathrm{OH^-}$ can passivate more interface traps as the electric field changes up and down. The interface trap densities were reduced due to the

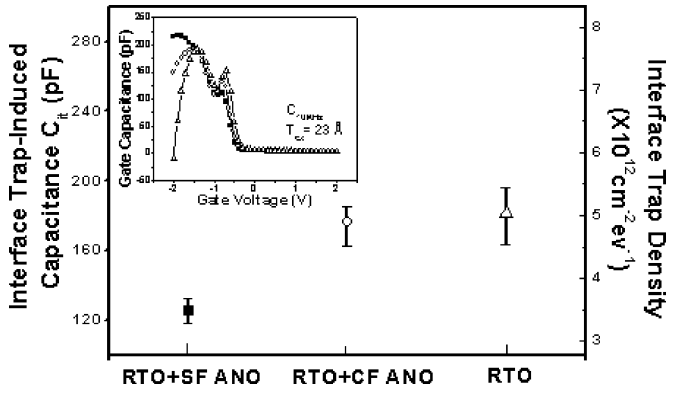

Fig. 4. Comparison of interface trap-induced capacitance ($C_{\rm it}$) and interface trap density ($D_{\rm it}$) for RTO+SF ANO, RTO+CF ANO, and RTO samples. The inset shows the *C–V* curves measured at 10 KHz for three typical samples with a $T_{\rm ox}$ of 23 Å.

passivation of silicon-dangling bond [11] during the repeated ac signal. In addition, the interface traps may distribute with energy level, and different response times should be considered. Moreover, different frequencies responded to the different energies of interface traps. More interface traps could be passivated if more frequencies are used during the anodization process. It is suggested that the SF technique could reduce the interface trap density more efficiently than the CF technique.

IV. Conclusion

In this letter, thermal growth followed by the SF ANO technique was proposed for the first time to improve the quality of ultrathin gate oxide. The gate leakage current density decreases without significant increase in the oxide thickness after the anodization process. In addition, the interface trap densities are reduced and uniformed apparently because of the possible passivation of interfacial dangling bonds. The SF ANO technique demonstrates great potential for improving the quality of the existing ultrathin gate oxides.

References

[1] *The International Technology Roadmap for Semiconductors*, Semicond. Industry Assoc., 2002.

[2] W.-J. Liao, Y.-L. Yang, and J.-G. Hwu, "Growth-then-anodization technique for reliable ultrathin gate oxides," *J. Electrochem. Soc.* , to be published.

[3] R. Paily and A. DasGupta, "Improvement in electrical characteristics of ultrathin thermally grown SiO_2 by selective anodic oxidation," *IEEE Electron Device Lett.*, vol. 23, pp. 707–709, Nov. 2002.

[4] J. Sune, E. Miranda, M. Nafria, and X. Aymerich, "Point contact conduction at the oxide breakdown of MOS devices," in *IEDM Tech. Dig.*, 1998, pp. 191–194.

[5] W. K. Henson, N. Yang, and J. J. Wortman, "Observation of oxide breakdown and its effects on the characteristics of ultrathin-oxide nMOSFE's," *IEEE Electron Device Lett.*, vol. 20, pp. 605–607, Oct. 1999.

[6] D. A. Buchanon and S. H. Lo, "Reliability and integration of ultrathin gate dielectrics for advanced CMOS," *Microelectron. Eng.*, vol. 36, pp. 13–20, 1997.

[7] E. Miranda and A. Cester, "Degradation dynamics of ultrathin gate oxides subjected to electrical stress," *IEEE Electron Device Lett.*, vol. 24, pp. 404–406, May 2003.

[8] K. J. Yang and C. Hu, "MOS capacitance measurements for high-leakage thin dielectrics," *IEEE Trans. Electron Devices*, vol. 46, pp. 1500–1501, Oct. 1999.

[9] M.-J. Jeng and J.-G. Hwu, "Thin-gate oxides prepared by pure water anodization followed by rapid thermal densification," *IEEE Electron Device Lett.*, vol. 17, pp. 575–577, Aug. 1996.

[10] Z. H. Chen, S. W. Huang, and J. G. Hwu, "Electrical characteristics of ultrathin gate oxide (< 3 nm) prepared by direct current superimposed with alternating-current anodization," *Solid State Electron.*, vol. 48, pp. 23–28, 2004.

[11] S.-W. Huang and J.-G. Hwu, "Electrical characterization and process control of cost-effective high-k aluminum oxide gate dielectrics prepared by anodization followed by furnace annealing," *IEEE Trans. Electron Devices*, vol. 50, pp. 1658–1664, Oct. 2003.