Band offsets and charge storage characteristics of atomic layer deposited high-*k* HfO_2/TiO_2 multilayers

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The band offsets and charge storage characteristics of atomic layer deposited high-*k* HfO_2/TiO_2 multilayers with ten periods in *p*-$Si/SiO_2/(HfO_2/TiO_2)/Al_2O_3$ structure have been investigated. The thickness of high-*k* HfO_2 or TiO_2 film is ~0.5 nm for each layer, before and after annealing treatment of 900 °C for 1 min in N_2 ambient. High-resolution transmission electron microscopy, x-ray photoelectron spectroscopy, and ultraviolet photoelectron spectroscopy measurements on high-*k* HfO_2/TiO_2 multilayers confirm the layer-by-layer structure after annealing treatment, suggesting the HfO_2/TiO_2 multilayer quantum wells. The valence band offsets of HfO_2 and TiO_2 films are found to be ~3.1 and ~1.5 eV, respectively. The conduction band offsets are found to be ~1.7 eV for HfO_2 films and ~0.9 eV for TiO_2 films. The high-*k* HfO_2/TiO_2 multilayers in *p*-$Si/SiO_2/(HfO_2/TiO_2)/Al_2O_3$/aluminum memory capacitor show a large capacitance-voltage hysteresis memory window of ~5 V at gate voltage of ±5 V, due to the charge storage in multilayer quantum wells. The hysteresis memory window of ~1.3 V at small gate voltage of ±1 V is also observed. The high-*k* HfO_2/TiO_2 multilayer memory structure can be used in future nanoscale flash memory device applications. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2751579]

Nonvolatile memory devices achieving high-speed writing and erasing of data with a low gate voltage ($V_g < 5$ V), consuming less power and allowing higher integration have an important position in the semiconductor industry for future nanoscale flash memory device applications. Due to poor retention and scaling issues in poly-Si-oxide-silicon-nitride-oxide-silicon nonvolatile memory devices,[1] the high-*k* charge trapping layers such as Al_2O_3, La_2O_3, ZrO_2, and HfO_2 in a metal-oxide-high-*k*-oxide-silicon structure are reported.[2–7] To further improve the scaling and to increase the program/erase speed, the high-*k* dielectric with a large barrier height such as Al_2O_3 can also act alternatively as a blocking oxide for high-speed flash memory device applications.[8–10] Recently, the high-*k* HfO_2 charge trapping layers in metal-aluminum-oxide-high-*k*-oxide-silicon (MAOHOS) structure with a large gate voltage operation ($V_g > 5$ V) are also reported.[9,10] To obtain a low gate voltage operation, high-speed, excellent retention, and highly scalable flash memory devices, the high-*k* HfO_2/TiO_2 multilayer quantum wells with an Al_2O_3 blocking oxide in MAOHOS structure have been proposed. In this letter, the band offsets and excellent charge storage characteristics of atomic layer deposited high-*k* HfO_2/TiO_2 multilayer quantum wells have been reported. The pure HfO_2 and TiO_2 charge trapping layers in MAOHOS structure have also been studied for comparison.

p-type Si (100) substrates (4 in.) with a resistivity of 15–25 Ω cm were cleaned by dipping in dilute HF for 1 min using the RCA process to remove native oxide from the surface. After cleaning the *p*-Si substrate, a tunneling oxide (SiO_2) with a thickness of 3 nm was grown by rapid thermal

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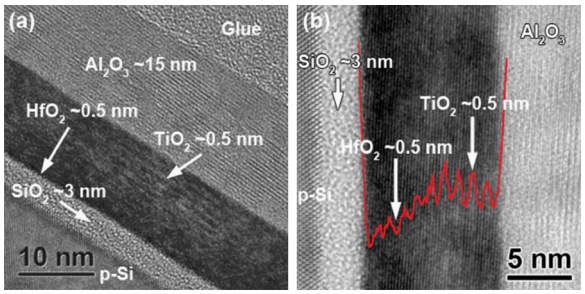

FIG. 1. (Color online) (a) HRTEM image of high-k HfO_2 (0.5 nm)/TiO_2 (0.5 nm) multilayers with ten periods in p-Si/SiO_2/(HfO_2/TiO_2)/Al_2O_3 structure after annealing treatment of 900 °C for 1 min in N_2 ambient. (b) HRTEM image with elemental line profile by DIGITAL MICROGRAPH software shows the clear HfO_2/TiO_2 layer-by-layer structure (red color).

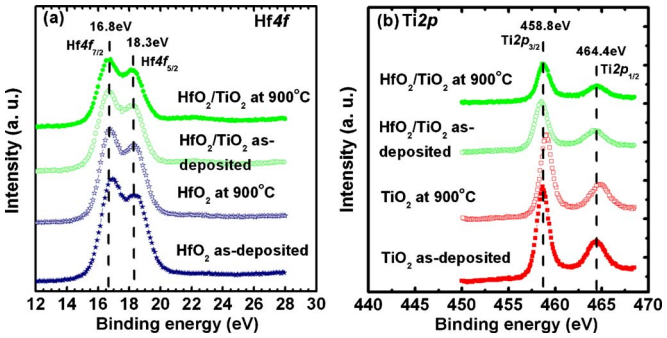

FIG. 2. (Color online) XPs spectra of (a) Hf 4f and (b) Ti 2p signals for pure HfO_2, pure TiO_2, and HfO_2(0.5 nm)/TiO_2(0.5 nm) multilayers with ten periods of as-deposited and after annealing treatment.

oxide system at a temperature of 1000 °C for 20 s. Then, the high-k HfO_2 film with a thickness of 0.5 nm for each layer was grown by atomic layer deposition (ALD) using hafnium tetrachloride ($HfCl_4$) at a substrate temperature of 300 °C. The high-k TiO_2 film with a thickness of 0.5 nm for each layer was deposited by plasma-enhanced atomic layer deposition (PEALD) using titanium (IV) isopropoxide precursor at a substrate temperature of 350 °C. The high-k HfO_2/TiO_2 multilayers with ten periods were deposited on SiO_2 (3 nm)/p-Si substrate. Basically, the total thickness of charge storage layer was ~10 nm. For comparison, the pure HfO_2 charge trapping layer with a thickness of 10 nm or pure TiO_2 charge trapping layer with a thickness of 10 nm was deposited on SiO_2 (3 nm)/p-Si substrate. Then, the high-k Al_2O_3 film as a blocking oxide was grown by ALD using trimethylaluminium [$Al(CH_3)_3$] precursor at a substrate temperature of 300 °C. The thickness of Al_2O_3 film was ~15 nm. All high-k films were *in situ* deposited by ALD/PEALD cluster tool. The postdeposition annealing (PDA) treatment at a temperature of 900 °C for 1 min in N_2 ambient was carried out for all memory structures. The post-metal annealing treatment at a temperature of 400 °C for 5 min was also carried out using N_2 (90%) and H_2 (10%) gases. All memory capacitors were fabricated using an aluminum (Al) metal gate electrode (gate area: 50×50 μm^2) with a lithography process. To probe the thickness and microstructure of high-k HfO_2/TiO_2 multilayers, high-resolution transmission electron microscopy (HRTEM) was performed using a FEI Technai F30 field emission system with an operating voltage of 300 kV and a resolution of 0.17 nm. X-ray photoelectron spectroscopy (XPS) was performed to investigate the interaction between the ultrathin HfO_2 and TiO_2 layers for as-deposited and after PDA treatment. To obtain the valence band and conduction band offsets of high-k HfO_2/TiO_2 multilayers, the ultraviolet photoelectron spectroscopy (UPS) was carried out. Electrical characteristics of memory capacitors were performed using HP 4284A *LCR* meter and HP 4156B semiconductor analyzer systems.

Figure 1(a) shows a HRTEM image of high-k HfO_2/TiO_2 multilayers after PDA treatment. The thicknesses of tunneling oxide (SiO_2) and blocking oxide (Al_2O_3) are found to be ~3 and ~15 nm, respectively, while the thickness of HfO_2 or TiO_2 film is observed ~0.5 nm for each layer. The thickness of as-deposited HfO_2 or TiO_2 film is also observed ~0.5 nm for each layer (not shown here). The high-k Al_2O_3 film as a blocking oxide shows partial crystalline, while the high-k HfO_2/TiO_2 multilayers show fully crystalline with maintaining the layer-by-layer structure. Figure 1(b) shows a HRTEM image with an elemental line profile (red color) of high-k HfO_2/TiO_2 multilayers plotted by the Gatan "DIGITAL MICROGRAPH." The high-k HfO_2/TiO_2 multilayers show a layer-by-layer structure, indicating that there is no intermixing between the HfO_2 and TiO_2 films after high temperature annealing treatment of 900 °C for 1 min in N_2 ambient, and it has also been confirmed by XPS measurement below.

The XPS spectra of pure HfO_2, pure TiO_2, and HfO_2 (0.5 nm)/TiO_2 (0.5 nm) multilayers for as-deposited and after PDA treatment are shown in Fig. 2. The binding energy of Hf $4f_{7/2}$ electrons is the same (~16.8 eV) for all memory structures of as-deposited and after PDA treatment [Fig. 2(a)], which is close to the reported value of binding energy (~16.7 eV) of HfO_2 films on Si substrate.[11] The binding energy of Ti $2p_{3/2}$ electron is also the same (~458.8 eV) for as-deposited and after PDA treatment [Fig. 2(b)], which is similar to the reported value.[12] Note that the binding energies of Hf–O and Ti–O bonds for HfO_2/TiO_2 multilayers are similar to the pure HfO_2 and TiO_2 films for as-deposited and after PDA treatment. It indicates that there is no interdiffusion or intermixing between the Hf and Ti atoms in HfO_2/TiO_2 multilayers after high temperature annealing treatment, which is corroborated by the HRTEM image.

The valence band as well as the conduction band offsets of HfO_2/TiO_2 multilayers have been measured by UPS. Figure 3(a) shows the UPS spectra of pure HfO_2, pure TiO_2, and HfO_2 (0.5 nm)/TiO_2 (0.5 nm) multilayers with ten periods on SiO_2 (3 nm)/p-Si substrates after PDA treatment. A −4 V bias is applied to the substrate to overcome the analyzer work function during UPS measurement. The valence band maximum (VBM) $[(E_f)_{Si}-(E_v)_{high\ k}]$ is found to be ~3.4 eV for pure HfO_2, ~1.8 eV for pure TiO_2, and ~2.6 eV for HfO_2/TiO_2 multilayers. Note that the VBM value of HfO_2/TiO_2 multilayer structure has an average value of the VBM of pure HfO_2 and TiO_2 films. Considering a doping of $\sim1\times10^{15}$ cm^{-3} for p-Si substrate, the energy difference of $(E_f)_{Si}-(E_v)_{Si}$ is ~0.3 eV. So, the valence band offsets $[\Delta E_v\approx(E_v)_{Si}-(E_v)_{high\ k}]$ for pure HfO_2 and TiO_2 films are found to be ~3.1 and ~1.5 eV, respectively, which are similar to the reported values.[12,13] The band gap energies (E_g) of pure HfO_2 and TiO_2 films measured by XPS method[14] are ~5.9 and ~3.5 eV, respectively (not shown here). Assuming a band gap energy of Si substrate ($E_g\approx1.1$ eV), the conduction band offsets $[\Delta E_c\approx(E_g)_{high\ k}-(E_g)_{Si}-\Delta E_v]$ are ob-

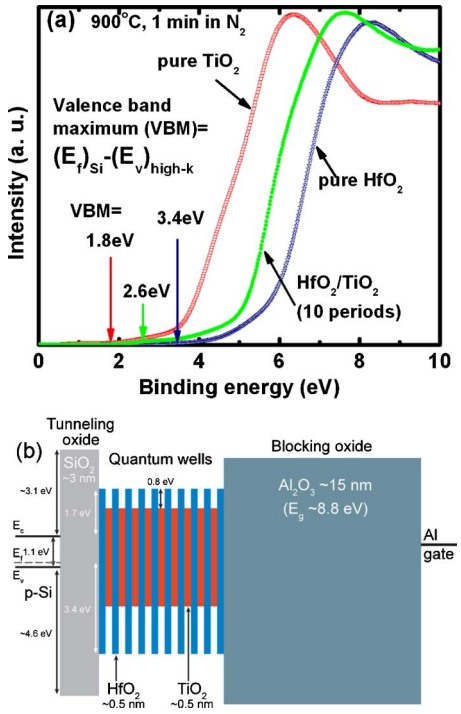

FIG. 3. (Color online) (a) UPS spectra of pure HfO_2, pure TiO_2, and HfO_2 (0.5 nm)/TiO_2 (0.5 nm) multilayers with ten periods after annealing treatment. (b) Schematic energy band diagram of the HfO_2(0.5 nm)/TiO_2 (0.5 nm) multilayers with nine quantum wells.

served ~1.7 eV for pure HfO_2 and ~0.9 eV for pure TiO_2 films. Considering all energies in pure HfO_2 and TiO_2 films, a schematic energy band diagram of the HfO_2/TiO_2 multilayer memory structure with ten periods (or nine quantum wells) is shown in Fig. 3(b). In this memory structure, the electrons can be stored in quantum wells under a small positive gate voltage and the stored electrons can be erased easily under a small negative gate voltage, due to small conduction band offset ($\Delta E_c \approx 0.9$ eV) of TiO_2 films. So, a large memory window with a small operation voltage can be expected and it has been confirmed by *C-V* measurement below.

Figure 4(a) shows a counterclockwise *C-V* (1 MHz) hysteresis of high-*k* HfO_2 (0.5 nm)/TiO_2 (0.5 nm) memory capacitor with different sweeping gate voltages (V_g). A holding time was 1 s during *C-V* measurement. A large hysteresis memory window of $\Delta V \approx 5$ V at $V_g = 5$ V is observed. A hysteresis memory window of $\Delta V \approx 1.3$ V at an extremely low gate voltage operation of ±1 V is also observed. The memory window is ~1.6 V for single quantum well device.[15] The hysteresis memory window of high-*k* HfO_2/TiO_2 multilayers is increased with increasing the sweeping gate voltage up to 5 V, while there is no hysteresis memory window of pure HfO_2 trapping layer up to $V_g = 5$ V [Fig. 4(b)]. The pure TiO_2 charge trapping layer does not show any hysteresis memory window up to $V_g = 10$ V. It indicates that the charge can be stored in HfO_2/TiO_2 multilayer quantum wells. The charge loss of multilayer quantum wells is less than 10% after 10 years of retention for high-*k* HfO_2/TiO_2 multilayer memory transistors (not shown here). Large memory window ($\Delta V > 5$ V) with a low gate voltage operation ($V_g < 5$ V) can be used in future multilevel charge storage high-density flash memory device applications.

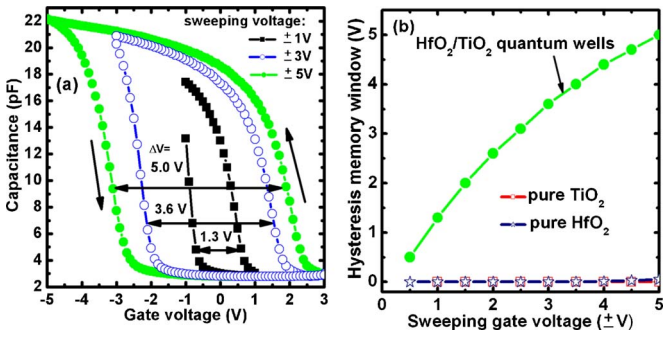

FIG. 4. (Color online) (a) Capacitance vs gate voltage characteristics of the HfO_2/TiO_2 multilayer quantum well memory capacitor. (b) Hysteresis memory window of HfO_2/TiO_2 multilayers, pure HfO_2, and TiO_2 films.

In conclusion, the excellent charge storage characteristics of high-*k* HfO_2/TiO_2 multilayer quantum wells have been observed. The high-*k* HfO_2/TiO_2 multilayer quantum well structure has been confirmed by physical and electrical measurements. A large memory window with a small gate voltage operation of 5 V in HfO_2/TiO_2 multilayer quantum wells has been observed as compared with those of pure HfO_2 and TiO_2 charge trapping layers, due to the charge storage in quantum wells. The high-*k* HfO_2/TiO_2 multilayer quantum wells pave the way in future nanoscale flash memory device applications.

[1] J. R. Hwang, T. L. Lee, H. C. Ma, T. C. Lee, T. H. Chung, C. Y. Chang, S. D. Liu, B. C. Perng, J. W. Hsu, M. Y. Lee, C. Y. Ting, C.-C. Huang, J. H. Shieh, and F.-L. Yang, Tech. Dig. - Int. Electron Devices Meet. **2005**, 161.
[2] S. Choi, M. Cho, H. Hwang, and J. W. Kim, J. Appl. Phys. **94**, 5408 (2003).
[3] T. Sugizaki, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, Symp. on VLSI Tech. Dig. **2003**, 27.
[4] Y.-N. Tan, W.-K. Chim, B. J. Cho, and W.-K. Choi, IEEE Trans. Electron Devices **51**, 1143 (2004).
[5] M. Specht, H. Reisinger, F. Hofmann, T. Schulz, E. Landgraf, R. J. Luyken, W. Rosner, M. Grieb, and L. Risch, Solid-State Electron. **49**, 716 (2005).
[6] Y.-H. Lin, T.-Y. Yang, C.-H. Chien, and T.-F. Lei, Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, 2006, p. 558.
[7] M. S. Joo, S. R. Lee, H. Yang, K. Hong, S.-A. Jang, J. Koo, J. Kim, S. Shin, M. Kim, S. Pyi, N. Kwak, and J.-W. Kim, Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, 2006, p. 982.
[8] C.-H. Lee, S. H. Hur, Y.-C. Shin, J.-H. Choi, D.-G. Park, and K. Kim, Appl. Phys. Lett. **86**, 152908-1 (2005).
[9] S. Maikap, P.-J. Tzeng, L. S. Lee, H. Y. Lee, C. C. Wang, P. H. Tsai, K. S. Chang-Liao, W. J. Chen, K. C. Liu, P. R. Jeng, and M. J. Tsai, 2006 International Symposium on VLSI Technology, System, and Application (VLSI-TSA), 2006, p. 36.
[10] S. Maikap, P. J. Tzeng, T.-Y. Wang, C. H. Lin, H. Y. Lee, C. C. Wang, L. S. Lee, J. R. Yang, and M. J. Tsai, Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, **2006**, p. 984.
[11] P.-J. Tzeng, S. Maikap, C. S. Liang, P. S. Chen, and L. S. Lee, IEEE Trans. Device Mater. Reliab. **5**, 168 (2005).
[12] C. C. Fulton, G. Lucovsky, and R. J. Nemanich, J. Vac. Sci. Technol. B **20**, 1726 (2002).
[13] C. C. Fulton, G. Lucovsky, and R. J. Nemanich, Appl. Phys. Lett. **84**, 580 (2004).
[14] R. Puthenkovilakam and J. P. Chang, J. Appl. Phys. **96**, 2701 (2004).
[15] S. Maikap, P. J. Tzeng, T.-Y. Wang, S. S. Tseng, C. H. Lin, H. Y. Lee, L. S. Lee, P. W. Li, J.-R. Yang, and M. J. Tsai, Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, 2006, p. 582.